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An Active Snubber Cell for N-Phase Interleaved DC-DC Converters

River T. H. Li and Carl N. M. Ho

Abstract – An active snubber cell and its dual circuit for reducing switching losses of 1- to N-phase dc-dc converter is presented. Main switch(s) of the converter can be turned-on and -off at zero-voltage (ZV); switch of the proposed snubber cell can be turned-on at zero-current (ZC) and turned-off at ZV. There are no extra current and voltage stresses will be introduced on the main switch and the reverse recovery current from the main diode can be limited by the snubber inductor. The operating principle and procedure of designing the values of the components will be given. The proposed active snubber cell can be applied into different dc/dc switching converters; the guidelines of connection of the cell will be illustrated. The performance of the proposed active snubber circuit has been evaluated on a 2kW, 180V_{in}, 400V_{out} interleaved boost converter prototype. Results show that switching losses of the converter are significantly reduced and the conversion efficiency is increased by 0.8% at rated load. The peak efficiency of the converter is higher than 97.9%. Experimental results are in good agreement with the theoretical predictions.

Index Terms – snubber; zero-voltage; zero-current; resonant; dc-dc converter; interleaving

I. INTRODUCTION

Low cost, high efficiency, high power density and light weight are the practical research focuses and design targets of modern power electronic converters. Recently, Wide-band gap semiconductors, such as SiC and GaN devices, have rapidly developed to improve the performance of converters and it has been shown that they are very effective in switching loss reduction [1]-[2], this results higher system power density due to utilization of higher switching frequency and lower thermal requirement. Although power density and weight of the converter can be improved, high component cost is still the downside in the near future. Besides, reliability issue is another barrier that oppose widely use of the devices [3]. Snubber circuit is the classical solution to tackle the same tasks and it can help to improve the EMI issue concurrently [4]-[5]. Snubber circuit can be basically classified into two technical categories, which are passive and active approaches. Passive snubber assists the main power switch to turn-on at Zero Current (ZC) and turn-off at Zero Voltage (ZV) without additional active device [6]-[7]. However, ZV turn-on is more favor for MOSFETs from the loss point of view and it cannot normally achieved by only passive snubber.

In emerging power electronic applications, interleaving techniques are commonly adopted in power supplies [8], solar inverters [1]-[2], Fuel Cell interfaces [9], power quality conditioners [10], and automotive applications [11]-[12], since this typically results in the lowest conduction loss and component cost. There are at least two converter cells in one interleaved dc-dc converter. And the two switching cells switch at 180° phase shifted. This results small output (buck converters) or input (boost converters) ripple current. Besides, the main current is shared by two cells, the thickness of copper windings is thinner. This leads easier for manufacturing. And low rated current class semiconductors can be used to have better semiconductor thermal management and increase the switching frequency this leads to reduce the inductances [2]. Active snubber circuits can also be applied to interleaved dc-dc converters to further improve

the switching efficiency and the power density. However, most of the conventional active snubber circuits which serve one switching cell by one snubber circuit [13]-[18]. In other words, it requires N snubber circuits to serve an N-phase interleaved dc-dc converter to achieve ZV or ZC switching. This leads complex control and driving circuit for the snubber circuits and it also reflects on the component cost and the system reliability.

In this paper, an active snubber circuit cell that can work for various types of power converter with single- or multi-phase topologies will be presented. The premier idea is to realize a cost-efficient solution especially in the multi-phase topologies as only one snubber circuit is required. Switching frequency of the converter can be increased due to the switching loss reduction. The magnetic parts will be beneficial coordinately from the low cost and low loss material, such as ferrite, due to the reduction in required inductance. The proposed snubber circuit cell and its variants are described in Section II and the simplified design guideline is given in Section III. The proposed solution is demonstrated in Section IV by a 50kHz per phase, 180V_{in}, 400V_{out}, 2kW interleaved boost converter experimentally as an example. The peak efficiency of the converter is higher than 97.9%; experimental results are in good agreement with the theoretical prediction.

II. OPERATING RINCIPLES

A. *The Proposed Snubber Circuit Cells*

Fig. 1 shows the proposed active snubber circuit cells. For single phase converter application, the snubber circuit consists of 1 active switch, 3 diodes, 2 inductors and 1 capacitor. The auxiliary switch, S_a, is turned-on at ZC and turned-off at ZV. Fig. 2 shows integrations of the proposed active snubber circuit cells to power converters, node A(1) should be connected to the common node of main switch, main diode and current source. Node B should be connected to the common node of main diode and voltage source. Node C should be connected to the common node of main switch and voltage source. In principle, operation of the two snubber cells is the

same except the polarity of current and voltage across the devices are reversed. Selection of the cell is based on the converter configuration. As shown in Fig. 2, Cell A is selected when current is flowing from node A to node B; otherwise, cell B is selected. Table I shows the values of V_x and I_x for different converters.

B. Boost Converter with the Proposed Snubber Circuit

The operation of a boost converter with the proposed snubber circuit is explained in this section. Fig. 3 shows the circuit diagram of a boost converter with the proposed snubber circuit. Fig. 4 shows the key waveforms and Fig. 5 shows the operating modes of the converter.

Mode 1 ($t_0 < t < t_1$)

Main switch, *S*, is off and the main diode, *D*, is on. The converter operates in the off-state until the auxiliary switch, S_a, turns-on at $t = t_1$.

Mode 2 ($t_1 < t < t_2$)

S_a turns-on at $t = t_1$ at ZC due to the present of L_s and L_{st}. i_D starts to decrease and i_{Sa} starts to increase correspondingly until i_D equals to zero and i_{Sa} equals to I_{in}. The di_D/dt is limited by L_s, reverse recovery current, as well as the reverse recovery loss, of *D* is reduced.

$$i_{L_s}(t) = \begin{cases} \frac{V_{out}}{L_s}(t - t_1) & i_{L_s}(t) \le I_{in} \\ V_{out}\sqrt{\frac{C_{ds\_S}}{L_s}}\sin[\omega_2(t - t_{1'})] + I_{in} & i_{L_s}(t) \ge I_{in} \end{cases} \quad (1)$$

where $t_1 < t_{1'} < t_2$.

The resonant paths, $L_{st} - D_{s1} - C_s - S_a$ and $C_{ds\_S} - L_s - S_a$, are excited when S_a is closed. The resonance ends when i_{Lst} equals to zero. The drain-source capacitor of the main switch, C_{ds_S}, and C_s start to discharge in this mode.

$$i_{L_{st}}(t) = v_{C_s}(t_2)\sqrt{\frac{C_s}{L_{st}}}\sin[\omega_1(t - t_2)] \quad (2)$$

$$v_{C_s}(t) = v_{C_s}(t_1)\cos[\omega_1(t - t_2)] \quad (3)$$

$$v_{C_{ds}}(t) = V_{out}\cos[\omega_2(t - t_2)] \quad (4)$$

$$\omega_1 = \frac{1}{\sqrt{L_{st}C_s}} \text{ and } \omega_2 = \frac{1}{\sqrt{L_s C_{ds\_S}}} \quad (5)$$

This mode ends when v_{Cds_S} is fully discharged.

Mode 3 ($t_2 < t < t_3$)

This mode starts when the body diode of *S* starts to conduct. v_{Cds_S} is clamped to zero. i_{Ls} equals to I_{in} and the path, $L_{st} - D_{s1} - C_s - S_a$, is continuing the resonance action from mode 2.

$$\boldsymbol{i_{L_s}(t) = I_{in}} \quad (6)$$

$$i_{L_{st}}(t) = v_{C_s}(t_2)\sqrt{\frac{C_s}{L_{st}}}\sin[\omega_1(t - t_2)] \quad (7)$$

$$v_{C_s}(t) = v_{C_s}(t_2)\cos[\omega_1(t - t_2)] \quad (8)$$

$$v_{C_{ds\_S}}(t) = 0 \quad (9)$$

C_s keeps discharging until v_{Cs} reaches negative V_{out}. D_{s2} will conduct and v_{Cs} is clamped to negative V_{out}. This mode ends when the resonant is finished and i_{Lst} equals to zero.

Mode 4 ($t_3 < t < t_4$)

This mode starts when i_{Lst} equals to zero. i_{Ls} conductor via the anti-parallel diode of *S*, therefore, *S* can be turned-on at ZV.

$$i_{L_s} = V_{out}\sqrt{\frac{C_{ds}}{L_s}}\sin[\omega_2(t - t_3)] + I_{in} \quad (10)$$

$$i_{L_{st}}(t) = 0 \quad (11)$$

$$v_{C_s}(t) = v_{C_s}(t_3) \quad (12)$$

$$v_{C_{ds\_S}}(t) = 0 \quad (13)$$

Voltage across *S* is clamped to zero and it can be turned-on during this mode at ZV. This mode ends when S_a starts to turn-off.

Mode 5 ($t_4 < t < t_5$)

This mode starts when S_a is turned-off. C_{ds_Sa} is charged by i_{Ls} until $v_{C_{ds\_S}} + v_{C_s} = V_{out}$. i_{Ls} will start to charge C_{ds_Sa} and discharge C_s until i_{Ls} equals to zero.

$$i_{L_s}(t) = [v_{C_s}(t_6) + V_{out}]\sqrt{\frac{C_{ds\_Sa}+C_s}{L_s}}\sin[\omega_3(t-t_6)] + i_{L_s}(t_4)\cos[\omega_3(t-t_6)] \quad (14)$$

$$i_{L_{st}}(t) = 0 \quad (15)$$

$$v_{C_s}(t) = i_{L_s}(t_6)\sqrt{\frac{L_s}{C_{ds\_Sa}+C_s}}\sin[\omega_3(t-t_6)] - [v_{C_s}(t_6) + V_{out}]\{1-\cos[\omega_3(t-t_6)]\} + v_{C_s}(t_6) \quad (16)$$

$$v_{C_{ds\_Sa}}(t) = \frac{1}{C_{ds\_Sa}+C_s}\left\{\left[-\frac{v_{C_s}(t_4)+V_{out}}{\omega_3}\sqrt{\frac{C_{ds\_Sa}+C_s}{C_s}}\cos[\omega_3(t-t_4)]\right] + \frac{i_{L_s}(t_4)}{\omega_3}\sin[\omega_3(t-t_4)]\right\} \quad (17)$$

$$\omega_3 = \frac{1}{\sqrt{L_s C_{ds\_Sa}}} \quad (18)$$

Mode 6 ($t_5 < t < t_6$)

This mode starts after i_{Ls} reaching zero. The converter is in on-state operating mode. This mode ends at the end of duty cycle.

Mode 7 ($t_6 < t < t_7$)

This mode starts when *S* turns-off. The *dv/dt* across *S*, as well as the turn-off loss, is reduced because the present of C_{ds_S}. This mode ends when V_{Cds_S} equals to V_{out}.

$$v_{C_{ds}}(t) = \frac{I_{in}(t-t_7)}{C_{ds\_S}} \quad (19)$$

The operation of one switching cycle is completed. The power converter returns to Mode 1.

III. SIMPLIFIED DESIGN PROCEDURES

The determination of the snubber circuit passive components values are described in this section.

A. *Design of resonant inductor, L_s:*

The value of L_s is depended on the reverse recovery characteristic of the main diode. The value can be determined by,

$$L_s = \frac{2\Delta Q_{rr} V_{out}}{(1+Snap)I_{rr}^2} \quad (20)$$

where I_{rr} is the peak reverse recover current, *Snap* is the snappiness factor of the main diode [19], Q_{rr} is the reverse recovery charge of the main diode. Notice that, $\widehat{I_S} = I_{in} + I_{rr}$.

B. *Design of dv/dt limiled capacitors, C_{ds_S} and C_{ds_Sa}:*

C_{ds_S} and C_{ds_Sa} are used to suppress the turn-off *dv/dt* and turn-off loss across *S* and S_a respectively. Design of C_{ds_S} should consider the turn-off loss and current stress across *S* as shown in Eq. (1). Similarly, design of C_{ds_Sa} should consider the turn-off loss of S_a. Accordingly, the value of C_{ds_S} and C_{ds_Sa} are 47pF in the prototype.

C. *Design of resonant capacitor, C_s:*

The energy stored in L_s has to be transferred to C_{ds_Sa} and C_s. In order to reduce the *dv/dt* and turn-off loss across S_a, v_{Cs} has to be charged until V_{out}. Therefore,

$$C_s = \frac{L_s}{v_{C_{ds\_S_a}}^2}\left(I_{in} + V_{out}\sqrt{\frac{C_{ds\_S}}{L_s}}\right)^2 - C_{ds\_S_a} \tag{21}$$

D. *Design of di/dt limited inductor, L_{st}:*

L_{st} assists S_a to turn-on at ZC. The value of L_{st} can be determined by considering the current stress across S_a and it is determined as follow,

$$L_{st} = C_s\left(\frac{V_{out}}{\widehat{iL_{st}}}\right)^2 \tag{22}$$

The proposed active snubber circuit cells can be applied to different converters respect to the connection criteria mentioned in Section II.A. Fig. 6 shows the application in the basic converter configurations, including buck, buck-boost, SEPIC and Cuk converters.

IV. EXPERIMENTAL VERIFICATION

A 50kHz per phase, 180V_{in}, 400V_{out}, 2kW two phases interleaved boost converter with the proposed active snubber cell has been built for experimental verifications. Fig. 7 shows the circuit schematic. The passive components values of the snubber circuit are determined based on the design guideline given in Section III and tableted in Table II.

A. *Operations of interleaved boost converter with the proposed active snubber circuit*

For the application of the proposed active snubber in the interleaved boost converter, or other N-phase converters, the gate signal of S_a has to be synchronized with the turn-on time of S_1 and S_2. The gate signals of S_1 and S_2 are 180° phase shifted, the operation condition is the same for duty ratio < 0.5 and duty ratio ≥ 0.5. However, the main switch and main diode current waveforms are different between these two cases.

For duty ratio < 0.5, S_a turns-on near the end of the duty cycle of S_1 so as to assist S_1 to turn-on at ZV. D_1 and D_2 are conducting at this moment as shown in Fig. 8 (a). Therefore, current will commutate from D_1 and D_2 to S_a. When S_1 is on, S_a can be turned-off and current will commutate back to D_2 as shown in Fig. 8 (b). As a result, there is a "notch" in the D_2 current as shown in Fig. 9. The situation is the same for D_1 when S_a is assisting the turn-on action of S_2.

Similarly, for duty ratio ≥ 0.5, S_a turns-on near the end of the duty cycle of S_1 so as to assist S_1 to turn-on at ZV. D_1 and S_2 are conducting at this moment as shown in Fig. 10 (a). Therefore, current will commutate from D_1 and S_2 to S_a. When S_1 is on, S_a can be turned-off and current will commutate back to S_2 as shown in Fig. 10(b). As a result, there is a "notch" in the S_2 current as shown in Fig. 11. The situation is the same for S_1 when S_a is assisting the turn-on action of S_2.

The operation of the converter and inductor current ripple magnitude will not be affected by the snubber in both operating modes.

B. *Loss breakdown of an interleaved boost converter*

Fig. 12 shows measured switching losses of a CoolMOS, SPP24N60C3, and an Ultrafast diode, MUR1660CT, by double pulse test at 75˚C and 125˚C junction temperature [20]. $R_{DS(on)}$ of the MOSFET is around 205mΩ; the diode has a forward voltage drop and an on-state resistance of around 1.1V and 25mΩ, respectively, at 75˚C as shown in Fig. 13. Fig. 14 shows the converter input inductor currents at different loading conditions. The proposed active

snubber has no inference to the input current for both discontinuous and continuous conduction modes. The semiconductor loss breakdown for an interleaved boost converter with input current ripple equals to 22% is summarized in Table III.

C. Switching Performance

From Table III, the turn-on current at 50% load, 1kW, is very small, 0.2A. Thus the turn-on loss can be neglected. The total switching loss is ~6.4W for two MOSFETs at 75˚C and which is consumed 0.64% efficiency. At 100% load, 2kW, the total switching loss including 2 MOSFETs and 2 diodes is ~26.4W and which consumed 1.32% of the converter efficiency. Fig. 15 shows the gate signals pattern for the duty ratio larger 0.5. Fig. 16 shows the switching waveforms of one of the main switches. The gate signal is applied after the drain-source voltage of the switch reaches zero. Therefore, the main switch is turned-on at ZV. Fig. 17 is the enlarged turn-on waveform of the main switch. A small reverse recovery exists while the auxiliary switch turns-off. It can be reduced by slow down the turn-off speed of the auxiliary switch. Fig. 18 shows the enlarged turn-off waveform of the main switch where the turn-off loss is very small. Oscillation happens after turning off; it is caused by the PCB stray inductance and the output capacitance of the main switch. It can be reduced by improving the PCB layout. Fig. 19 shows an efficiency comparison of the interleaved boost converter with and without the proposed snubber circuit. The peak efficiency of the converter with the proposed active snubber is higher than 97.9% and ~0.8% efficiency increment at 100% load. Fig. 20 shows the prototype for experimental verification.

V. CONCLUSION

In this paper, an active snubber circuit for a range of power converters to realize soft-switching is presented. The main switch can be turned-on and -off at ZV while the auxiliary switch can be turned-on at ZC and turned-off at ZV. Only one snubber circuit is required for multi-phase topologies. A 2kW, 400V_{out}, 50kHz per phase switching frequency interleaved boost has been

built for experimental verification. The experimental results show the switches are switching at very low loss. However, the conduction loss in the snubber circuit which is proportional to its operating duration. Thus, it is preferred to disable the snubber circuit when the converter is in discontinuous conduction mode, as the main switches and diodes are turned-on and -off at ZC respectively. The peak efficiency of the 2kW interleaved boost converter with the proposed active snubber circuit is higher than 97.9%. The overall efficiency can be further increased by optimizing the loss of the input chokes and minimizing the conduction time of the snubber cell. Applications of the proposed snubber cells in different topologies and design guidelines are presented coordinately.

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Footnote

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Figures Captions

Fig. 1. Circuit schematic of the proposed active snubber circuit cells.

Fig. 2. Required connection of the proposed snubber. (a) Cell A. (b) Cell B.

Fig. 3. Integration of the proposed active snubber into a boost converter.

Fig. 4. Key waveforms of boost converter with the proposed active snubber circuit.

Fig. 5. Modes of operations.

Fig. 6. Application of the proposed active snubber circuit cell in different basic converters (a) buck, (b) buck-boost, (c) SEPIC and (d) CUK.

Fig. 7. Interleaved boost converter with the proposed active snubber circuit.

Fig. 8. (a) Commutation from *D1* and *D2* to *Sa* and (b) Commutation from *Sa* to *D2*

Fig. 9. Switchig waveforms when D < 0.5

Fig. 10. (a) Commutation from *D1* and *S2* to *Sa* and (b) Commutation from *Sa* to *S2*

Fig. 11. Switchig waveforms when D > 0.5

Fig. 12. Dynamic characterization of the MOSFET and diode.

Fig. 13. Static characterization of (a) $RDS_{(on)}$ of MOSFET and (b) *Vf* of diode.

Fig. 14. Input current waveform of the interleaved boost converter with the proposed active snubber

Fig. 15. Gate pattern of the interleaved boost converter.

Fig. 16. Switching waveform of the one of the main switches.

Fig. 17. Enlarged turn-on waveform of the main switch.

Fig. 18. Enlarged turn-off waveform of the main switch.

Fig. 19. Measured efficiency of the interleaved boost converter with and without the proposed active snubber circuit.

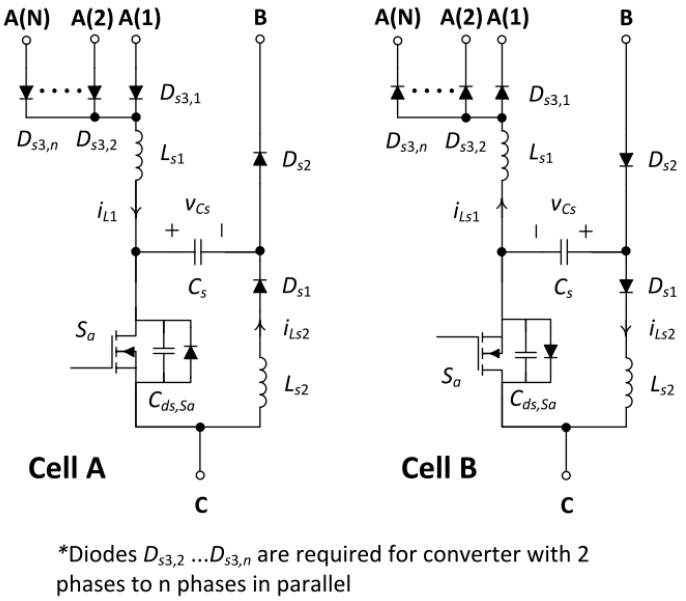
Fig. 20. Photos of the experimental prototype (a) top side and (b) bottom side.

TABLE I. VALUE OF V_X AND I_X FOR DIFFERENT CONVERTERS.

Table II. Component values of the experimental prototype

Table III. SEMICONDUCTOR LOSS BREAKDOWN OF BOOST CONVERTER (VIN = 180V, VOUT = 400V, CURRENT RIPPLE = 22%, SWITCHING FREQUENCY = 50KHZ, JUNCTION TEMPERATURE = 75˚C)

Tables Captions



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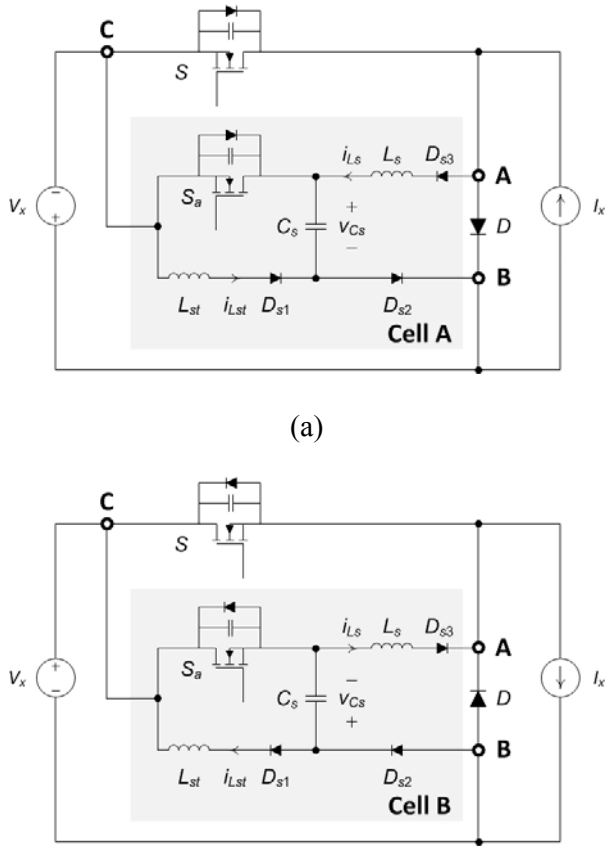

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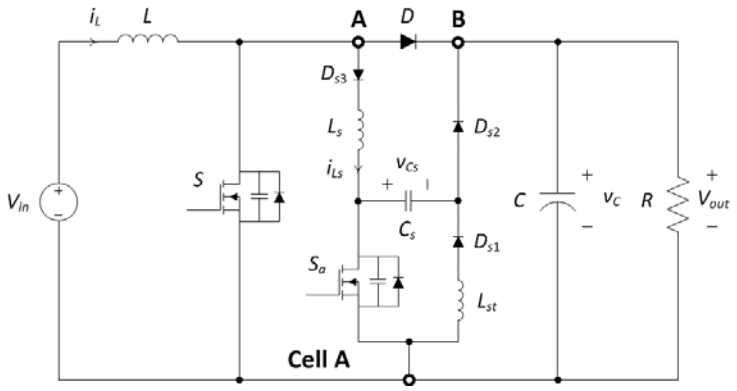

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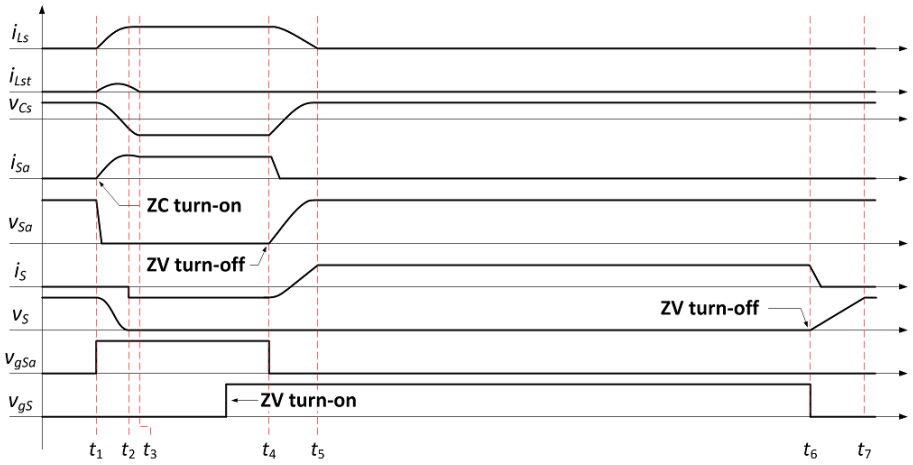


Fig. 4. Key waveforms of boost converter with the proposed active snubber circuit.

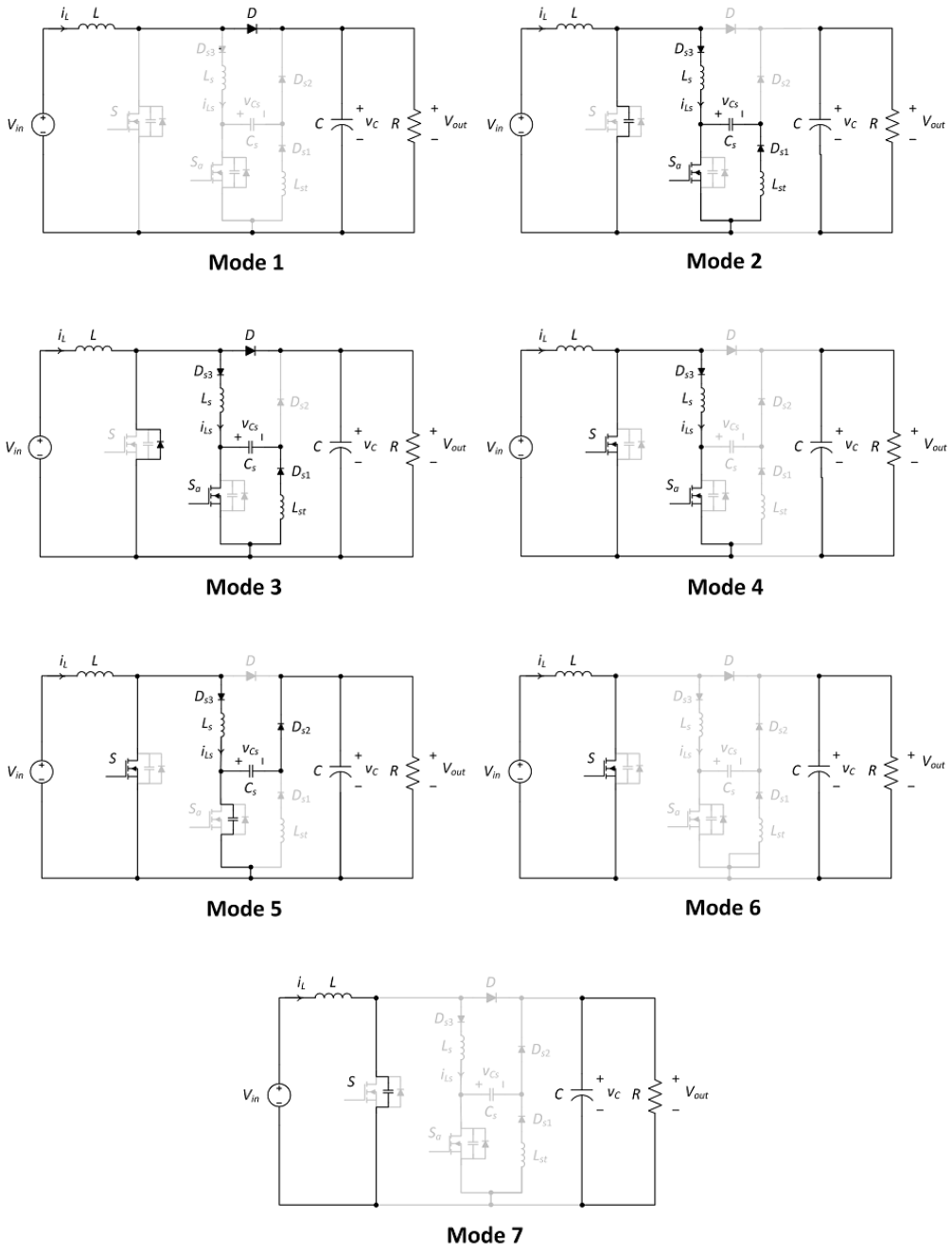


Fig. 5. Modes of operations.

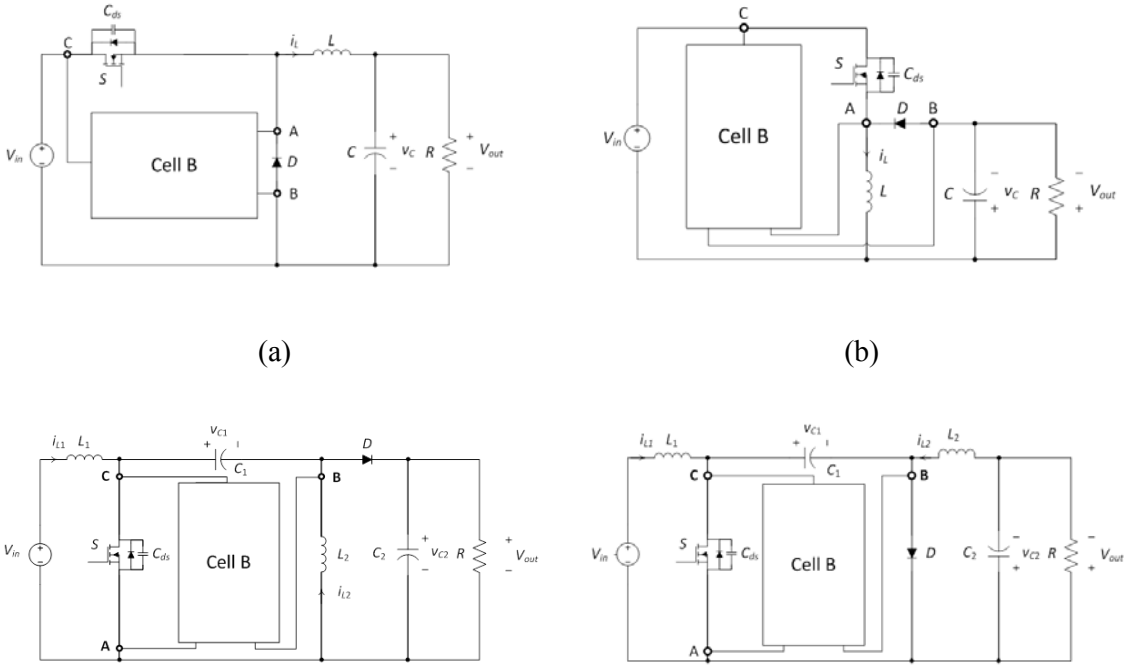


Fig. 6. Application of the proposed active snubber circuit cell in different basic converters (a) buck, (b) buck-boost, (c) SEPIC and (d) CUK.

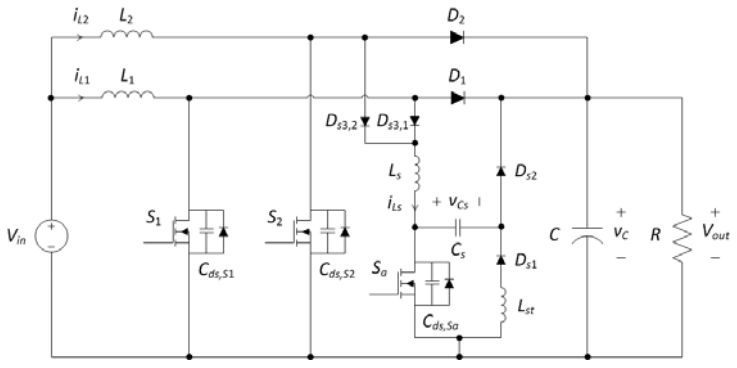


Fig. 7. Interleaved boost converter with the proposed active snubber circuit.

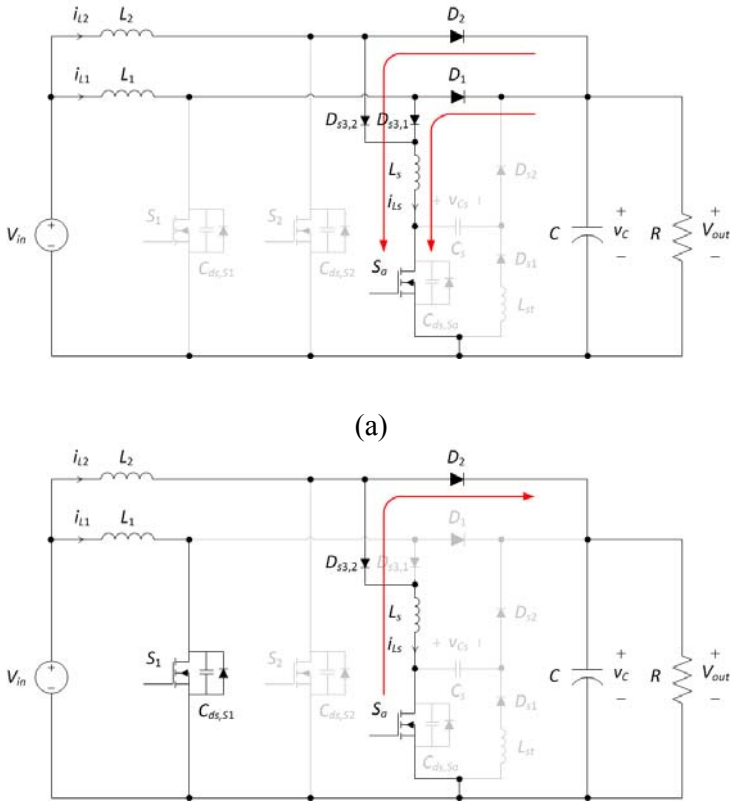


Fig. 8. (a) Commutation from D_1 and D_2 to S_a and (b) Commutation from S_a to D_2.

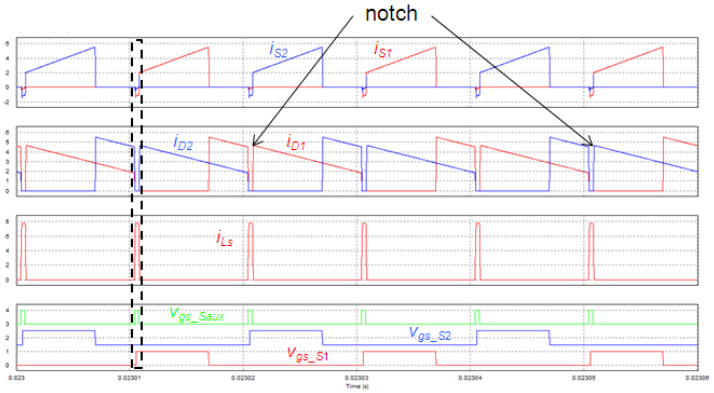
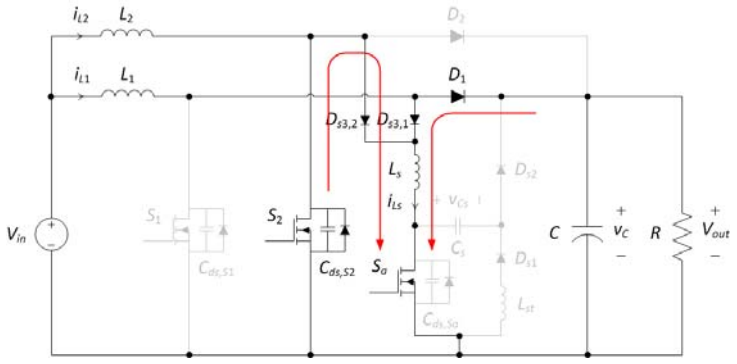
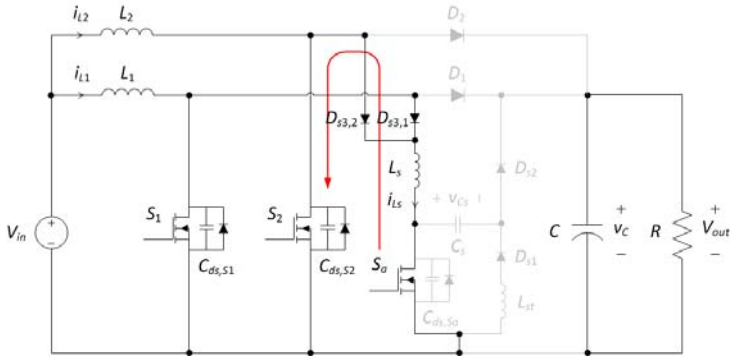


Fig. 9. Switchig waveforms when D < 0.5.



(a)



(b)

Fig. 10. (a) Commutation from D_1 and S_2 to S_a and (b) Commutation from S_a to S_2 .

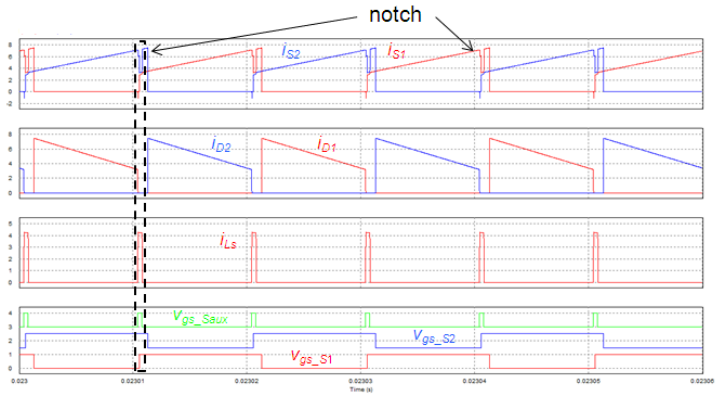


Fig. 11. Switchig waveforms when D > 0.5.

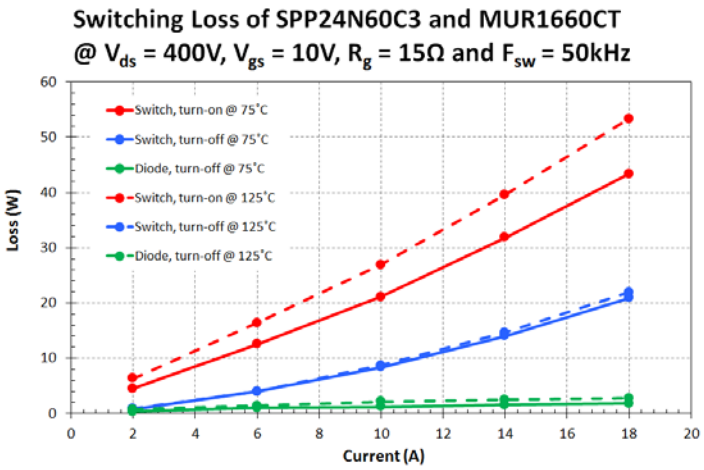
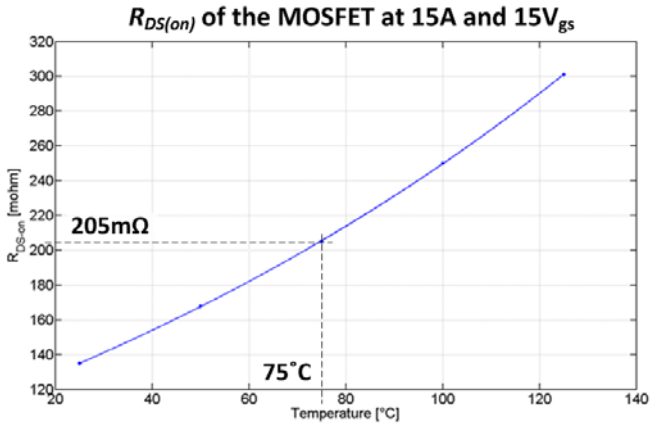
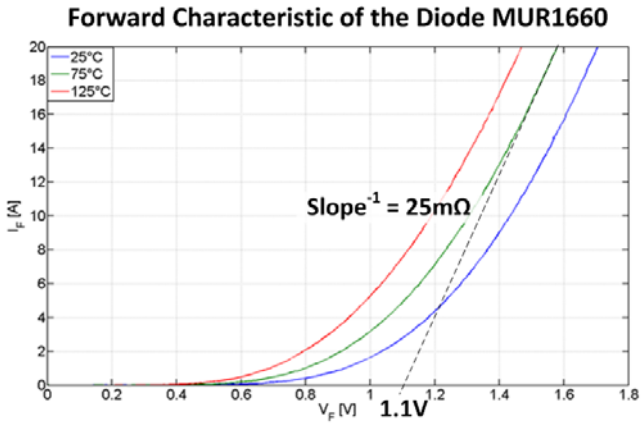


Fig. 12. Dynamic characterization of the MOSFET and diode.



(a)



(b)

Fig. 13. Static characterization of (a) $R_{DS(on)}$ of MOSFET and (b) V_f of diode.

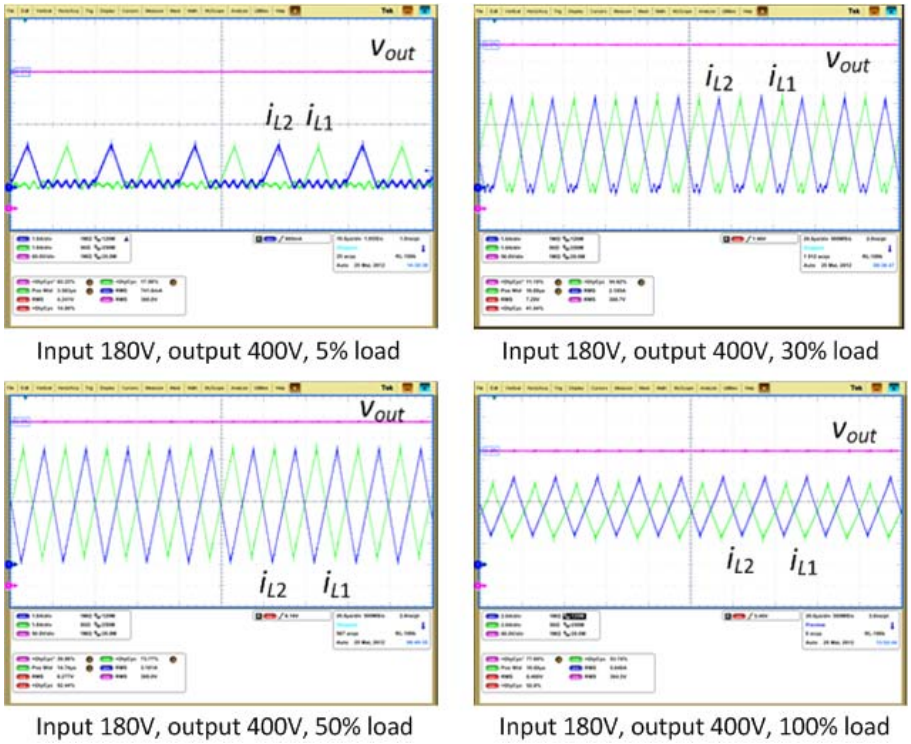


Fig. 14. Input current waveform of the interleaved boost converter with the proposed active snubber

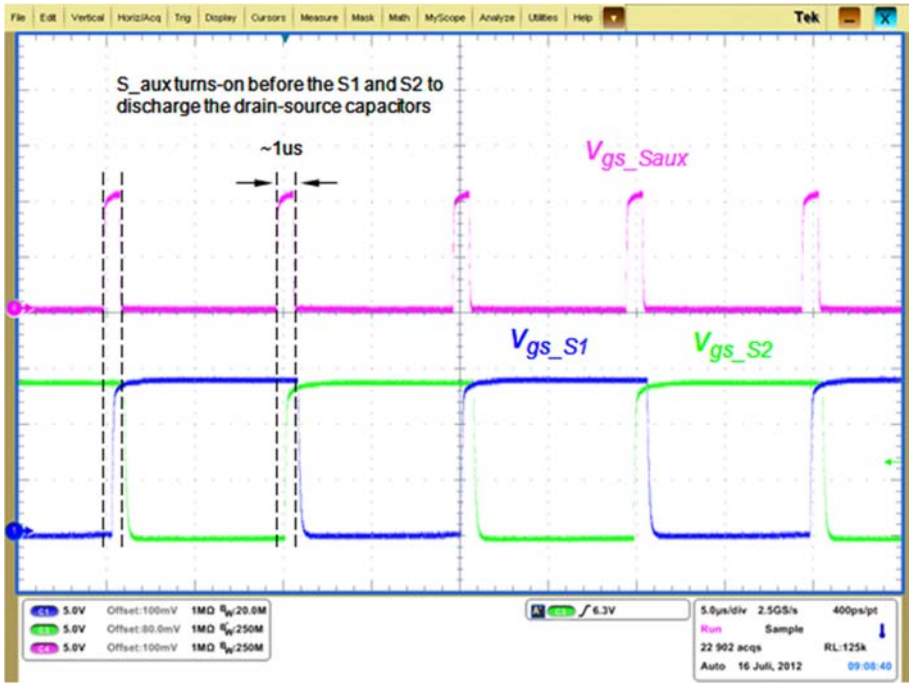


Fig. 15. Gate pattern of the interleaved boost converter.

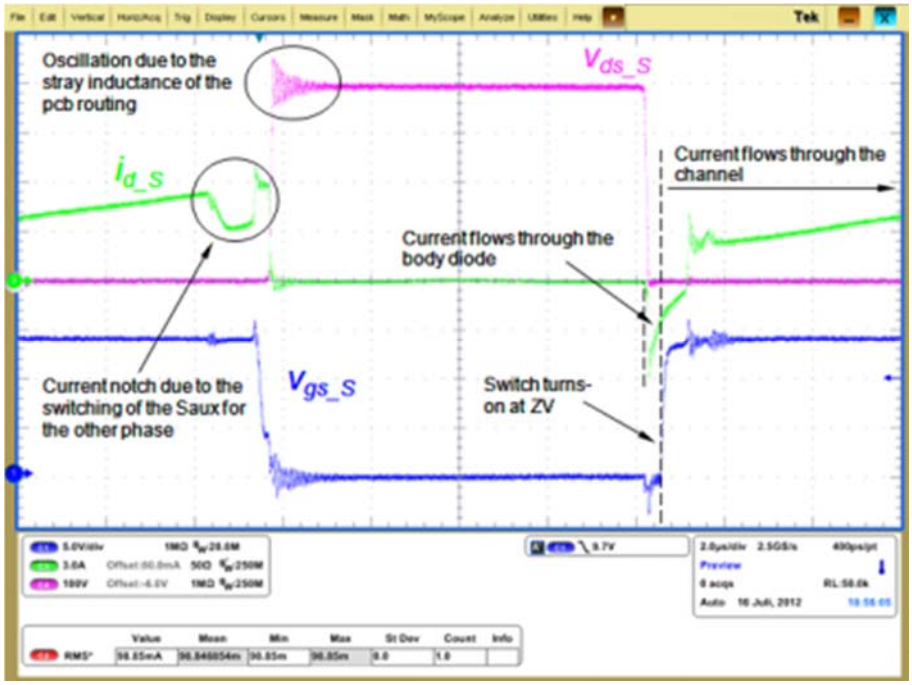


Fig. 16. Switching waveform of the one of the main switches.

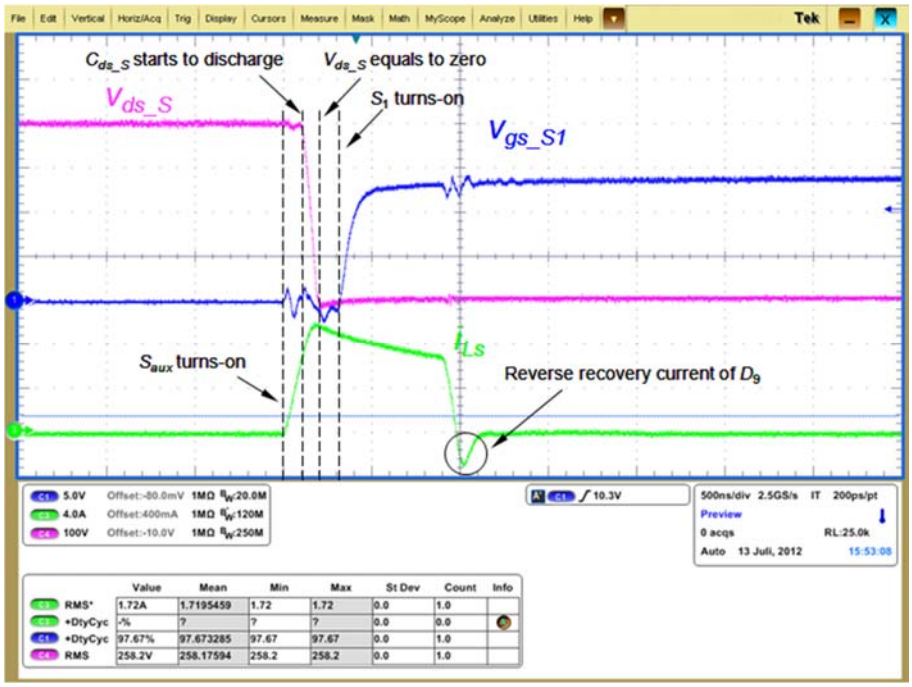


Fig. 17. Enlarged turn-on waveform of the main switch.

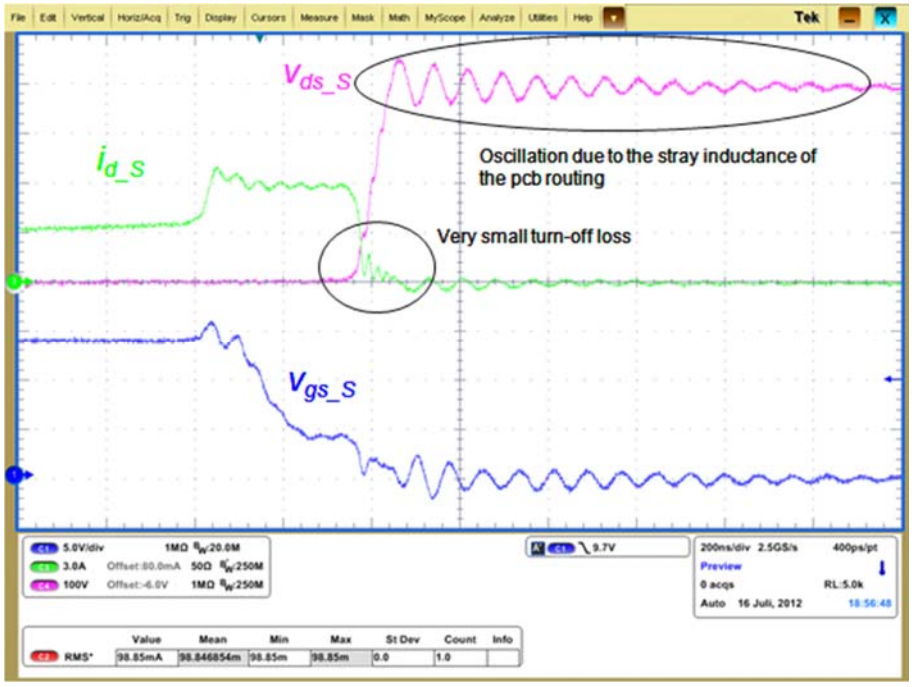


Fig. 18. Enlarged turn-off waveform of the main switch.

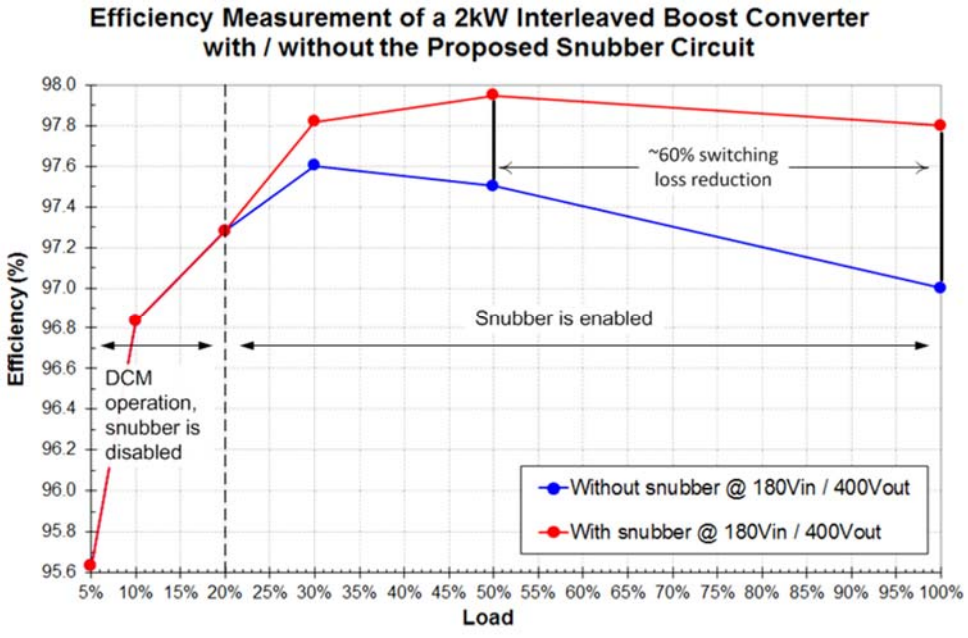
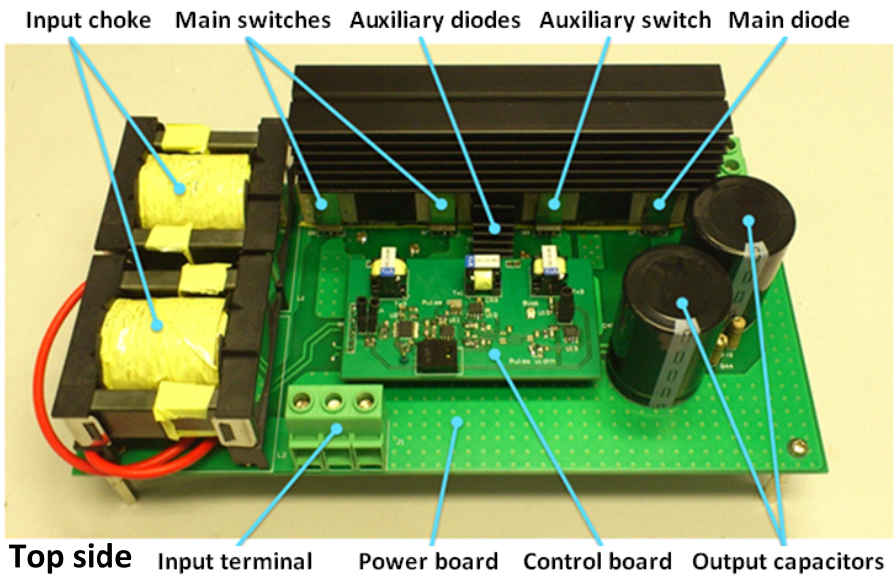
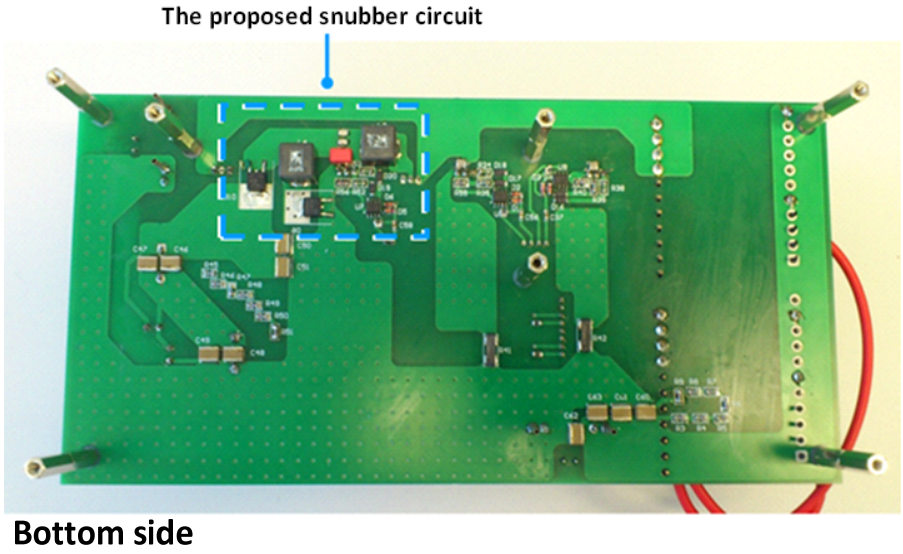


Fig. 19. Measured efficiency of the interleaved boost converter with and without the proposed active snubber circuit.



(a)



(b)

Fig. 20. Photos of the experimental prototype (a) top side and (b) bottom side.

TABLE I. VALUE OF V_X AND I_X FOR DIFFERENT CONVERTERS.

Converter type	V_x	I_x
Buck	V_{in}	I_L
Boost	V_{out}	I_L
Buck-boost	$V_{in} + V_{out}$	I_L
SPEIC	$V_{C1} + V_{out}$	$I_{L1} + I_{L2}$
CUK	V_{C1}	$I_{L1} + I_{L2}$

TABLE II. COMPONENT VALUES OF THE EXPERIMENTAL PROTOTYPE

ITEM	**VALUE**	**ITEM**	**VALUE**
L_1, L_2	450μH (3C90)	S_1, S_2	SPP24N60C3
C_1, C_2	560μF	S_A	STP9NK90Z
D_1, D_2	MUR1660CT	L_S	4.7μH
F_{SW_S}	50KHz	F_{SW_SA}	100KHz
D_{S1}, D_{S2}	VS-5EWX06FN-M3	C_S	450PF
D_{S1}	ISL9K460P3	L_{ST}	2.2μH

Table III. SEMICONDUCTOR LOSS BREAKDOWN OF BOOST CONVERTER (VIN = 180V, VOUT = 400V, CURRENT RIPPLE = 22%, SWITCHING FREQUENCY = 50KHZ, JUNCTION TEMPERATURE = 75˚C)

Power	**Turn-on current**	**Turn-off current**	**Switch turn-on loss**	**Switch turn-off loss**	**Diode turn-off loss**
1kW	0.2A	5.2A	~0W(*DCM)	3.2W	~0W
2kW	3A	8A	6.55W	6.15W	0.5W
Power	**Switch RMS current**	**Diode AVE current**	**Switch conduction loss**	**Diode conduction loss**	
1kW	2.3A	1.3A	1.08W	1.48W	
2kW	4.1A	2.5A	3.82W	3.21W	

*DCM : Discontinuous conduction mode.