Active Virtual Ground - Bridgeless PFC Topology

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***Abstract* – The paper presents a new bridgeless Power Factor Correction (PFC) topology, using a recently proposed controllable *LCL* filter, namely Active Virtual Ground (AVG) to achieve efficient power conversion, and high frequency (HF) common mode voltage (CM) reduction. The proposed PFC circuit consists of high frequency semiconductors for shaping inductor current, and low frequency semiconductors to form two different *LCL* structures for different conditions. This reduces grid differential mode (DM) current ripple or inductance. Besides, the PFC CM voltage, a main problem of bridgeless PFCs, is significantly reduced, since the capacitor in the *LCL* filter clamps the voltage between the grid and the converter ground. The performance of the proposed PFC is experimentally verified. The results show that the proposed PFC guarantees sinusoidal input current, low high frequency common-mode voltage noise and has a good agreement with the theoretical findings.**

***Index Terms*—PFC, AVG, Common mode, EMI, LCL.**

I. INTRODUCTION

Power Factor Correction (PFC) circuit is a front-end power stage of grid-connected power converter, such as power supply, motor drive and electronic ballast [1]-[7]. It is used to meet international grid current standards, such as IEEE519 and IEC-61000-3-2 (for 1-phase). And those standards are also applied to single phase grid network which is typically as an AC power source for low power industrial applications and household devices. By using a PFC in a system, it ensures sinusoidal input current and stable output DC voltage. It can be foreseen that PFC will be a very important device to ensure good power quality in further complex grid network. Among PFC topologies, Bridgeless PFC (BPFC) was proposed in the early 80s [8] and it is promising in terms of efficiency due to fewer semiconductors in the current paths. However, common mode (CM) voltage issue leading to leakage current issue is the limitation of the topology in a lot of applications [9]. The CM voltage issue creates Electro-Magnetic Interference (EMI) problems.

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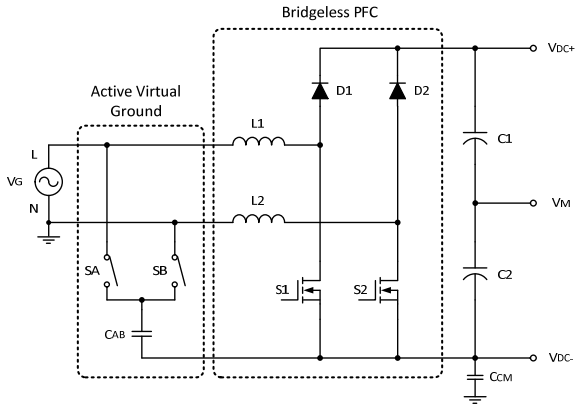


Fig. 1 The proposed single phase bridgeless PFC topology

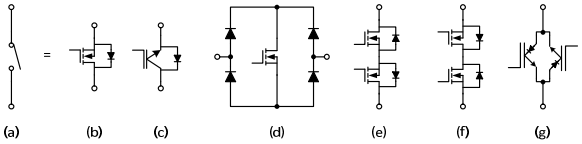


Fig. 2 Bi-directional switch arrangements, (a) Ideal switch, (b) MOSFET, (c) IGBT, (d) Diode bridge, (e) Common emitter back-to-back, (f) Common drain back-to-back, and (g) anti-paralleled reverse blocking IGBTs.

Some methodologies have been proposed to solve the CM voltage issue for BPFC, they can be classified into three categories. The first is to give an electrical isolation. Generally, it gives an additional current circulating path [10] or disconnects the leakage current path [11] by using additional semiconductors. However, they increase semiconductor cost and conduction losses, as extra full power rating semiconductor devices are required and they are in the main PFC current path. The second is to use additional semiconductors to clamp the common mode voltage to be zero either using diodes [12], the original topology was in [13], or active switches [14], [15]. The method effectively suspends the common mode voltage due to physically connecting the converter-ground to a grid terminal, but the inductors are not fully utilized which cause high differential mode (DM) current to the grid. The third is to use capacitors to clamp the common mode voltage [16] - [18]. It is a good approach to give low impedance paths for the high frequency components, but the large HF DM current is still presenting in the grid terminals due to two capacitors are in parallel for high frequency components and the grid is in between. Therefore, the methods can solve the CM voltage issue, but they creates other problems such as higher semiconductor conduction losses, larger grid current ripple

and higher system or component design complexity.

This paper proposes a new bridgeless PFC topology to transform single-phase AC voltage to DC voltage. Fig. 1 shows the proposed topology. The PFC consists of a conventional BPFC and an additional circuit. The additional circuit can change the input filter to different *LCL* structures depending on grid voltage polarities by using the built-in BPFC inductors. This results a reduction of grid side DM current ripple or required inductance of the input chokes. Besides, the PFC can mitigate the conventional CM voltage issue, since the capacitor in *LCL* filter clamps the voltage between the grid and the negative terminal of dc bus and provides a low impedance path for high frequency components. Thus, this technique is namely Active Virtual Ground (AVG). This paper will define the problems, explain the operating principle of the proposed converter, provide steady-state characteristics, and experimental results will be demonstrated to verify the proposed concept. A simple add-on AVG circuit and a 300 W BPFC have been built. The AVG circuit can be simply connected in front of the BPFC then it will give the advantages of 1) low CM voltage, and 2) low grid side DM ripple current and will keep the low conduction loss advantages of BPFC, since the AVG circuit only manages the high frequency current and it is in parallel with the main current path.

II. Principles of Operation

Fig. 1 shows that the proposed bridgeless BPFC boosts an AC grid voltage to a higher DC bus voltage and regulates the dc component of the DC bus voltage to a desired value. The circuit includes a typical BPFC circuit and an AVG circuit. The AVG circuit filters out high frequency (HF) components which are generated by the BPFC during switching. It avoids the HF components flowing through the ac grid. The additional circuit consists of two bi-directional switches (S_A and S_B) connecting in series, and they are coupled to a Line (L) and Neutral (N) of the grid separately. The bi-directional switches (S_A or S_B) can be realized by connecting two MOSFETs back-to-back in series or other configurations which is shown in Fig. 2. The switches switch alternatively and synchronize with the line frequency. The AVG circuit also includes a capacitor (C_{AB}) that is coupled between the junction point of the two bi-directional switches (S_A and S_B) and any point of the DC bus, such as the negative of DC bus (V_{DC-}). It is used to clamp the potential difference between the AC power source and the converter ground. From a high frequency noise's point of view, there is a very low impedance path between the dc link and the system ground. And the path is different in positive and negative half line cycles, it requires semiconductors to reconfigure the high frequency path. Thus, the circuit and technology are named as Active Virtual Ground (AVG) [19], [20].

A. Operating Mode: Positive half line cycle

In Fig. 3, there are two switching states in the proposed BPFC during a positive half line cycle. In this half line cycle, the filter capacitor (C_{AB}) is connected to the Line (L) of grid voltage source through the bi-directional switch (S_A), the main switch (S_2) is always conducting and the main switch (S_1) is switching at a high frequency. Fig. 3 (a) and (b) show the circuit when the main switch (S_1) switching on and off, respectively. Fig. 4 (a) and (b) are corresponding equivalent circuits of Fig. 3 (a) and (b), note that S_2 is always conducting thus it is not shown in the circuits. It can be seen that L_1, C_{AB} and L_2 form a *LCL* filter between the grid and the switching cell S_1 and D_1. In this case, L_2 takes the role of grid inductor L_G, then a low grid differential mode (DM) current ripple is achieved. And C_{AB} is coupled between the Line (L) and the negative terminal of DC bus, the potential difference between them is clamped, therefore a low CM leakage current is achieved.

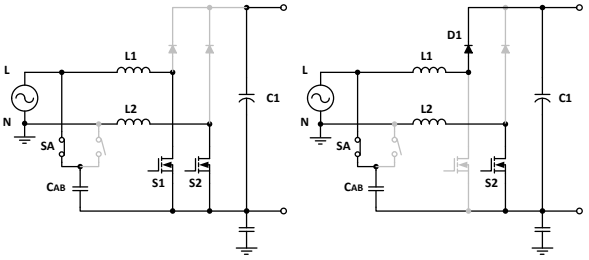


Fig. 3 Current conducting paths of the AVG-BPFC in positive line cycle, (a) S_1 is ON, and (b) S_1 is OFF.

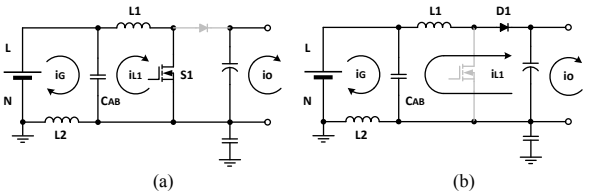


Fig. 4 Equivalent circuits of the AVG-BPFC in positive line cycle, (a) S_1 is ON, and (b) S_1 is OFF.

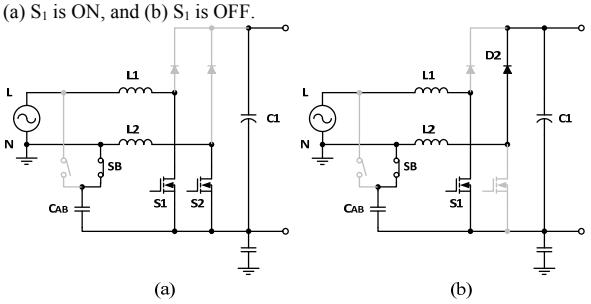


Fig. 5 Current conducting paths of the AVG-BPFC in negative line cycle, (a) S_2 is ON, and (b) S_2 is OFF.

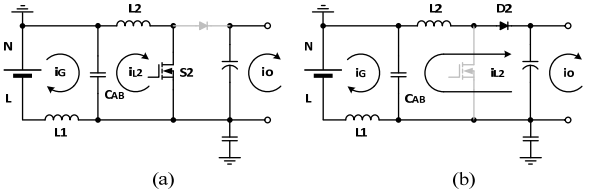


Fig. 6 Equivalent circuits of the AVG-BPFC in negative line cycle, (a) S_2 is ON, and (b) S_2 is OFF.

B. Operating Mode: Negative half line cycle

In Fig. 5, there are two switching states in the proposed BPFC during a Negative half line cycle. In this half line

cycle, C_{AB} is connected to N of grid voltage source through S_B, S_1 is always conducting and S_2 is switching at a high frequency. Fig. 5 (a) and (b) show the circuit when S_2 switching on and off, respectively. Fig. 6 (a) and (b) are corresponding equivalent circuits of Fig. 5 (a) and (b). It can be seen that L_2, C_{AB} and L_1 form a *LCL* filter between the grid and the boost converter. In this case, L_1 takes the role of L_G, then a low grid DM current ripple is achieved. And C_{AB} is coupled between N and the negative terminal of DC bus, the potential difference between them is clamped, therefore a low CM leakage current is achieved.

C. Modulation Scheme

Control methodology of the AVG circuit is simple. Fig. 7 shows an example of a controller for a BPFC with the proposed AVG circuit. In principle, the controller is compatible to a conventional BPFC. It consists of an outer voltage controller to regulate the DC bus voltage and an inner current controller to shape the converter-side inductor L_C currents. The AVG gate signals, S_A and S_B, are took from the outputs of a Polarity Detector to synchronize the AVG gate signals and the grid voltage v_G. Fig. 8 shows simplified gate signals for the proposed topology. The AVG gate signals, S_A and S_B, are with the line frequency and complementary. The main switches, S_1 and S_2, switch at high frequency in a half line cycle alternately to shape the currents of L_1 and L_2, respectively. It is important to note that semiconductor losses can be minimized by the modulation scheme,

- Switching losses of the main switches: There is only one pair of switching cell with high frequency switching at all time.
- Conduction losses of the main switches: When the main switch is not with high frequency switching, it is turned on to let the reverse current go through the channel instead of the body diode. Generally, a channel of a MOSFET is lower voltage drop than a body diode of a MOSFET [21].
- Switching losses of the AVG switches: The AVG switches switch at grid voltage zero crossings. In principle, it is also the zero crossing points of the grid current, thus it is zero current switching. Besides, the switching frequency is the line frequency, e.g. 60Hz. Thus, switching losses of the AVG Switches can be neglected.
- Conduction losses of the AVG switches: The fundamental PFC current component does not pass through the AVG circuit. The circuit only conducts the high frequency inductor ripple current. Generally, a root-mean-square value of inductor ripple current is small, thus the conduction losses are also small.

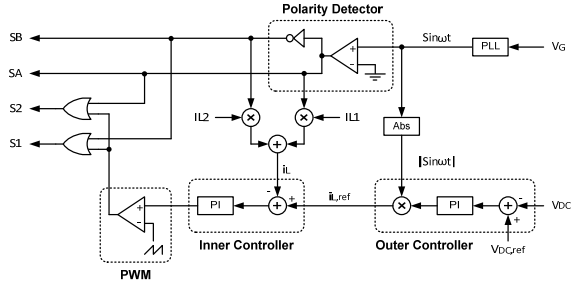


Fig. 7 Controller block diagram for the AVG-BPFC topology.

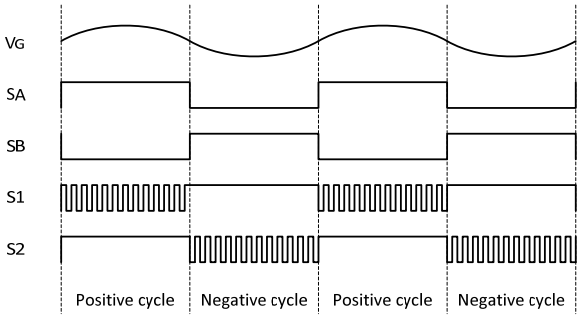


Fig. 8 Simplified gate signals for the AVG-BPFC topology.

III. STEADY-STATE CHARACTERISTICS

A. Duty Ratio

The inductors, L_1 and L_2, act as converter-side inductors L_C and grid-side inductors L_G, which depends on the grid voltage polarity. In the case of positive half line cycle, L_1 is the converter-side inductor L_C, and Fig. 4 (a) and (b) indicate the equivalent circuits of on and off states.

Neglecting the voltage drop on the grid inductor, the AVG capacitor voltage v_C is the same as the grid voltage, thus,

$$v_C(t) \approx v_G(t) = V_G \sin \omega t \tag{1}$$

where v_G is the instantaneous grid voltage, V_G is the peak amplitude of grid voltage, and ω is the angular line frequency.

Fig. 4 and Fig. 6 shows the on and off states of the main switches. The PFC operation is the same as a simple boost converter. Thus, the duty ratio D can be expressed by,

$$D(t) = 1 - \frac{V_G}{V_{DC}} \sin \omega t \tag{2}$$

where V_{DC} is the output DC bus voltage.

A detailed derivation of (2) is given in the Appendix.

B. Converter-side Inductor Current Ripple

The duty ratio is time varying in a line cycle following the change of grid voltage, which is shown in (2). Besides, in order to simplify the calculations, the inductances of L_1 and L_2 are assumed as identical and represented by L_X, i.e. $L_X = L_1 = L_2 = L_C = L_G$. If a constant switching frequency and continuous-conduction mode inductor current are considered, the converter-side current ripple Δi_{LC} can be found as,

$$\Delta i_{LC}(t) = \frac{(V_{DC} - V_G \sin \omega t) V_G \sin \omega t}{V_{DC} L_X f_{sw}} \quad (3)$$

where f_{sw} is the switching frequency.

A detailed derivation of (3) is given in the Appendix.

C. AVG Capacitor Voltage Ripple

The voltage ripple of AVG capacitor is mainly contributed by the current ripple of converter-side inductor, thus the voltage ripple peak to peak value Δv_C is,

$$\Delta v_C(t) = \frac{(V_{DC} - V_G \sin \omega t) V_G \sin \omega t}{8 V_{DC} C_{AB} L_X f_{sw}^2} \quad (4)$$

where C_{AB} is the capacitance of AVG capacitor.

A detailed derivation of (4) is given in the Appendix.

D. Grid-side Inductor Current Ripple

The grid current is the same as the grid-side inductor current. The current ripple peak to peak value Δi_G is,

$$\Delta i_G(t) = \frac{(V_{DC} - V_G \sin \omega t) V_G \sin \omega t}{16 \pi V_{DC} C_{AB} L_X^2 f_{sw}^3}. \quad (5)$$

A detailed derivation of (5) is given in the Appendix.

E. Common-mode Voltage

The CM parasitic capacitor C_{CM} is shown in Fig. 1. Fig. 9 shows the high frequency (HF) equivalent circuit of the BPFC with AVG. It can be seen that the CM capacitor is in parallel to the AVG capacitor. Thus, the HF CM voltage ripple is the same as the AVG capacitor ripple. By modifying (4), the HF CM voltage ripple Δv_{CM} can be obtained,

$$\Delta v_{CM}(t) = \frac{(V_{DC} - V_G \sin \omega t) V_G \sin \omega t}{8 V_{DC} (C_{AB} + C_{CM}) L_X f_{sw}^2} \quad (6)$$

where C_{CM} is the capacitance of the parasitic CM capacitor.

Typically, the value of the parasitic CM capacitor is much smaller than that of the AVG capacitor, e.g. 4.7 nF and 4.7 uF, respectively. According to that assumption the HF CM voltage is almost the same as the AVG capacitor ripple voltage.

F. Common-mode Leakage Current

The HF CM leakage current is defined as the current passing through the CM capacitor and the grid terminals, it is shown with dash line in Fig. 9. According to the HF CM equivalent circuit in Fig. 9, the HF CM leakage current is from the converter-side inductor ripple current, and the current is shared by the AVG capacitor. Thus, a current divider equation can be used to determine the HF CM leakage current Δi_{HFCM} in the circuit,

$$\Delta i_{HFCM}(t) = \frac{C_{CM}}{C_{AB} + C_{CM}} \Delta i_{LC}(t). \quad (7)$$

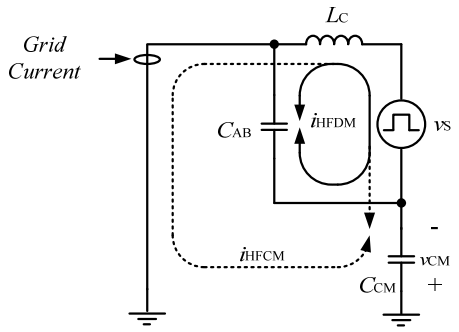


Fig. 9 High frequency common mode equivalent circuit of a BPFC with AVG.

G. Frequency Response of AVG filter

The proposed AVG circuit is used to change a first-order *L* filter to become a third-order *LCL* filter. The equivalent circuits were shown in Fig. 4 and Fig. 6. Thus the conventional *LCL* filter transfer function can be applied to the AVG filter [22] - [23],

$$G_{AVG}(\mathrm{s}) = \frac{-i_G(\mathrm{s})}{u_{S1/S2}(\mathrm{s})} = \frac{-1}{\mathrm{s}(L_1 L_2 C_{AB} \mathrm{s}^2 + L_1 + L_2)} \quad (8)$$

where $u_{S1/S2}(s)$ is the voltage across S_1 or S_2, that is the HF signal source of the *LCL* filter.

The grid and converter inductances of the AVG circuit are identical. Thus, Eq. (8) can be simplified as,

$$G_{AVG}(\mathrm{s}) = \frac{1/2L_X}{\mathrm{s}\left(\frac{L_X C_{AB}}{2}\mathrm{s}^2 + 1\right)}. \quad (9)$$

The AVG circuit's characteristic resonance frequency, ω_r, can be determined as,

$$\omega_r = \sqrt{\frac{2}{L_X C_{AB}}}. \quad (10)$$

IV. Variants of AVG-BPFC

The AVG concept can be implemented by various topologies to operate as the modes in Fig. 4 and Fig. 6. And the control methodology and the gate signals in Fig. 7 and Fig. 8 can be applied.

Fig. 10 (a) is a "Common-Source" type AVG-BPFC. It spits the AVG capacitor (C_{AB}) into two independent capacitors (C_{A} and C_{B}), and they only operate in a half line cycle by controlling the AVG switches, S_{A} and S_{B}. The advantage of the circuit is that it simplifies the gate drive circuit, since all active semiconductor devices are reference to one point, in other words, no isolation is required for gate drive and sensing circuits. However, there are one additional AVG capacitor is required. It is suitable to low power and low cost applications.

Fig. 10 (b) is an "X-Type" AVG-BPFC. It is similar to "Common-Source" type topology, it uses two independent AVG branches, one switch and one capacitor in series. The branches connect to the boost inductors (L_1 and L_2) in "X-Shape". The advantage of the X-Shape type topology is easily adding the AVG circuit in an existing BPFC without connecting to the negative terminal of dc link capacitor.

However, it requires two low frequency floating gate drivers for the AVG switches.

Fig. 10 (c) and (d) are "H-Type" and "2Y-Type" AVG-BPFCs, respectively. The concept of the topologies is similar to "X-Type" but using one AVG capacitor. Thus, the advantage and the disadvantage are the same as the "X-Type" circuit. All in all, all types of AVG circuits are good for high power applications, since the AVG circuit is only managing the high frequency ripple current.

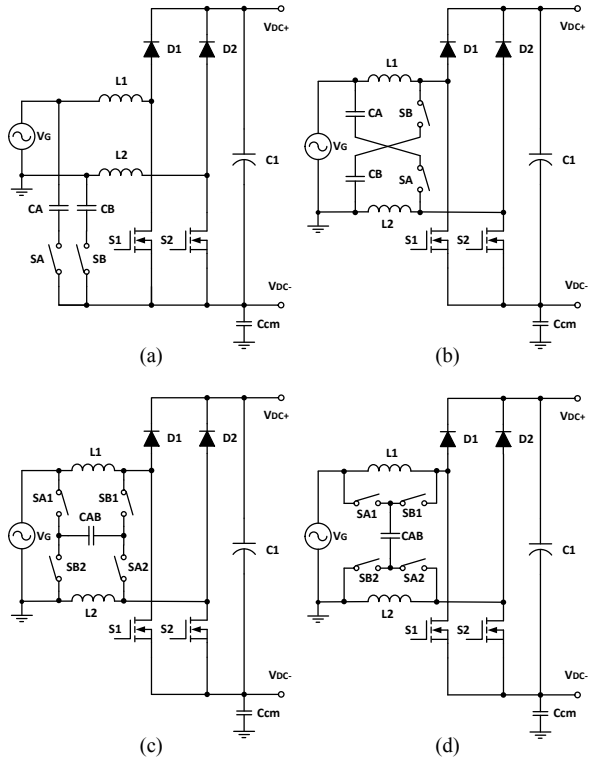


Fig. 10 Four AVG variants for BPFC, (a) Common-source, (b) X-shaped, (c) H-shaped and (d) 2Y-shaped.

V. System Implementation

A 300 W, 120 V / 60 Hz input, 400 V output voltages BPFC converter prototype has been used to evaluate the proposed topology, the specification is shown in Table I. The BPFC is a commercial product, Texas Instruments (TI) HV Bridgeless PFC Developer's Kit [27] - [28], with removing the high frequency input filter. A 60 Hz switching frequency AVG circuit has been implemented. Fig. 11 (a) and (b) show a testbed photo and a system block diagram of the laboratory setup, respectively, for evaluating the proposed AVG-BPFC topology. The photo shows two PCBs, the right hand side one is the conventional BPFC, another one is the AVG circuit. The AVG circuit works like an "add-on" circuit by connecting three terminals to the BPFC, which is shown in Fig. 11(b). A TI designed BPFC controller is used [29]. It is a peak current controller and is implemented by a Digital Signal Processor (DSP). The AVG controller is a simple open loop analog polarity detector with dead time circuits. It turns on S_A when v_G is positive voltage and turns on S_B when v_G is negative voltage. A 300 W resistive load bank is used and connected to the DC bus of the BFPC. The AVG capacitor, C_{AB}, value is chosen as 4.7 uF which is based on two criteria,

1. Maximum leakage current, there are some industrial standards to limit the leakage current to be suppressed to a certain level, such as 30 mA [24] and 7 mA [25], to protect equipment and human beings. And a typical stray capacitance (C_{CM}) for a PFC is about 5 nF [26]. Thus, according to the equations (3) and (7), the AVG capacitor value is limited by,

$$C_{AB} \geq \frac{C_{CM}}{\Delta i_{HFCM}} \frac{(V_{DC}-\hat{V}_G)\hat{V}_G}{V_{DC}L_X f_{sw}} - C_{CM}. \quad (11)$$

By the use of the circuit values from Table I and setting the maximum leakage current as 7mA, the minimum capacitor value of C_{AB} is calculated as 2.32 uF based on equation (11).

2. Maximum resonance frequency, in order to avoid the interferences between the resonance frequency and the switching frequency, at least 20 times difference is chosen. By using the equation (10), the AVG capacitor is limited by,

$$C_{AB} \geq \frac{2}{L_X}\left(\frac{20}{2\pi f_{sw}}\right)^2. \quad (12)$$

By putting the values from Table I into equation (12), thus C_{AB} must be bigger than 3.37 uF for the frequencies interference point of value.

Thus, a standard value 4.7 uF is chosen as the value of the AVG capacitor in the prototype which can be satisfied both of the above criteria.

Although the AVG circuit is implemented as an "add-on" circuit for a commercial BPFC for demonstrating the AVG circuit can change the conventional BPFC topology to the AVG-BPFC without any converter or system controller modifications, the AVG circuit also can be integrated into the BPFC when designing a new converter. All necessary signals for the AVG circuit will be outputted by the system DSP. In other words, it requires extra two semiconductor switches and their gate drivers, and an AC capacitor only.

TABLE I
SPECIFICATION OF THE PROTOTYPE OF AVG-BPFC SYSTEM

Parameter	Value	Parameter	Value
v_G	120 V	V_{DC}	400 V
P_O	300 W	f_{sw}	200 kHz
L_1, L_2	150 uH	C_{AB}	4.7 uF

In order to verify the system design and the steady state equations, a simulation has been created and evaluate the AVG circuit and BPFC system. All parameters are the same as the designed system which shows in Table I and using 5 nF as the common mode capacitor. Fig. 12 shows the waveforms from the simulation. The calculated peak value of leakage current, which is determined by (3) and (7) and shown with the dash line in Fig. 12, is the same as

the envelop of the simulated leakage current. Similarity, the calculated peak value of common voltage, which is determined by (6) and shown with the dash in Fig. 12, is the same as the envelop of the simulated common mode voltage. This simulation ensures that the designed system has a good agreement with the determined steady state characteristics.

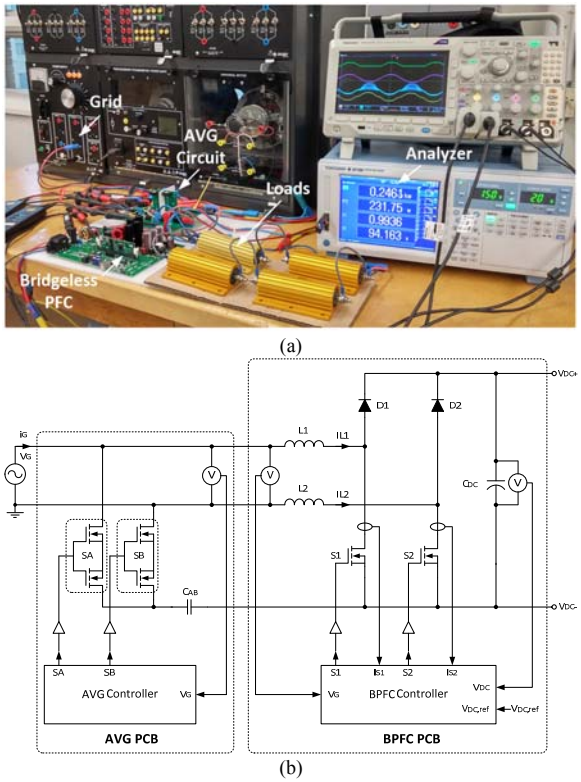


Fig. 11 Experimental setup.

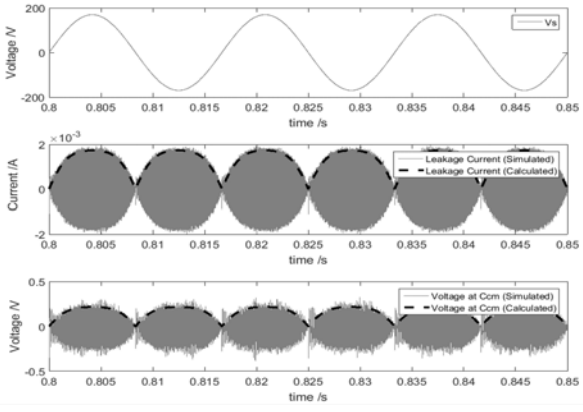


Fig. 12 Simulation waveforms of high frequency leakage current and common mode voltage.

VI. Experimental Verification

Performance of the built prototype is experimentally demonstrated in the section. In contrast, two other conventional HF DM and CM mitigation techniques, cascading a HF filter and capacitor-clamped circuit, are compared experimentally. The schematics are shown in Fig. 13.

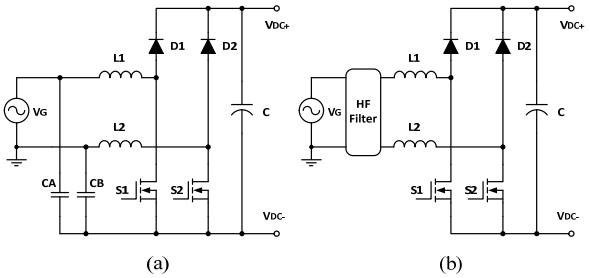


Fig. 13 Conversional BPFCs with (a) high frequency filter, and (b) capacitor-clamped circuit.

A. DM and CM noises mitigating performance.

Fig. 14 (a) and (b) show experimental results of the BPFC without and with the AVG circuit, respectively. It shows that the BPFC generates high frequency noise to interference the grid voltage without the AVG circuit in Fig. 14 (a) and the grid current ripple is large. It is improved significantly by adding the AVG circuit as shown in Fig. 14 (b), the grid current ripple reduced and the grid voltage did not have interference since the filter becomes a *LCL* filter in the converter. And the switches in the AVG circuit are switching at low frequency (60Hz) and synchronized with the grid voltage.

Fig. 15 (a) to (d) show experimental results of the BPFC without and with different DM and CM noises mitigation methods. Fig. 15 (a) shows that there is a huge HF CM voltage in the conventional BPFC. Besides, the grid current and inductor current are identical where high frequency current ripples are in both positive and negative half cycles. The DM and CM noises affect the shape of the input voltage. Fig. 15 (b) shows the BPFC operating with a cascaded HF filter which is shown in Fig. 13 (a). The corresponding structure of the TI pre-installed HF filter is shown in Fig. 16 [28]. The grid current quality is improved, a detailed explanation of the equivalent circuit model is given in the Appendix. However the HF CM voltage remains large amplitude and it affects the grid voltage quality. Fig. 15 (c) shows the BPFC with capacitor-clamped circuit which is shown in Fig. 13 (b) and was proposed in [16] where two 4.7 uF capacitors were used. The high frequency CM noise is minimized which can be seen by the CM voltage waveform, however the grid current carries a HF DM current. The reason is that there are two HF paths (two capacitors) for high frequencies returning to the noise source. One of the paths is in series with the grid source, therefore the HF noise appears in the grid current, a detailed explanation of the equivalent circuit model is given in the Appendix. But in Fig. 15 (d), it shows the HF CM voltage is minimized by the AVG circuit. And the inductor current has a large current ripple in the positive half cycles, since the inductor acts as a converter side inductor in the *LCL* filter. The inductor current has very small current ripple in the negative half cycles, since the inductor acts as a grid side inductor in the *LCL* filter. There is a low frequency CM

voltage in the results of the capacitor-clamped and the AVG BPFCs, since the grid voltage is in between the measurement points (Line terminal to negative terminal of dc link) during the positive half line cycle. But the low frequency CM voltage does not generate leakage current. Similarly, there is a HF CM voltage in the results of the capacitor-clamped and the AVG BPFCs. Those two techniques do not completely suspend the HF CM voltage, they reduce the voltage to an acceptable level to avoid of generating high leakage current. The HF CM voltage amplitude of the capacitor-clamped and the AVG BPFCs are presented in (A12) and (6), respectively. Besides, the measured power factor of AVG-BPFC converter can achieve 0.9953.

The experimental results proved that the DM and CM noises of a BPFC converter can be improved at the same time by simply adding an AVG circuit in the front without any modification of the main circuit of BPFC and its controller.

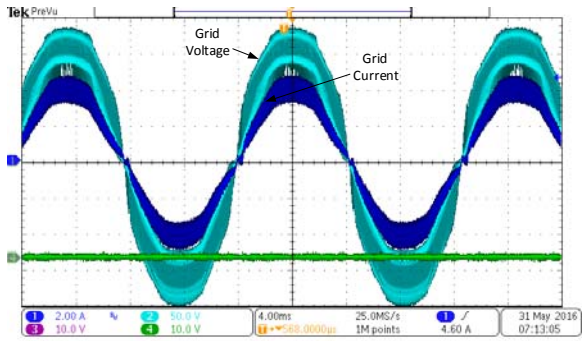


Fig. 14 Experimental results, (a) conventional, and (b) with proposed circuit.

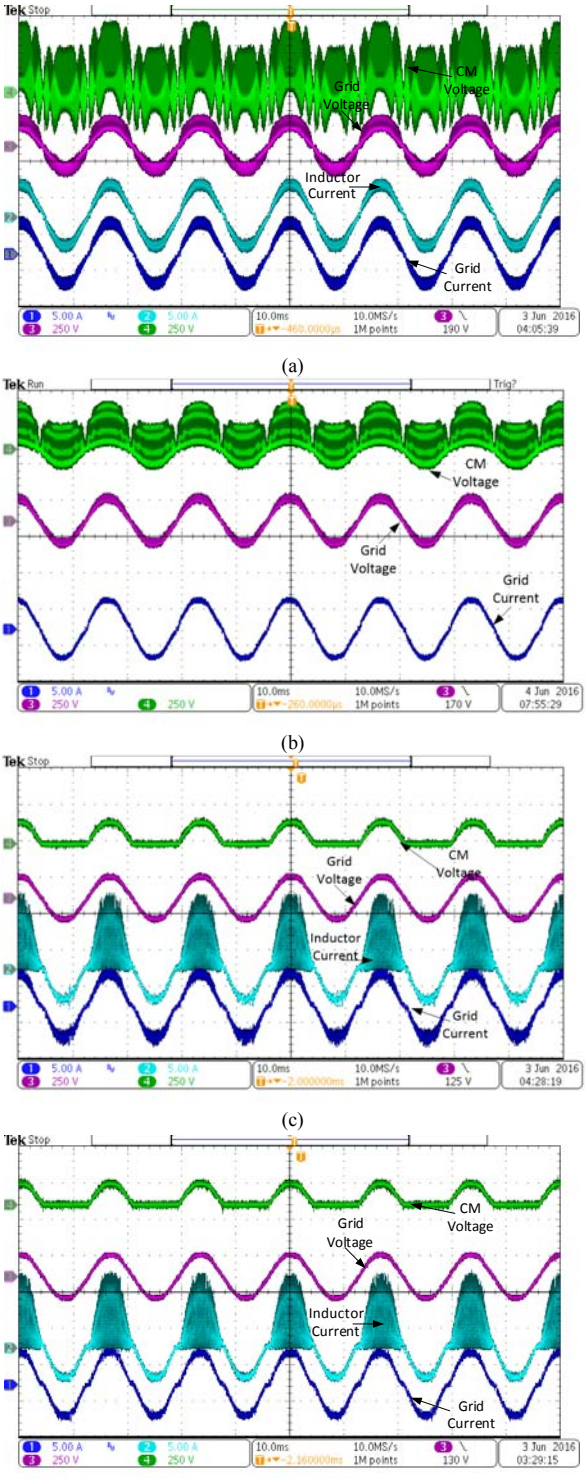


Fig. 15 Experimental results, (a) conventional, (b) with HF filter, (c) with capacitor clamped circuit and (d) with the proposed AVG circuit.

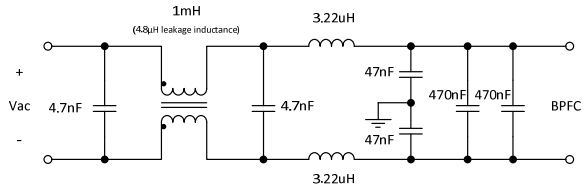
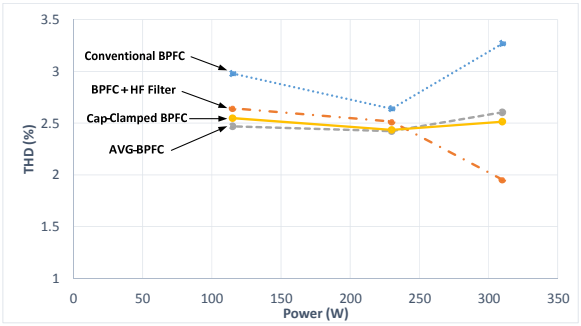


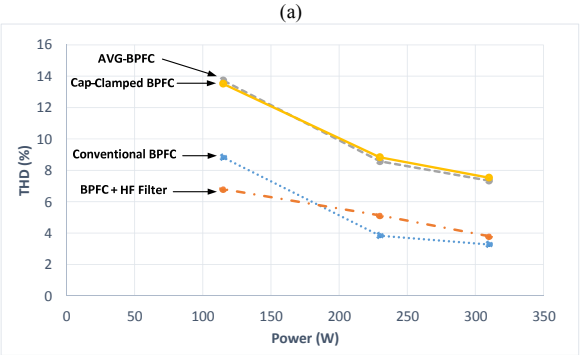
Fig. 16 A high frequency filter for the BPFC [28].

B. Grid-side voltage quality and current quality

The grid current waveforms shown in Fig. 14 (b) appears a short dead zone (0.17 ms) at the zero crossing. This dead zone affects the grid current quality. The possible reason of generating that dead zone is the TI built-in controller is optimized for the original first-order filter, when the AVG circuit is applied, it forms a third-order *LCL* filter. The built-in controller controls the converter-side inductor current to be sinusoidal and in-phase with the grid voltage. Thus, the phase of grid current is shifted due to the AVG capacitor, C_{AB}, contributing a reactive current. As a result, although the add-on AVG circuit improves the THD of grid voltage, which is shown in Fig. 17 (a), due to lower CM voltage, it increases the THD of grid current due to the zero crossing distortion. It is a drawback of the AVG technique for the particular system. Fig. 17 shows a comparison of the THDs of different CM and DM noises mitigating approaches. The AVG-BPFC is measured as 7.3% current THD at the full rated power, but all harmonics currents, which are shown in Fig. 18, are under the limits in the industrial standard IEC 61000-3-2:2001 [30]. It can be believed that the current distortion can be improved by using some recent proposed grid current control strategies [22], [31]-[33].



(a)



(b)

Fig. 17 THDs for different BPFC topologies, (a) Grid voltage, and (b) Grid current.

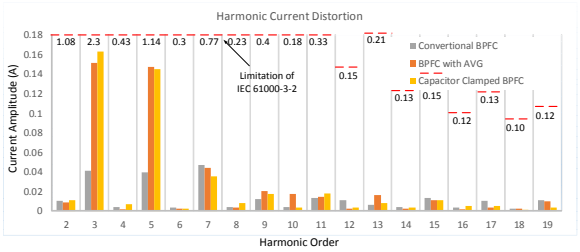


Fig. 18 Measured current harmonics.

VII. Conclusions

The paper has presented a proposed topology of bridgeless PFC using Active Virtual Ground technology. The PFC guaranteed a small grid current ripple and a low high frequency leakage current. The concept is to use an additional low frequency switching circuit to reconfigure the built-in inductors of a BPFC to become a *LCL* filter, thus the grid current ripple is minimized. Furthermore, since the filtering capacitor connects in between the DC bus and one of the grid terminals by using the proposed AVG circuit, the high frequency common mode voltage is minimized. The switching states and the steady-state characteristics of the proposed topology were explained in details. A 120 V, 60 Hz, 300 W prototype has been built in order to verify the concept. The performance of the AVG-BPFC was demonstrated and compared to conventional BPFCs by experimental results. There is good agreement between theoretical analysis and experimental results.

Appendix

A. Derivation of (2)

The duty ratio of a boost converter with a time varying input voltage can be defined as,

$$D(t) = 1 - \frac{v_C(t)}{V_{DC}} \tag{A1}$$

By using (A1) and (1), (2) can be obtained.

B. Derivation of (3)

The inductor charging characteristic is defined as,

$$v_{LC} = L_X \frac{di_{LC}}{dt} \tag{A2}$$

Assume that the switching frequency is much higher than the line frequency, i.e. $f_{sw} > 1000 \cdot f$. When the main switch is turned-on, the equivalent circuit is in Fig. 4 (a), the current is charging up linearly, thus (A2) can be changed as,

$$v_{LC} = L_X \frac{\Delta i_{LC}}{T_{ON}} \tag{A3}$$

where T_{ON} is the turn-on period in a switching cycle.

By using duty ratio D and switching frequency f_{sw} to replace T_{ON} in (A3), the converter-side current ripple can be found,

$$\Delta i_{LC}(t) = \frac{v_C(t)D(t)}{L_X f_{sw}} \tag{A4}$$

It shows that the current ripple size is time varying in a line cycle. And by putting (1) and (2) into (A4), (3) can be obtained.

C. Derivation of (4)

The capacitor voltage ripple peak to peak value is defined as,

$$\Delta v_C = v_{C,max} - v_{C,min} = \frac{1}{C_{AB}} \int_0^{T_S/2} i_C(t)dt \qquad \text{(A5)}$$

where i_C is the current of AVG capacitor, and T_S is the switching period.

The capacitor voltage ripple is basically contributed by the converter-side inductor current and it is a triangular waveform, thus (A5) can be modified with the triangle area equation.

$$\Delta v_C = \frac{T_S \cdot \Delta i_{LC}}{8C_{AB}} \qquad \text{(A6)}$$

By putting (A4) into (A6)

$$\Delta v_C(t) = \frac{v_C(t)D(t)}{8C_{AB}L_X f_{sw}^2} \qquad \text{(A7)}$$

It shows that the voltage ripple size is time varying in a line cycle. And by putting (1) and (2) into (A7), (4) can be obtained.

D. Derivation of (5)

The grid current ripple peak to peak value is defined as,

$$\Delta i_G = i_{G,max} - i_{G,min} = \frac{1}{L_X} \int_0^{T_S/2} v_{LG}(t)dt \qquad \text{(A8)}$$

where v_{LG} is the grid inductor voltage.

The grid current ripple is basically contributed by the AVG capacitor voltage and it is close to a sinusoidal waveform, thus (A8) can be modified as,

$$\Delta i_G = \frac{1}{L} \frac{\Delta v_C}{2} \int_0^{T_S/2} \sin 2\pi f_{sw} t \, dt \qquad \text{(A9)}$$

$$\Delta i_G(t) = \frac{\Delta v_C(t)}{2\pi L_X f_{sw}} \qquad \text{(A10)}$$

It shows that the current ripple size is time varying in a line cycle. And by putting (4) into (A10), (5) can be obtained.

E. Discussion of HF Filter Response

The built-in TI HF filter, which is shown in Fig. 16, is using a two-stage HF filter. From DM performance point of view, the HF filter is a high-order filter, the equivalent circuit with measured values are shown in Fig. 19 (a). The transfer function of the filter is,

$$G_{AVG}(\mathrm{s}) = \frac{-i_G(\mathrm{s})}{u_{S1/S2}(\mathrm{s})} = \frac{-1}{L_c L_f L_{lk} C_1 C_2 \mathrm{s}^5 + C_2 L_{lk}(L_f + L_c)\mathrm{s}^3 + C_1 L_c (L_1 + L_f)\mathrm{s}^3 + (L_1 + L_f + L_c)s} \qquad \text{(A11)}$$

However, the AVG circuit is a single stage third-order *LCL* filter which is integrated into the converter, the equivalent circuit with measured values are shown in Fig. 19 (b), and the transfer function is in (9). Fig. 20 shows the frequency response of two filter configurations. It shows that the filtering performance are quite similar, the crossover frequencies are both at 3.3 krad/s (or 525 Hz). Thus grid current ripple amplitude of the BPFC with the HF filter is similar to that of the AVG circuit in Fig. 15 experimental results.

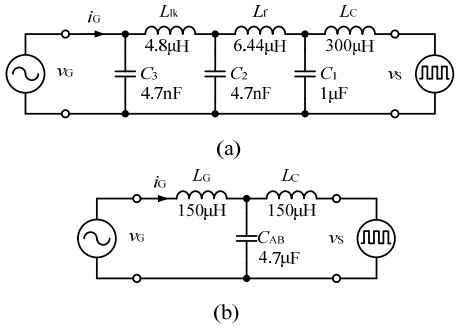


Fig. 19 Filter structures, (a) HF filter in conventional BPFC, and (b) AVG filter.

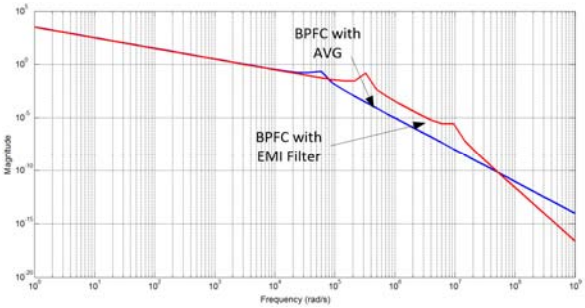


Fig. 20 Filter performance in the DM circuit.

F. Discussion of Capacitor-Clamped Circuit

By comparing the performance of a BPFC with AVG and capacitor-clamped circuits, the capacitor-clamped circuit gives slightly higher measured efficiency (94.2% and 93.5% for the capacitor-clamped and the AVG circuits, respectively) and higher attenuation of the CM voltage and, but it consists of large current ripple in the grid current which are shown in the experimental results in Fig. 15. The steady-state characteristics are studied in this section. Fig. 21 shows the positive half cycle HF equivalent circuit of the BFFC with capacitor-clamped circuit which is in Fig. 13 (b). The capacitors C_A and C_B are in parallel in the structure to clamp the CM voltage, V_{CM}, and they share the same HF DM current. In the fact that, the HF DM current path of C_B is in series of the grid source, thus the ripple of grid current is the same as the current go through C_B. In principle, the grid current ripple is half of the inductor current ripple Δi_{LC}. Thus, the capacitor-clamped circuit consists of larger current ripple in the grid current comparing to AVG circuit. And it is the disadvantage of the capacitor-clamped circuit.

The CM voltage is similar to the AVG model in (6), since two capacitors are in parallel, the equation is,

$$\Delta v_{CM}(t) = \frac{(V_{DC} - V_G \sin \omega t) V_G \sin \omega t}{8V_{DC}(C_A + C_B + C_{CM})L_X f_{sw}^2} \qquad \text{(A12)}$$

Similarly, the HF leakage current can be obtained by,

$$\Delta i_{HFCM}(t) = \frac{C_{CM}}{C_A + C_B + C_{CM}} \Delta i_{LC}(t). \qquad \text{(A13)}$$

By comparing the equations (6) and (A12), and, (7) and (A13), besides, assuming $C_A = C_B = C_{AB}$, the CM voltage and leakage current of capacitor-clamped circuit is half of the AVG circuit. However, the advantage is not significant since both systems are within the leakage current limit. And the CM voltage mitigating capability of the AVG circuit can be simply increased the value of AVG capacitor, C_{AB}. But it is not easy to reduce the grid current ripple of capacitor-clamped circuit since it requires a front stage HF filter or bulky boost inductors.

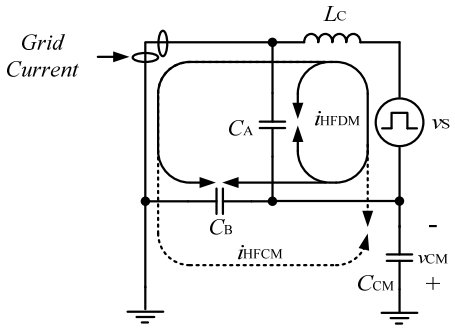


Fig. 21 HF equivalent circuit of a BPFC with capacitor-clamped circuit.

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