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Active Virtual Ground - Single Phase Transformerless Grid-Connected Voltage Source Inverter Topology

River T. H. Li, † Carl N. M. Ho and * Eric X. Chen

Abstract — An efficient single-phase Transformerless grid-connected voltage source inverter (VSI) topology by using a proposed Active Virtual Ground (AVG) technique is presented. With the AVG, the conventional output *L* filter can be reconfigured to *LCL* structure without adding additional inductor. High frequency differential mode (DM) current ripple can be significantly suppressed comparing to the available single-phase grid-connected inverter topologies. Additionally, strong attenuation to the high frequency common mode (CM) current is achieved. It is particularly important for some applications such as photovoltaic (PV) and motor drives. High efficiency can be achieved due to fewer components involved in the conduction loss. Cost of the magnetic device can be reduced since the required inductance of the filter becomes smaller. Performance of the proposed inverter has been evaluated analytically. Experimental verification is performed on a 1kW, 400V input, and 110V/60Hz output prototype.

Index tems—inverters; leakage current; common mode current; differential mode current

I. INTRODUCTION

Nowadays, Direct Current (DC) energy sources and storage elements, such as photovoltaic (PV) and battery cells, become essential in the modern power systems [1]-[2]. In order to feed DC energy to alternative current (AC) grid network, a grid-connected power electronics Voltage Source Inverter (VSI) is generally used as an interface [3]. It converts DC voltage to AC voltage and delivers the energy from the DC sources to the AC grid. The most well-known topology is the non-isolated full bridge inverter. It has a simple structure and low semiconductor losses as only two semiconductors conduct at any the time [4]. However, a simple grid-connected full bridge VSI has to use bipolar switching scheme (2-Level switching scheme), otherwise, using unipolar switching scheme (3-Level switching scheme) will induce a high frequency (HF) Common-Mode (CM) voltage to AC grid. Therefore, a lot of researches have been studying the issue [5]-[8]. Practically, the CM voltage generates a high-frequency leakage current at ground terminal in a grid network which can trigger circuit breakers to shut down the whole network. Besides, DC sources such as PV and battery cells are sensitive to CM voltage which will reduce their life time and degrade their performance [9]. Using a line-frequency transformer as an isolating element to break the leakage current path between grid network and system is a conventional and the most straight-forward method to avoid the CM voltage problems. But the transformer is bulky, expensive and high loss. This solution is not well preferred nowadays. Tranformerless VSI topologies with unipolar modulation are more preferred. But high CM current is a typical problem. In order to protect equipment and human, there are some industrial standards which limit the leakage current to a certain level, such as 300 mA [10], for commercial power electronics transformerless inverter.

For grid connected applications, many manufacturers and researchers have proposed various methods to get rid of the leakage current problems with a simple transformerless full bridge inverter. The conventional method is to use the bipolar switching scheme (2-level switching

scheme) [3], [11], however, the method leads to large current ripple at the output current and a high inductance value output inductor is required. Besides, all anti-parallel diodes in the inverter have to be low in reverse recovery loss since they all are in HF commutation loops. Using MOSFET is not a good option due to its poor body diode [12]. IGBT can be used but the current tail causes relatively high turn-off loss [13]. In order to achieve the following features, several VSI topologies has been proposed in the last decade.

1) providing unipolar switching to reduce the inductances of output filter,

2) utilizing fast commutation cells, a MOSFET and an individual fast reverse recovery diode, e.g. SiC Schottky diode, to reduce switching losses of semiconductors, and

3) suppressing leakage current to satisfy the industrial standards,

Firstly, H5 topology was successfully proposed to solve the CM voltage issues and utilized in commercial products [14]. The topology includes an additional power semiconductor switch, which is connected in series of the DC source and the full bridge inverter. Switching actions of the additional power switch is synchronized with the main HF switches in the full bridge inverter. As a result, the additional power switch breaks the leakage current path when the current is circulating in the main semiconductor switches during the freewheeling states. However, the additional switch has to be full voltage and current rated and it conducts the rated current of the inverter. It slightly reduces the overall system efficiency due the conduction loss on the additional switch. Secondly, HERIC topology is another topology which was successfully proposed and adopted by industry [15]. The topology includes an additional path in parallel with the full bridge inverter. HERIC topology successfully disconnects the input DC source from the output AC grid network during the freewheeling state by conducting the additional path and turning-off the four switches in the full bridge inverter. As a result, HF CM voltage can be avoided theoretically. But it requires two more full voltage and current rated HF power

semiconductor switches, e.g. IGBTs, to form a bidirectional blocking switch and it increases the component cost. Other topologies have been proposed to solve the same problems, such as hybrid frequency phase legs [16], H6-Type configuration [17] - [18] and Neutral Point Clamped (NPC) type [19]. In principle, they are all based on the H5 and the HERIC concepts, adding semiconductors to break or to bypass the leakage current path in the circuit. But they require adding further more semiconductor devices. Thirdly, Virtual Ground (VG) technology has been proposed for PV systems to solve the common mode (CM) voltage issues by using a three-phase three-wire inverter with controlling a potential difference of its mid-point of DC input capacitors and an unconnected neutral terminal to be almost zero voltage [20] - [21]. This method can effectively reduce the leakage current for three phase inverters. A similar approach has been proposed for single phase inverters that uses two capacitors to return HF components to the input DC side of the full bridge inverter [9], it is namely capacitor-center-tapped (CCT) technique. CCT technique can minimize the CM voltage, but it still feeds the HF DM current to the grid. A bulky inductor for filtering will be required. Apart from mentioned three methods, connecting the neutral terminal to the DC input, such as connecting to the middle point [22], [23] and the negative point [24], [25], can also suppress the leakage current. However, they require higher voltage and current rating semiconductor devices since the topologies work as a half bridge inverter or cascading buck-boost converters. Higher semiconductor cost and switching losses are the drawback.

A transformerless grid-connected inverter associated with Active Virtual Ground (AVG) topology is proposed in this paper to mitigate the HF CM voltage and reduce the HF DM current ripple concurrently. Two bidirectional blocking semiconductors and a capacitor form the AVG circuit which is connecting to the line terminal, the neutral terminal and a terminal of the input DC link. Fig. 1 shows the configuration and connections of the system. The circuit always keeps one of the grid terminals connecting to the input DC link through the AVG capacitor, C_1. From

HF equivalent circuit point of view, the AVG capacitor is a low impedance element and the DC link seems always connecting to the network ground though the capacitor. Therefore, the technique is namely Active Virtual Ground. This inverter topology has above three mentioned features. Additionally, it provides the following advantages.

1) The output filter is a *LCL* filter but without additional grid side inductor. The output inductor of switching legs takes different roles, inverter side inductor or grid side inductor, in different operating modes. It further reduces the inductance of output inductors, grid current ripple amplitude, and the cost of inductors.

2) As only high-frequency current components pass through the AVG circuit, additional conduction losses are minimized.

The paper will explain the operating principles of the proposed topology. Mathematical steady-state characteristics and a simplified design guideline of the proposed AVG circuit will be explained. Furthermore, benchmarking and variants of the proposed solution will be shown and discussed. The proposed topology is successfully demonstrated in a 1kW, 400V input, 110Vrms / 60Hz AC grid-connected VSI prototype with a digital controller. The steady-state CM voltage characteristics of the VSI are studied. Experimental results show that the proposed inverter with AVG can effectively attenuate both HF CM and DM current ripples to the grid. The theoretical prediction and experimental results are in good agreement.

II. Operating Principle

A. The proposed inverter topology and high frequency (HF) DM voltage attenuation

Fig. 1 shows the circuit schematic of the proposed inverter with the AVG circuit. S_1 – S_4, L_1, and L_2 form the ordinary single-phase full bridge inverter; S_5, S_6, and C_1 form the AVG circuit. Fig. 2 shows the gate signals of all the switches and output waveforms of the proposed inverter with unipolar switching scheme (USS) at unity power factor condition. Based on the switching

scheme, S_1 and S_2 switch alternately at grid frequency; S_3 and S_4 switch at HF, i.e. switching frequency, to shape the output current waveform as sinusoidal. Fig. 3(a) shows the operating mode for the positive half line cycle. S_1 is constantly ON; S_4 is modulated by an average current mode controller and switched at HF. It can be inspected that an equivalent HF switching voltage source, namely v_b, with magnitude changing between V_{in} and zero is applied across node *b* and the negative terminal of V_{in}. As a result, a HF differential mode (DM) voltage with magnitude equal to V_{in} applies across the output inductors, L_1 and L_2, which creates large HF DM current ripple. Therefore, large inductance is required for L_1 and L_2 to suppress the current ripple which helps to lessen the EMI problem for inverter with the ordinary USS. The proposed AVG circuit aims to suppress the DM current ripple considerably in a way of reconfiguring the output filter form *L* to *LCL* structure. It is realized by synchronizing the switching actions of S_5 and S_6 with S_2 and S_1, respectively, for the case of unity power factor operation. By conducting S_6 and opening S_5 together with the aforementioned switching pattern among S_1 – S_4, the output filter towards v_b will become an *LCL* structure in the positive half line cycle. The HF equivalent circuit of the proposed inverter with AVG for positive half line cycle is presented in Fig. 3(b). L_2, C_1, and L_1 form an *LCL* filter towards v_b. It can be observed that L_1 and L_2 act as the grid side and the inverter side inductors respectively. As a result, attenuation to the HF DM voltage, as well as the HF DM current, by the output filter is 60dB/decade. Most of the prior single-phase grid-connected inverter topologies cannot provide output *LCL* filter unless adding an additional grid side inductor per phase leg. Therefore, the HF DM voltage attenuation of the proposed inverter with AVG is 40dB/decade higher comparatively. A significant reduction on the required filter inductance is resulted for a given HF DM current ripple limit. S_5 and S_6 are bi-directional blocking switches and it can be implemented in different ways, some examples are shown in Fig. 1. Similarly, the HF equivalent circuit for the negative half line cycle is shown in Fig. 3(c). An *LCL* output filter towards the HF switching voltage source, v_a, is formed by conducting S_5

and opening S_6. L_1 becomes the inverter side inductor and L_2 acts as the grid side inductor; S_2 is constantly ON and S_3 is switched at HF to shape the output current as sinusoidal.

B. High frequency (HF) CM voltage attenuation

CM voltage is an important issue to be considered for many applications such as motor drives and PV inverters. Apart from high DM voltage attenuation capability; the proposed inverter is also providing high attenuation capability to CM voltage. As shown in Fig. 3(b) and 3(c), C_1 is connected in parallel with the leakage capacitor (C_{lk}), such as the parasitic capacitor across the ball bearing in a motor or across the frame and ground of a PV panel [9]. Therefore, the CM voltage, particular the HF component, is stabilized by C_1 and the HF CM current will be reduced accordingly. From HF signal point of view, the AVG capacitor (C_1) and the AC grid source are low impedance elements, it seems that the negative terminal of the DC input (V_{in}) connects to the earth. Thus, the circuit is namely Active Virtual Ground (AVG). The relationship between the normalized CM voltage and C_1 is given by Eqn. (1),

$$V_{hf_{CM\_normalized}} \leq \left| \frac{1}{1-0.5(n\omega_{sw})^2 L(C_{lk}+C_1)} \right|_{n=1,3,\ldots} \quad (1)$$

where ω_{sw} is angular switching frequency, by setting $L_1 = L_2 = L$, and n is the harmonic order of the HF switching voltage source v_a or v_b dependence on the polarity of the line voltage. Fig. 4 shows the graphical expression of Eqn. (1), it can be seen that the attenuation to the HF CM voltage is higher with larger C_1. As a result, the HF CM current of the proposed inverter with AVG can be adjusted by the value of C_1.

C. Grid frequency ground leakage current of full bridge inverter using USS with AVG

AVG is not affecting the Grid Frequency (GF) CM voltage of a typical full bridge (FB) with USS. Fig. 5 shows the equivalent circuits for investigating the GF CM voltage by shorting the inductors and opening the HF leg. C_{lk} is connected in parallel with the circuit that is highlighted in blue. Therefore, the total voltage across the blue paths show in Fig. 5 (a) and (b) are the GF

CM voltage across the C_{lk} in positive and negative half line cycles, $v_{CM\_GF\_AVG\_+ve}$ & $v_{CM\_GF\_AVG\_-ve}$, respectively. The CM voltage can be described as follow.

For positive half line cycle,

$$v_{CM\_GF\_AVG\_+ve} = V_{in} - \widehat{V_{ac}} \sin \omega t \tag{2}$$

where $\widehat{V_{ac}}$ is peak value of grid voltage.

For negative half line cycle,

$$v_{CM_{GF\_AVG\_-ve}} = V_{in} \tag{3}$$

Fig. 6 shows the plot of GF CM voltage of FB inverter using USS with AVG by using Eqns (2) and (3). The GF CM voltage can be expressed as follow by the observation of Fig. 6.

$$v_{CM\_GF\_AVG} = V_{in} - \frac{\widehat{V_{ac}}}{2}\left(\frac{2}{\pi} + \sin \omega t - \frac{4}{\pi}\sum_{n=2,4,\ldots}^{\infty} \frac{\cos n\omega t}{n^2-1}\right) \tag{4}$$

The first, second and third terms inside the bracket of Eqn. (4) are the DC, the fundamental and the even order harmonics terms of the GF CM voltage, respectively. Derivative of Eqn. (4) shows the GF ground leakage current,

$$i_{CM\_GF\_AVG} = -\frac{\widehat{V_{ac}} C_{lk}}{2}\left(\omega \cos \omega t + \frac{4n\omega}{\pi}\sum_{n=2,4,\ldots}^{\infty} \frac{\sin n\omega t}{n^2-1}\right) \tag{5}$$

From Eqn. (5), it can be seen that the ground leakage current is not affected by the proposed AVG circuit.

Fig. 3(d) shows the positive half line cycle HF equivalent circuit of inverter with capacitor-center-tapped (CCT). In considering the total capacitance of the filter capacitor is the same between AVG and CCT, in circuitry point of view, AVG and CCT give the same equivalent circuit towards CM current. Therefore, both solutions give the same response to the CM current.

III. SIMPLIFIED DESIGN GUIDELINE

In this section, a simplified design procedure of the AVG circuit is presented. It is basically governed by the required HF DM and HF CM current magnitudes.

A. Design of output filter capacitor (C_1)

The output filter capacitor is designed according to the HF CM current limitation. By Fig. 3(c), it can be observed that the HF CM current can be determined as follow,

$$i_{HF\_CM}(t) = i_{L1}(t) - i_{L2}(t) - i_{C1}(t) \tag{6}$$

The impedance of L_2 towards the HF CM current is much higher than C_{lk} and C_1, Δi_{L2} is assumed to zero for simplicity and without loss of generality. Therefore, C_1 and C_{lk} are connected in parallel as a current divider towards i_{L1}. The capacitance C_1 can be determined as follows,

$$\Delta i_{L1} = \Delta i_{HF\_CM} + \Delta i_{C1} \tag{7}$$

$$C_1 = C_{lk}\,\frac{\Delta i_{L1}}{\Delta i_{HF\_CM}} - C_{lk} \tag{8}$$

B. Design of output filter inductors (L_1, L_2)

The output filter inductor is designed by considering the maximum allowable HF DM current ripple. By setting the grid side HF DM current of FB with CCT equals to the one with AVG, and $L_1 = L_2 = L$,

$$\Delta i_{CCT}\,\frac{1}{2} = \Delta i_{AVG}\,\frac{1}{1+\omega_{sw}^2 L C_1} \tag{9}$$

Δi_{CCT} is the inverter side DM peak to peak current ripple magnitude of FB with CCT and USS. The grid side DM current ripple magnitude is about half of the inverter side. Δi_{AVG} and $\Delta i_{AVG}\,\frac{1}{1+\omega_{sw}^2 L C_1}$ are the inverter side and grid side DM current ripple respectively of FB with AVG and USS.

By using Eqn. (9)

$$\frac{v_{L_{CCT}}}{L_{CCT}}\Delta t\frac{1}{2}=\frac{v_{L_{AVG}}}{L}\Delta t\frac{1}{1+\omega_{sw}^2 L_{AVG}C_1} \tag{10}$$

$v_{L_{CCT}}$ and $v_{L_{AVG}}$ are the voltage across inverter side inductor of inverters with CCT and AVG. By observing Figs. 3(b) and 3(d), it can be been that the $v_{L_{CCT}}$ and $v_{L_{AVG}}$ are the same, that is $v_{L_{CCT}}=v_{L_{AVG}}$. Therefore, the required inductance of FB with AVG can be determined as follow,

$$L^2+\frac{L}{\omega_{sw}^2 C_1}-\frac{2L_{CCT}}{\omega_{sw}^2 C_1}=0 \tag{11}$$

The change in permeability against magnetic field strength of the core material should be considered after determining required inductance. But it is out of the scope of this paper.

Fig. 7 shows a design example of the required inductance by using Eqn. (11) with respect to the switching frequency for 1 kW, 110V/60Hz single-phase inverter with the AVG circuit and inverter with (CCT) [9] with 10% current ripple. The red line shows the minimum required total inductance, i.e. L_1 plus L_2, and the blue line shows the minimum required inductance for the one with CCT. For 20kHz switching frequency, the minimal total required inductance is 1.1mH for AVG and 3.1mH for CCT. This design results in a smaller inductor and lower cost. In case of keeping the same inductance between AVG and CCT at 3.1mH, the switching frequency of the inverter with AVG can be reduced to 10kHz for keeping the same HF DM ripple current magnitude. This design results in a lower switching loss. Hence, inverter with the proposed AVG circuit provides higher flexibility on the optimization of cost and efficiency.

IV. Benchmarking with Different Single-Phase Inverter Topologies and Its Variants

Table I shows a comparison of the proposed AVG topology to the other candidates which are used to solve CM voltage issue. It can be seen that the advantages of the proposed topology

are, 1) low conduction loss since only two semiconductor devices are creating losses in both power transfer and freewheeling modes as shown in the third column of Table I, 2) high utilization of output filter inductors and higher order output filter structure without adding additional inductor as shown in the fourth column. It results smaller inductance requirement for a specified DM current ripple, 3) no complicated additional control since the AVG's switches are switching at low frequency and synchronizing with the low frequency main switches. As a result, the proposed inverter can give high efficiency, small size of filter inductor and simple in implementation.

The topology shown in Fig. 1 is one of the possible configuration of the proposed AVG in single phase full-bridge inverter. By considering zero internal resistance of ideal voltage source; Fig. 8 shows the alternative configurations which give the same aforementioned electrical characteristics. The electrical performance of all these variants are the same except the DC voltage offset across C_1 since it is connecting to V_{in} minus, half V_{in}, or V_{in} plus in the three variants.

V. Simulation and Experimental Results

In order to verify the HF DM and CM currents suppression capability of the proposed inverter with AVG; simulations have been run in PLECS to study the performance between the proposed AVG and the conventional CCT topologies. The value of the output filters, including the filter inductor and capacitor, are identical for the 2 topologies in this comparison. The corresponding experimental verifications are performed and the circuit diagram of the prototype is shown in Fig. 9. Fig. 10 shows the simulation results of both inverters with AVG and CCT at different output power. The output filter design is following the guideline presented in Section III and the values of L and C are shown in Fig. 9. The windows on the left show the simulation results of inverter with AVG and the right for CCT. It can be seen that the HF current ripple of the ac grid current is less than 0.5A with AVG from 150W to 950W output. On the contrary, it is ~2.8A at

150W and ~4.5A at 440W and 950W for CCT. It verifies the high DM ripple current attenuation ability of the proposed AVG. Drain-source voltage across S_5 and S_6 are shown in Fig. 10 and it is equal to the ac grid voltage when the switch is in blocking state. Fig 11 shows the simulation results of the output filter inductor currents, i_{L1} and i_{L2}, and the CM current, i_{CM}, of the inverters with both AVG and CCT. It can be seen that the inductor current of both AVG and CCT are very similar. Therefore, it offers an opportunity to modify the existing inverter with CCT to AVG without changing the output filter inductors. The CM current of the inverter with CCT and AVG is the same as discussed in Section II A. However, with considering the forward voltage, V_f, drop across the diodes around S_5 and S_6, the diodes can be conducted unless high enough voltage, i.e. $2V_f$, has been built up across C_{lk} which leads to higher CM current. A simulation results is shown in Fig. 12 that the V_f of the diodes is 0.5V. It can be seen that the CM current becomes higher for roughly 3 times. In order to lessen this issue, S_5 and S_6 can be implemented by back-to-back connected MOSFETs which has zero V_f.

A 1kW, 400V DC input and 110Vrms/60Hz AC output full-bridge inverter with the proposed AVG circuit hardware prototype has been built for experimental verification. The inverter is switching with unipolar modulation at 20kHz. The CCT counterpart is also tested on the same prototype for benchmarking. The circuit diagram and key components of the prototype are shown in Fig. 9. Due to the better switching performance of MOSFETs and anti-parallel diode of IGBTs; MOSFETs are selected for S_3 and S_4 and IGBTs are selected for S_1 and S_2. IGBTs can also be used in S_3 and S_4 which give lower cost but higher conduction and switching losses in general. The prototype was tested with 400V DC input and 110Vrms AC grid with both AVG and CCT configurations. Fig. 13 shows the experimental steady state waveforms of both candidates at 150W, 440W, and 950W output. It can be seen that the HF DM mode current ripple of the inverter with AVG is much smaller than the one with CCT from light load to heavy load. The HF current ripple of the ac grid current is less than 1.0A with AVG from 150W to

950W output. On the contrary, it is ~2.8A at 150W and ~6.0A at 440W and 950W for CCT. The experimental results are matching with the simulation results which show in Fig. 10. Fig. 14 shows the dynamic power change waveforms of the proposed inverter with AVG between 150W and 950W. It can be seen that the power is changing smoothly and the drain-source voltage across S_5 and S_6 is not subject to the power change as explained. Fig. 15 shows the inductor currents of L_1 and L_2 and the CM current across C_{lk}. Similar to the simulation results, the inductor acts as an inverter side inductor where the current ripple is larger; the current ripple is smaller when the inductor acts as a grid side inductor. The HF CM current is around 130mA to 170mA RMS, there is ~50mA measurement offset, where the C_{lk} is 220nF. The HF CM current for AVG and CCT under the same conditions is around 200mA and 180mA RMS at 950W output. It proves that the AVG topology can effectively suppress the CM currents. Apart from the low frequency distortion in the results of inverter with CCT, the inductor current waveforms are very similar between inverter with AVG and with CCT. There is no observable difference in the current ripple magnitude in both positive and negative half line cycles. It is in-line with the simulation results and no change on the inductor is required for changing the topology from CCT to AVG. A little higher in CM current in the case with AVG, it is due to the voltage drop across the diodes around S_5 and S_6 which is simulated and shown in Fig. 12. Fig. 16 shows the measured efficiency and THD of the proposed inverter with AVG, the maximum efficiency is around 96.4% at 250W, it reaches 95.3% efficiency at rated power 950W. According to the current waveforms in Fig. 15 and the KCL circuit theory, there is a 8A peak-to-peak HF ripple current going through the AVG circuit and its RMS value is about 1.4A. The overall semiconductor loss of the AVG circuit is ~3W. It is not significant for a 950W inverter. Output current THD is smaller in higher output power, it is mainly due to the inductor current is in discontinuous conduction mode (DCM) at light load. The THD equals to 4.9% at 950W output. Fig. 17 shows the photos of the prototype, the dimension is 24.0cm × 14.4cm × 8.2cm. All

semiconductor switches are controlled by a DSP. Two output filter inductors are designed as identical, and each inductor connects to one individual current sensor. This is because the operating modes of the inductors are changed in every half line cycle; it requires individual inductor current feedback signals to control the semiconductor switches for shaping the output current.

The prototype demonstrated the concept and functionalities of the proposed AVG circuit applying to a grid-connected full bridge inverter. By using the same concept and the suggested design guideline, the rated power of inverter could be scaled up (e.g. 5 kW) or down (e.g. 300W) for different applications. The AVG circuit only has semiconductor conduction losses which is created by the HF ripple current. As long as the same ripple current amplitude, the loss of the AVG circuit will be quite consistent in the range of the rated power.

VI. CONCLUSIONS

The proposed single-phase full-bridge grid-connected inverter with Active Virtual Ground (AVG) circuit htas been presented in this paper. The proposed topology provided a high attenuation ability on both HF Differential Mode current and HF Common Mode current. The key merit is to change the output filter from *L* (1st order) to *LCL* (3rd order) structure by using additional low frequency switching semiconductors instead of adding additional grid inductors. Thus, the grid current ripple amplitude or the required inductance can be reduced comparing to the conventional topologies. Besides one of the grid terminals (Neutral or Line) is always connected to the DC link terminal with the AVG capacitor that mitigates the HF leakage current in the system. The operating principle and converter steady-state characteristics of AVG-VSI topology were studied. Besides, dynamic behaviors and simplified design guidelines of the proposed AVG-VSI topology were presented. The theoretical predictions were successfully verified by computer simulations and laboratory measurements with a good agreement.

VII. APPENDIX

Proof of Eqn. (1)

$$V_{n\omega_{sw}\_normalized} = \left| \frac{\frac{1}{jn\omega(C+C_{lk})}}{\frac{jn\omega L}{2}+\frac{1}{jn\omega(C+C_{lk})}} \right|_{n=1,3,\ldots}$$

$$V_{n\omega_{sw}\_normalized} = \left| \frac{1}{1-0.5(n\omega_{sw})^2 L(C_{lk}+C_1)} \right|_{n=1,3,\ldots} \quad (1)$$

Proof of Eqn. (4)

Fig. 6 shows the plot of GF CM voltage of FB inverter using USS with AVG by using Eqns. (2) and (3).

$$v_{CM\_GF\_AVG} = V_{in} - \frac{\widehat{V_{ac}}}{2}(sin\,\omega\,t + |sin\,\omega t|)$$

By Fourier analysis, $|sin\,\omega t| = \frac{2}{\pi} - \frac{4}{\pi}\sum_{n=2,4,\ldots}^{\infty} \frac{cos\,n\omega t}{n^2-1}$

$$v_{CM\_GF\_AVG} = V_{in} - \frac{\widehat{V_{ac}}}{2}\left(\frac{2}{\pi} + sin\,\omega\,t - \frac{4}{\pi}\sum_{n=2,4,\ldots}^{\infty} \frac{cos\,n\omega t}{n^2-1}\right) \quad (4)$$

Proof of Eqn. (8)

By Eqn. (7) $$\Delta i_{L1} = \Delta i_{HF\_CM} + \Delta i_{L2} + \Delta i_{C1} \quad (7)$$

Set $\Delta i_{L2} = 0$,

$$\Delta i_{L1} = \Delta i_{HF\_CM} + \Delta i_{C1}$$

$$\Delta i_{HF\_CM} = \Delta i_{L1} \frac{C_{lk}}{C_1+C_{lk}}$$

$$C_1 = C_{lk}\,\frac{\Delta i_{L1}}{\Delta i_{HF\_CM}} - C_{lk} \quad (8)$$

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Figure captions

Fig. 1. The proposed single-phase Transformerless full-bridge inverter with AVG topology.

Fig. 2. Switching pattern of S_1 – S_6 for unity power factor condition.

Fig. 3. Circuit diagram of (a) positive half line cycle with AVG, (b) positive half line cycle HF equivalent circuit with AVG, (c) negative half line cycle HF equivalent circuit with AVG, and (d) positive half line cycle high HF equivalent circuit with CCT.

Fig. 4. Frequency response of normalized CM voltage with different C_1.

Fig. 5. Equivalent circuits for investigating the GF CM voltage (a) positive half line cycle and (b) negative half line cycle.

Fig. 6. GF CM voltage of FB USS AVG.

Fig. 7. Minimum required output filter inductance of inverters with AVG and with CCT.

Fig. 8. Variants of the proposed inverter with AVG.

Fig. 9. Circuit diagram of the laboratory prototype and experimental set-up for inverter with AVG and CCT.

Fig. 10. Simulated steady state output current waveforms of the inverters with AVG and CCT at 150W, 440W, and 950W output.

Fig. 11. Simulated steady state output filter inductor currents and Current waveforms of the inverters with AVG and CCT at 150W, 440W, and 950W output and C_{lk} equals to 220nF.

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Fig. 14. Experimental dynamic power changes waveforms of the inverters with AVG from 150W to 950W and from 950W to 150W.

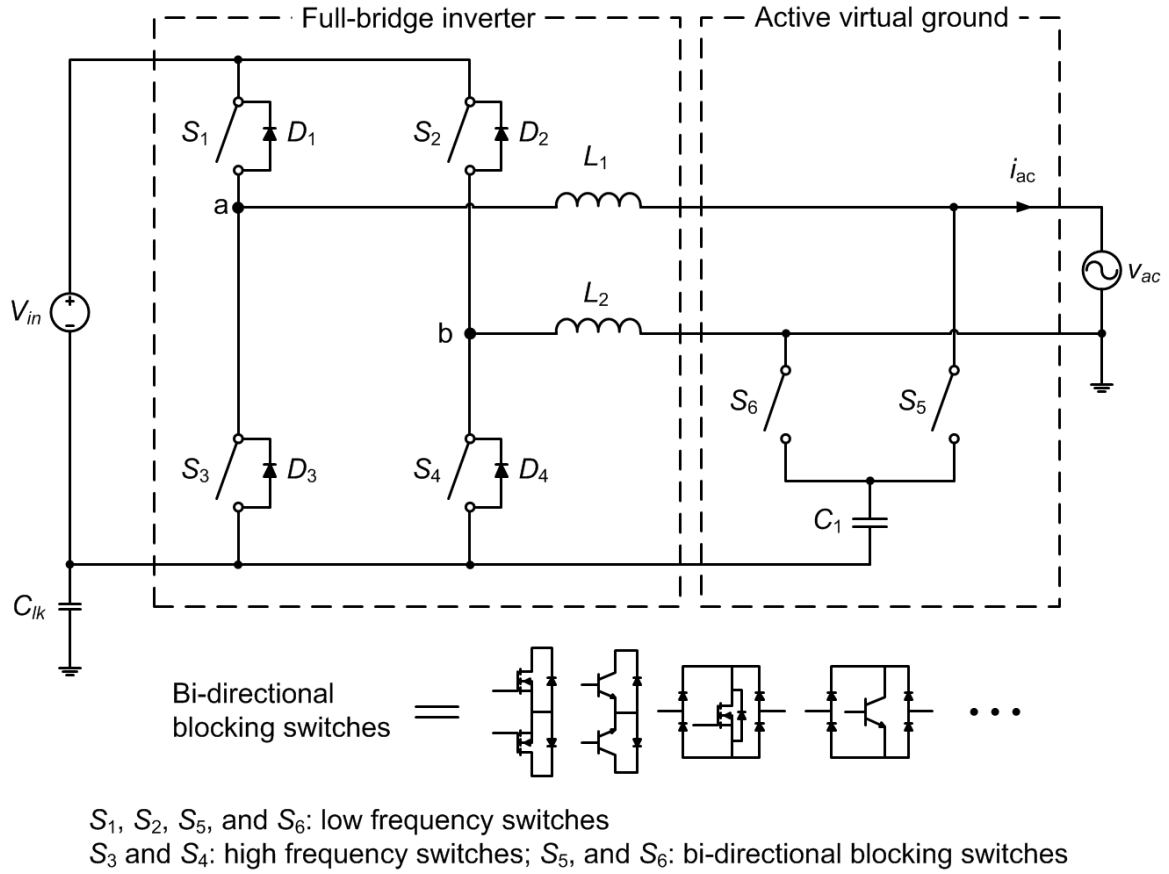
Fig. 15. Experimental steady state output filter inductor currents and CM mode current waveforms of the inverters with AVG and CCT at 150W, 440W, and 950W output and C_{lk} equals to 220nF.

Fig. 16. Measured efficiency and current THD of the prototype with AVG.

Fig. 17. Photos of the proposed inverter with AVG laboratory prototype.

Table Captions

Table I. Benchmarking of the prior single-phase grid-connected inverters.



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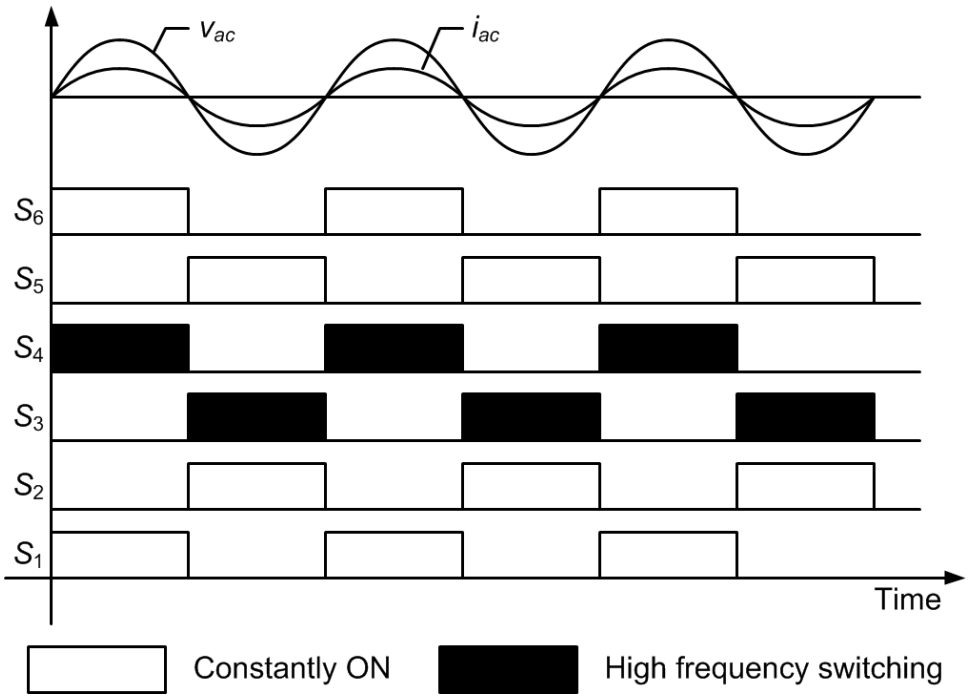

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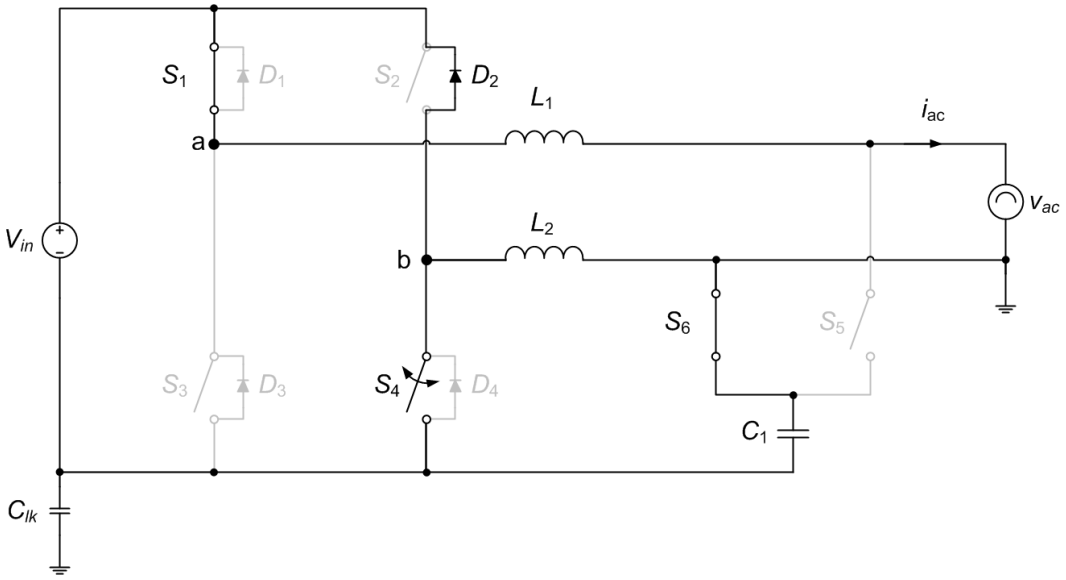
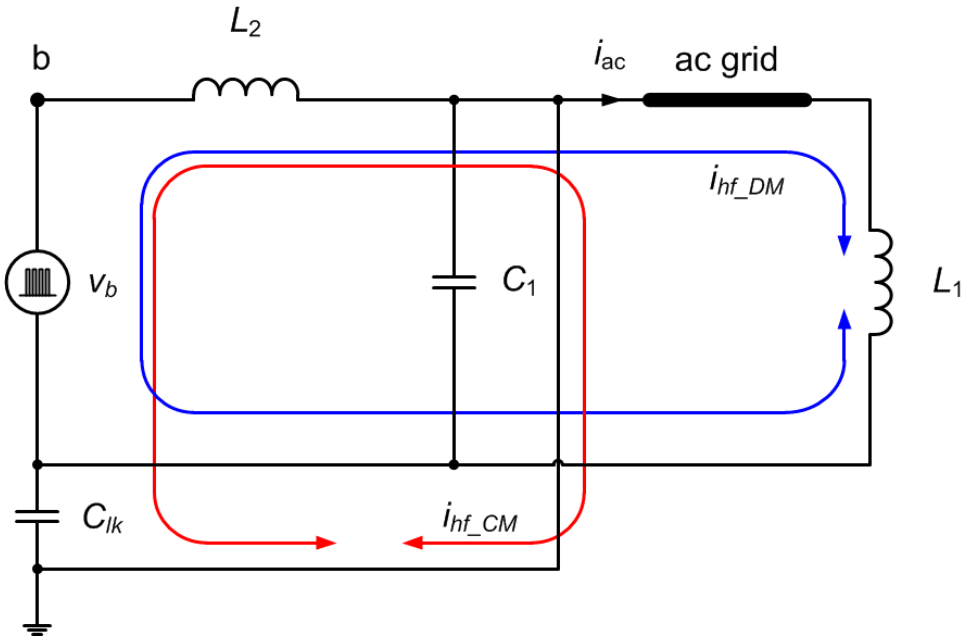
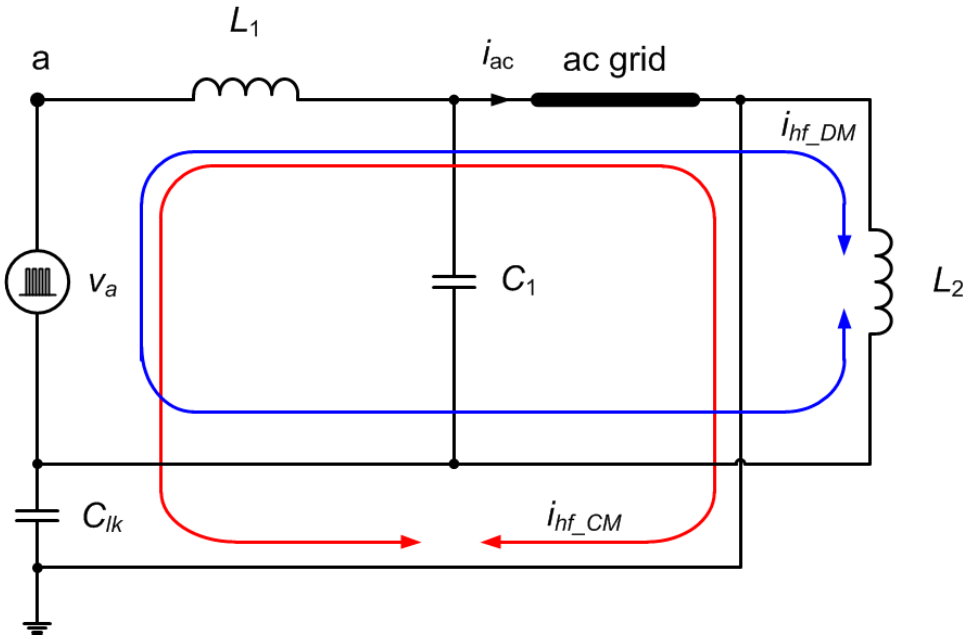

S1
D1
S2
D2
L1
iac
a
Vin
L2
vac
b
S6
S5
S3
D3
S4
D4
C1
Clk

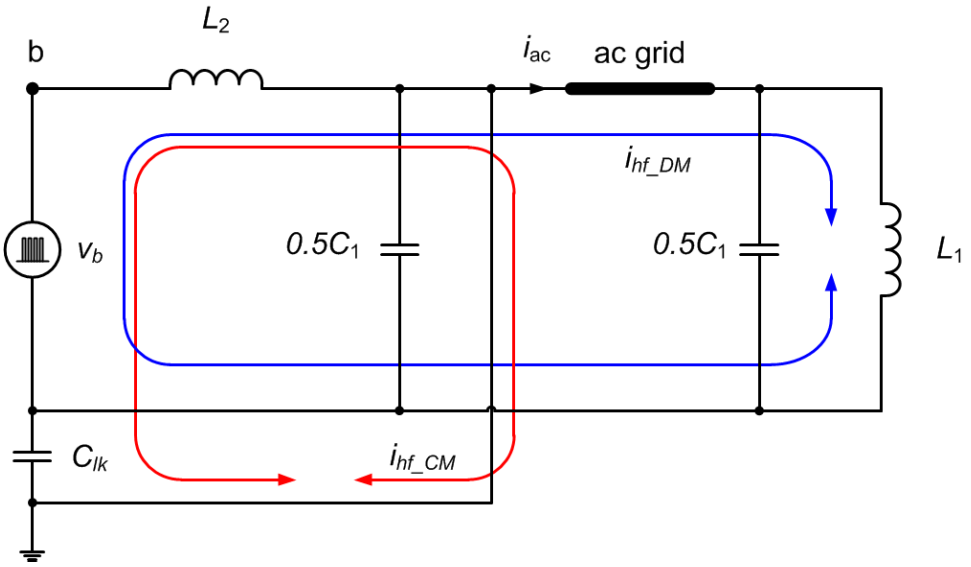
(a)


L2
b
iac
ac grid
ihf_DM
vb
C1
L1
Clk
ihf_CM

(b)



(c)



(d)

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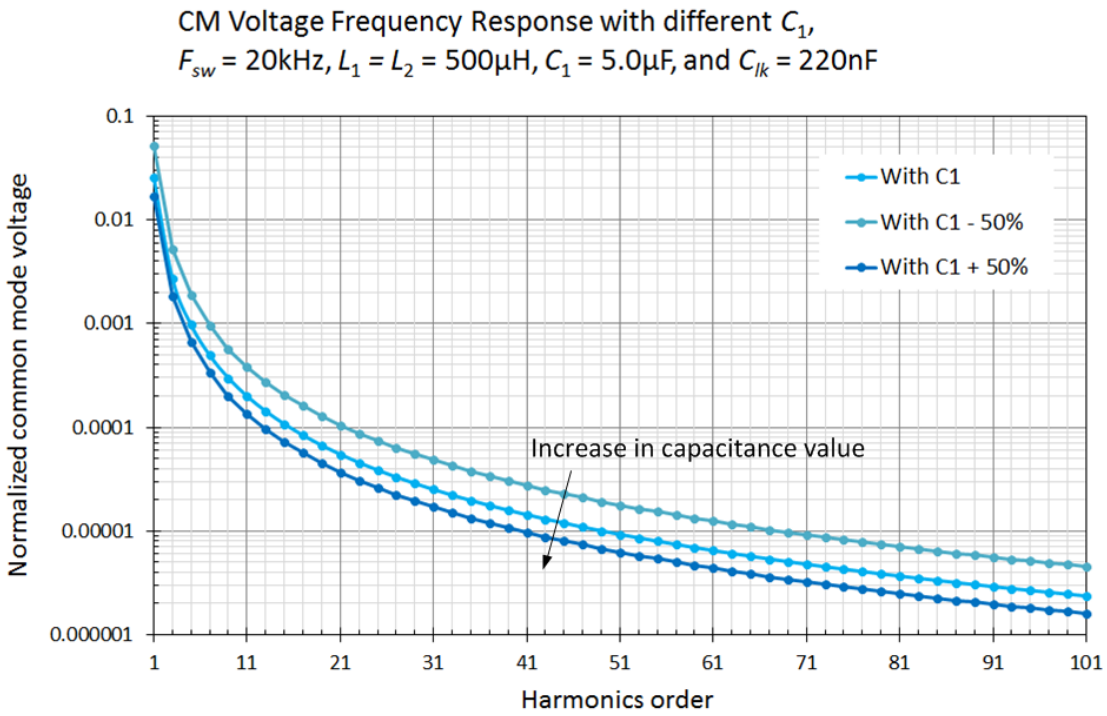

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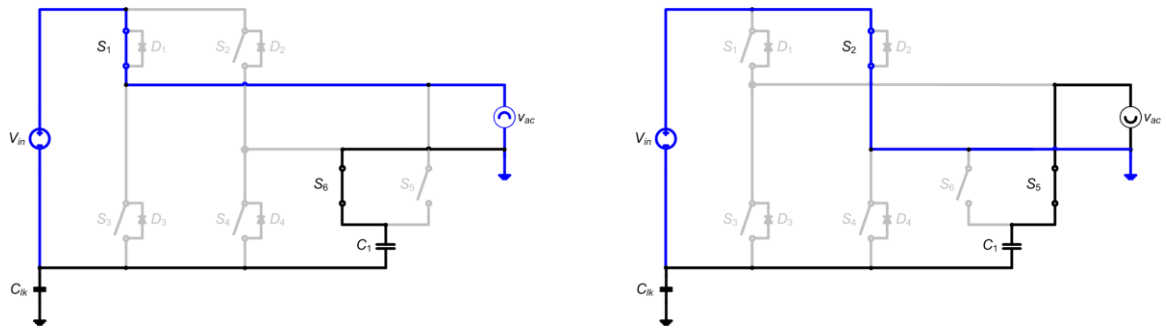

(a) (b)

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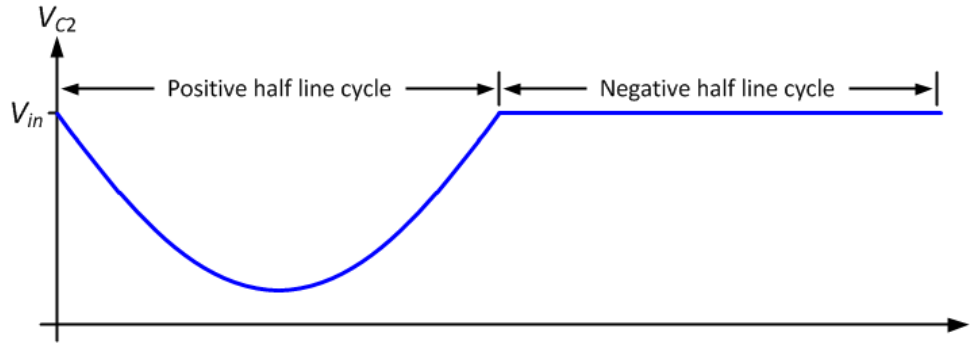

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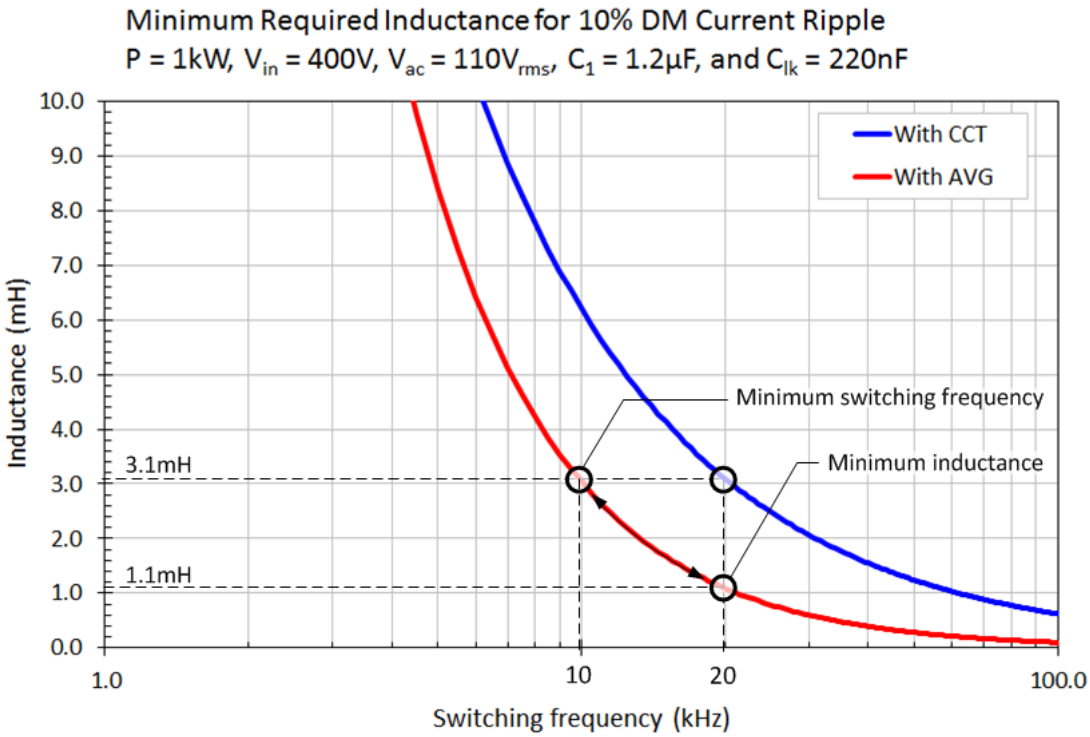

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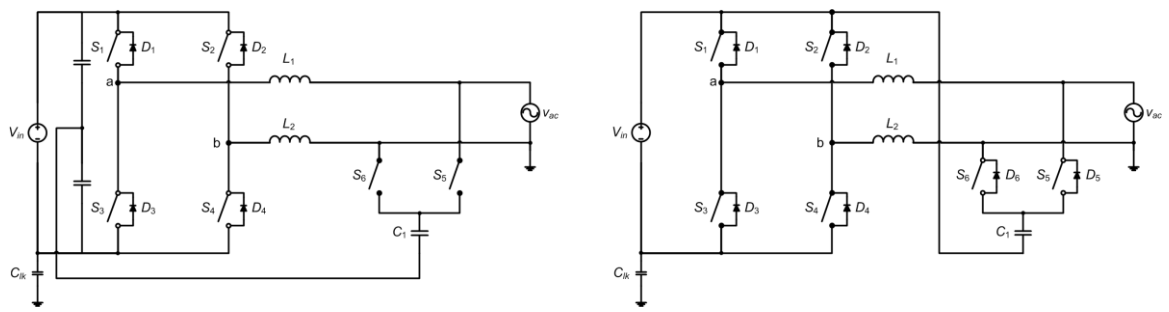
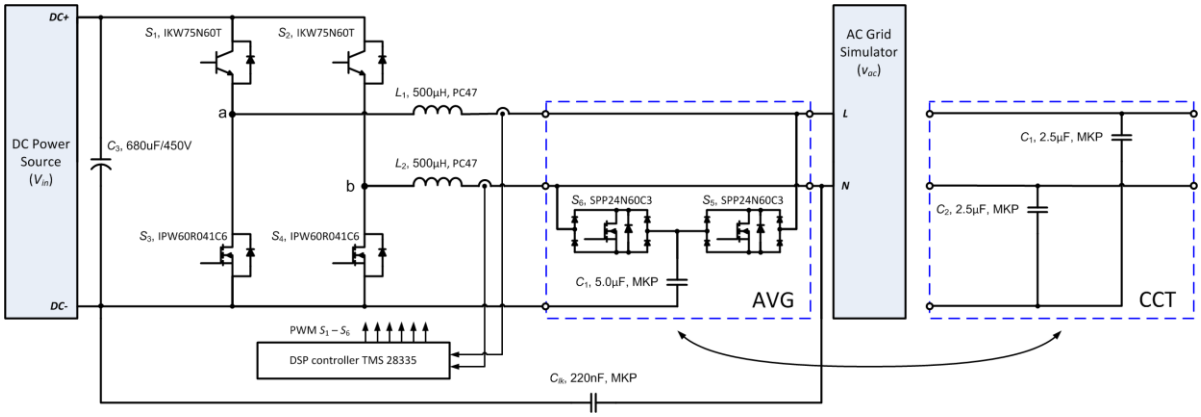


Fig. 8. Variants of the proposed inverter with AVG.



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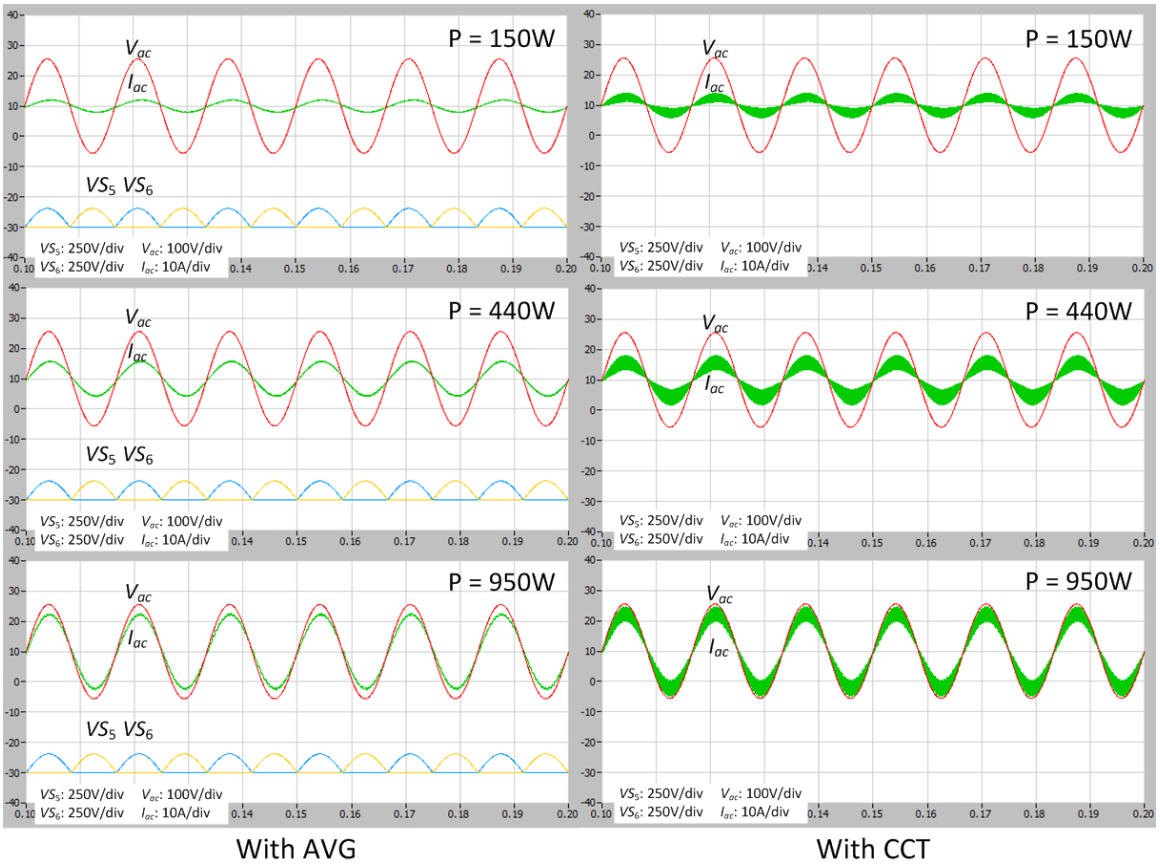

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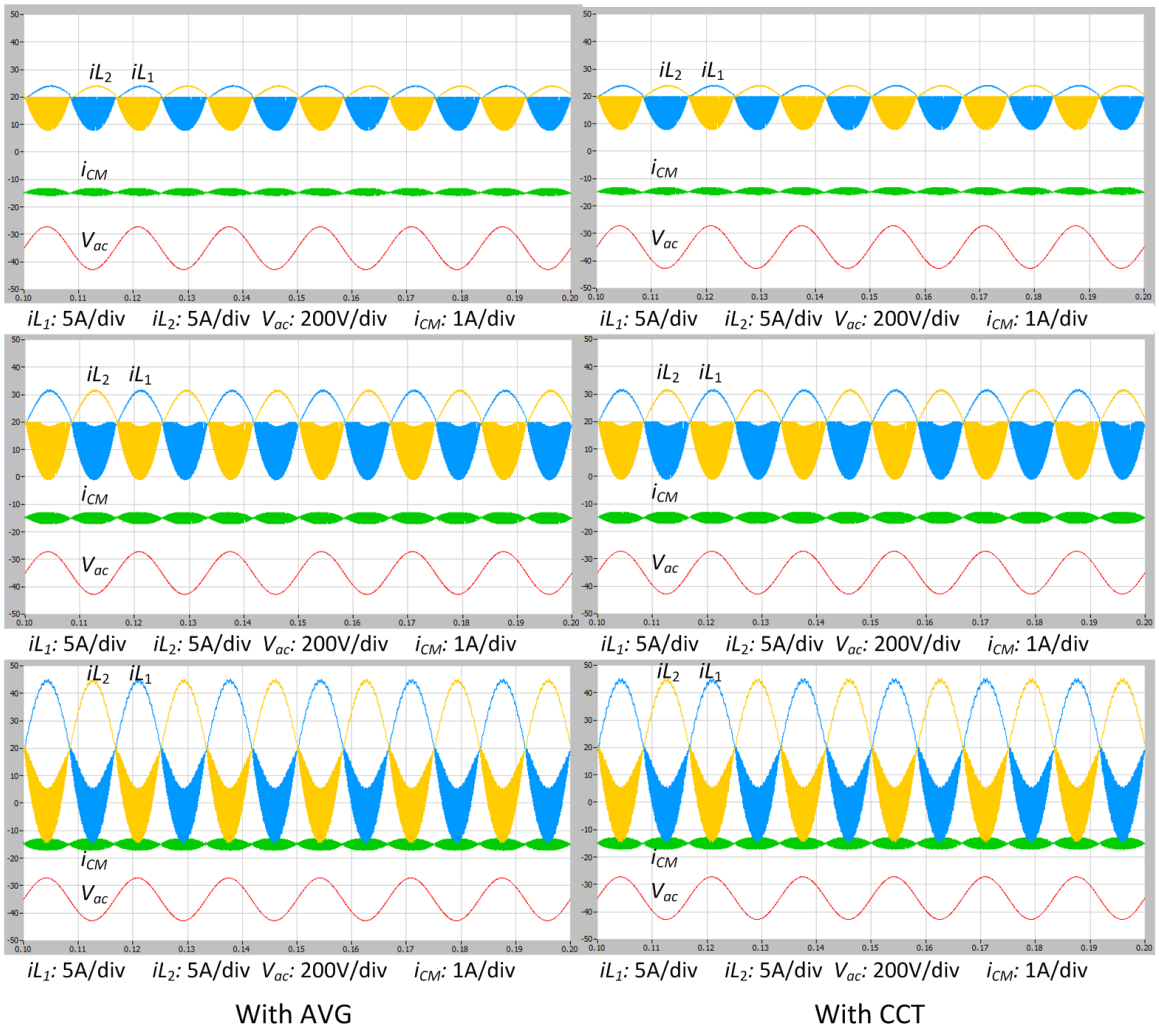

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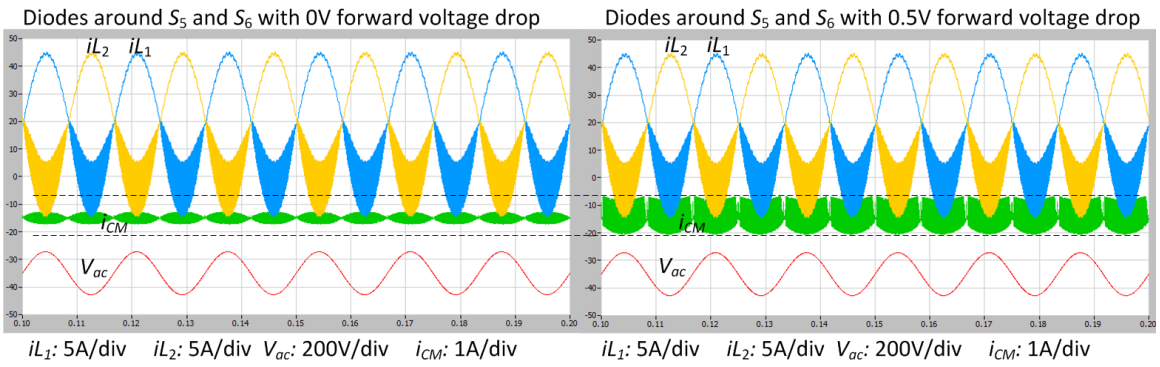

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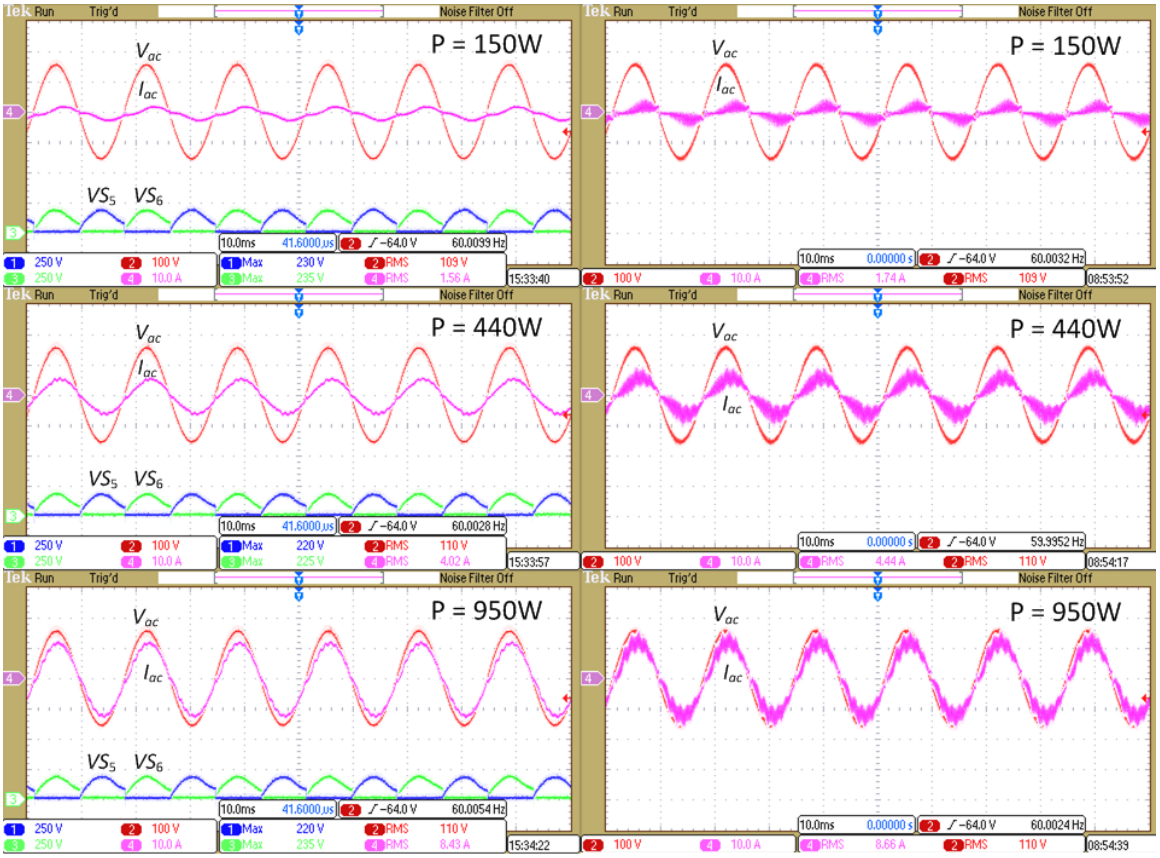

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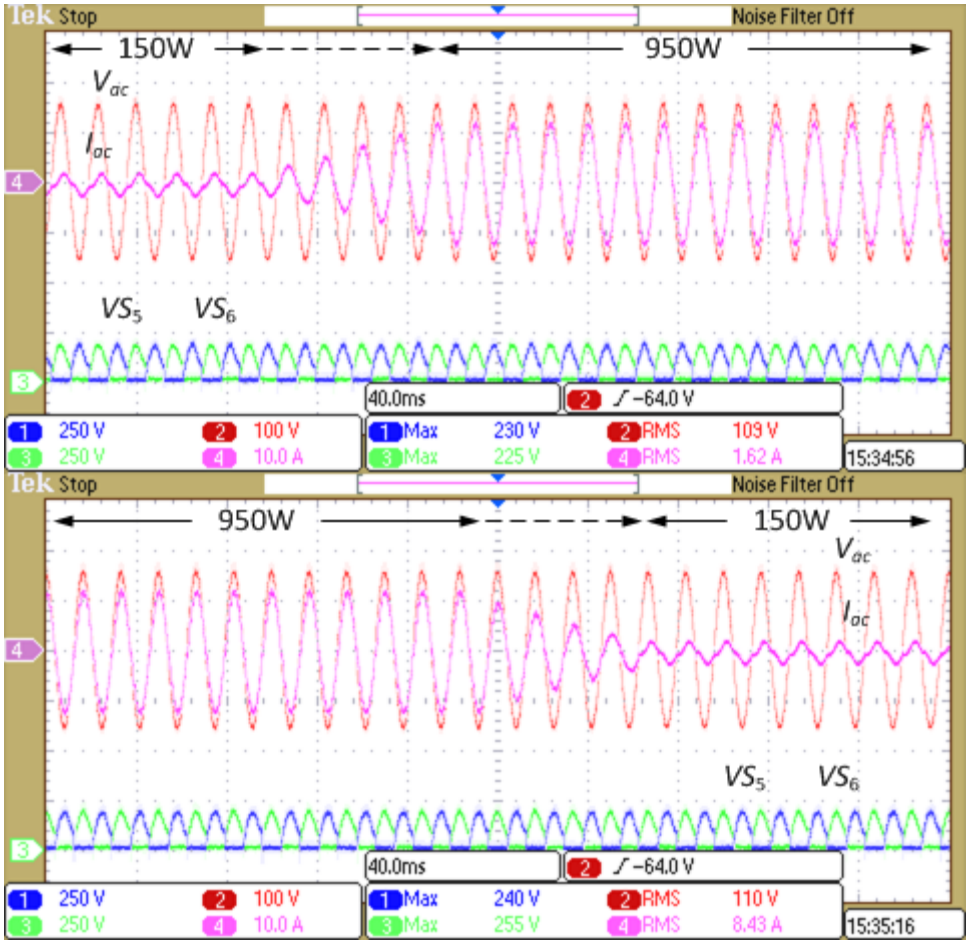

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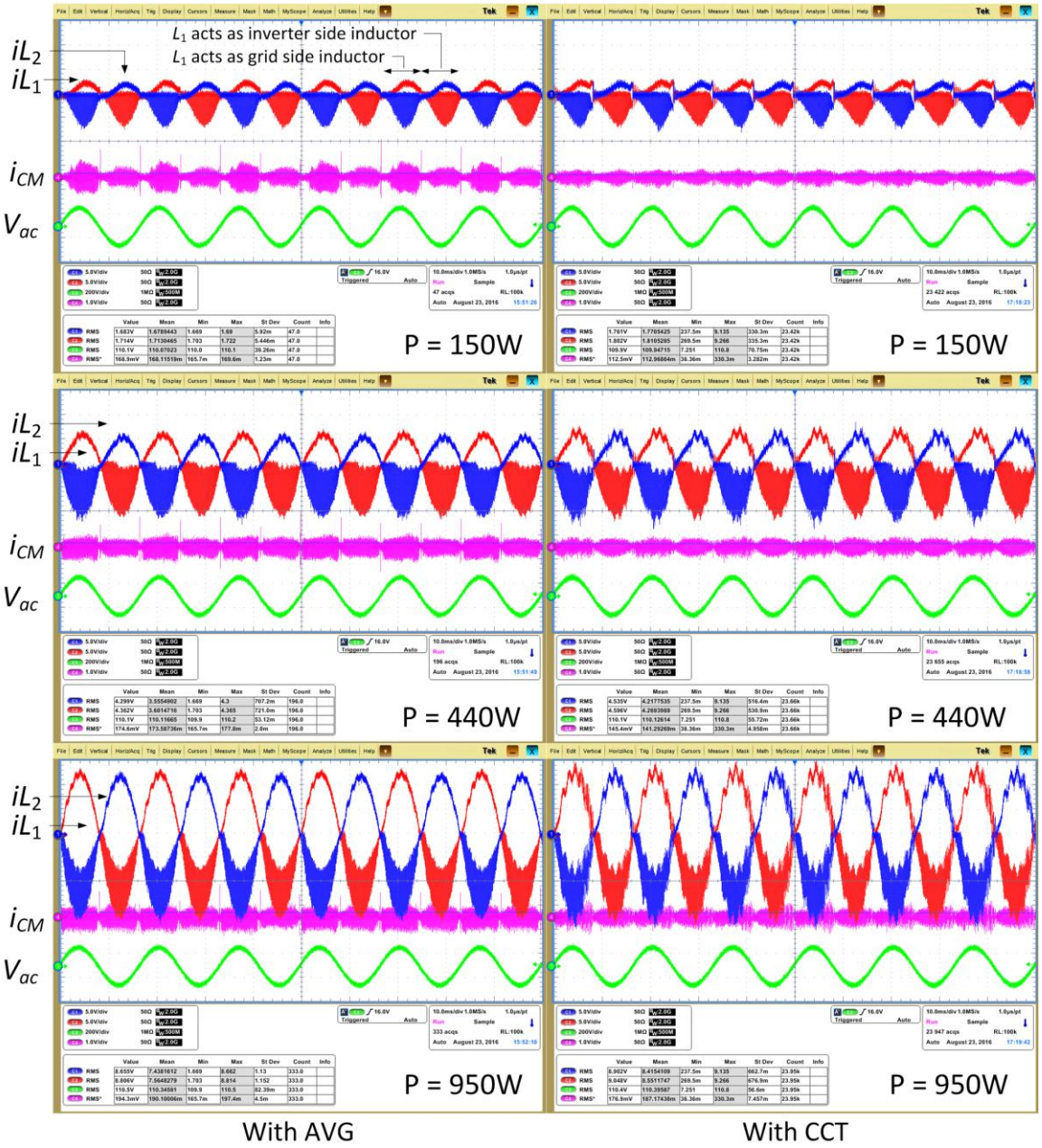

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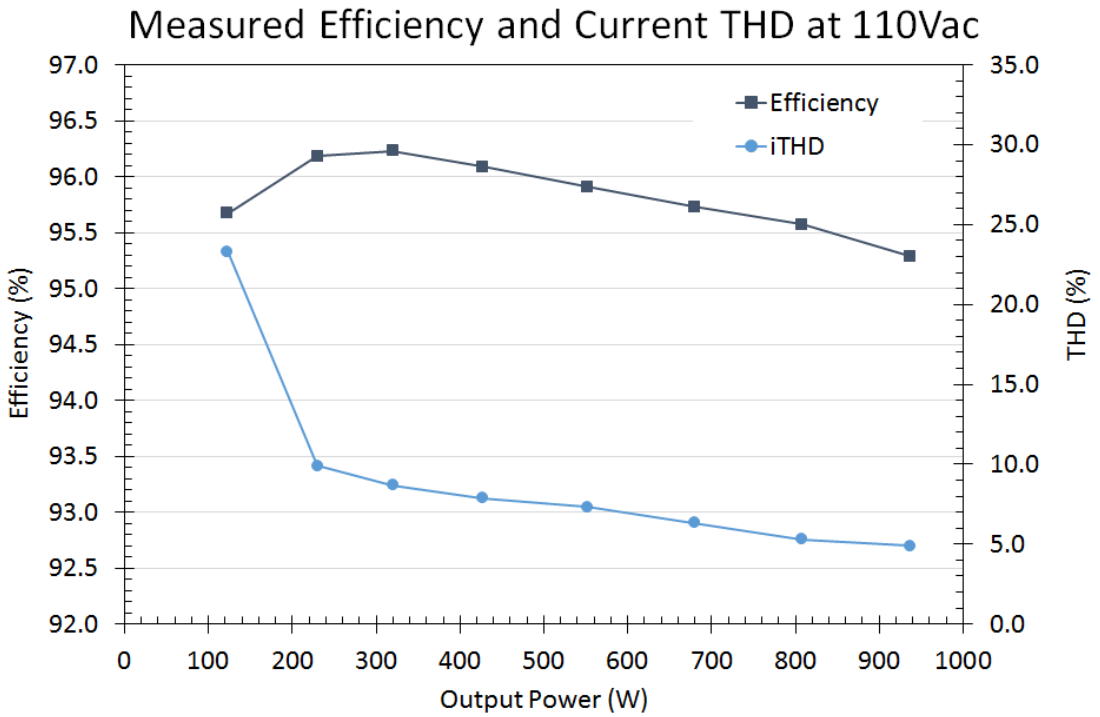

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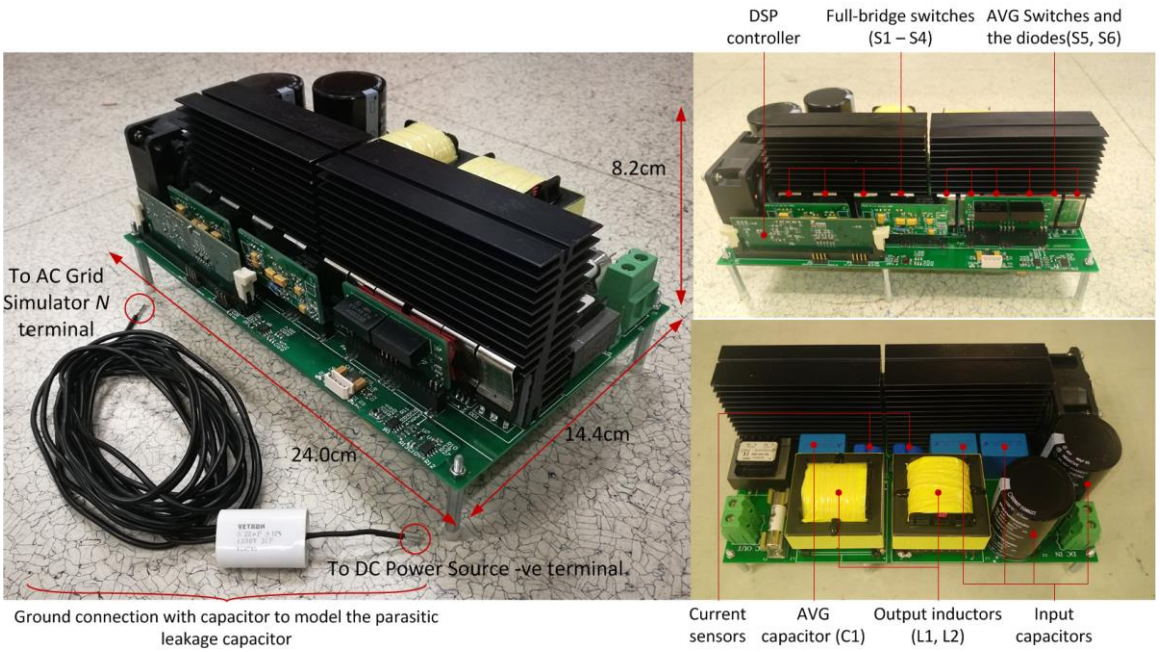

Fig. 17 Photos of the proposed inverter with AVG laboratory prototype.

Table I. Benchmarking of the prior single-phase grid-connected inverters

Inverter topology	No. of switches	No. of devices conduct in energy transfer or freewheeling states	O/P filter
HERIC [15]	6	2	*L*
Hybrid frequency phase legs [16]	4	2	*L*
H5 [14]	5	3	*L*
H6 [18]	6	4	*L*
H6 type [17]	6	transfer: 3, freewheeling: 2	*L*
Neutral wire – PV panel direct connection [22]	6	2	*L*
Neutral wire – PV panel direct connection [24]	6	transfer: 3, freewheeling: 5 (equivalent)	*L*
Neutral wire – PV panel direct connection [23]	2	2	*L*
Neutral wire – PV panel direct connection [25]	3	Positive half-line cycle: 1, negative half-line cycle: 3	*L*
NPC type [19]	6	transfer: 3, freewheeling: 2	*L*
The proposed inverter with AVG	6	2	*LCL*