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Advanced Digital Controller for Improving Input Current Quality of Integrated Active Virtual Ground-Bridgeless PFC

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Abstract- The paper presents a new digital control scheme for Active Virtual Ground-Bridgeless PFC (AVG-BPFC) which is able to obtain an optimized solution between the system efficiency and Electromagnetic Interference (EMI) performance in the PFC stage. However, a resonant characteristic is generating from the input *LCL* filter structure of the converter. In addition, there is a phase difference between two inductor currents which also leads the controller design in the AVG-BPFC to become challenging, especially on the system stability and the current quality. Thus, a triple loop control's architecture together with an integrated state machine is proposed as the control methodology of the AVG-BPFC. Under the simple control structure in the digital platform, a stable system is achieved together with a precise grid current tracking function. Such control scheme was implemented digitally on a 1.5 kW prototype. In the paper, theoretical models of the whole system were analysed and the system performance was successfully verified in both steady state and transient state conditions. The experimental results showed a good agreement with the theoretical knowledge.

Keywords— Bridgeless Power Factor Correction, Active Virtual Ground, LCL Filter, Boundary Control.

I. INTRODUCTION

Nowadays, a PFC converter is usually applied to the system front stage due to the power quality requirement. The wireless power transfer (WPT) system of Electric vehicle (EV) and hybrid electric vehicle (HEV) are the typical examples on the PFC stage application [2] - [4]. In the EV system, battery power management is very crucial as it directly links with the vehicle safety and the battery life time. Therefore many design requirements and industrial standards are needed to follow by the WPT system. Under the standard IEC 61980-1 [5] and the SAE J2954 [6], the efficiency requirement of the overall WPT system needs to be higher than 85%. In addition, the system is required to pass the CISPR 11 [7] in the EMI performance test. To fulfill efficiency standards, bridgeless PFC (BPFC) is widely preferred in the PFC stage. However, a large EMI filter is required to supress the common-mode (CM) noise generated from the BPFC system in order to achieve the industry requirement on the EMI standard. Another alternative solution is to apply a CM noise mitigation topology to solve the CM noise issue [8].

The recently proposed Active Virtual Ground-Bridgeless PFC (AVG-BPFC) topology [9] - [10], as shown in Fig. 1, can achieve the above criteria by providing both low leakage current and high energy efficiency in the PFC stage. The AVG-BPFC takes the optimized point between the conventional PFC and the BPFC. The AVG-BPFC adopts the advantage of the BPFC, which is that there is only two semiconductors conducted in the main current path in each switching action. In addition, based on the operation structure, an *LCL* filter is formed at the input side. The filter capacitor clamps the high frequency voltage ripple in the circuit parasitic capacitor, therefore the leakage current flowing back into the earth is minimized [9].

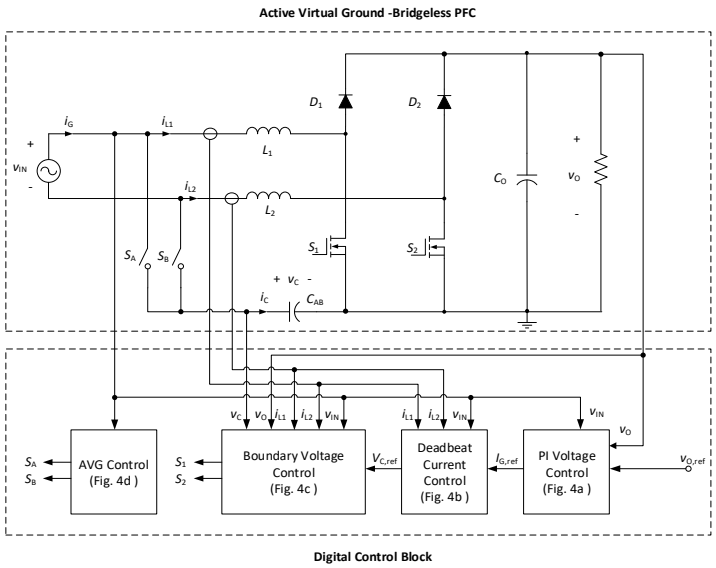


Fig. 1 The proposed control scheme in AVG-BPFC.

In the AVG-BPFC, a *LCL* input filter structure is formed. There are two key main issues that should be considered in designing the controller. They are the phase shift properties and the resonant characteristics [9]. Firstly, there is a phase difference between the converter side inductor and grid side inductor. In AVG-BPFC, it is insufficient to use a single current detection control in ensuring system stability and performance characteristics. If only the converter side inductor current is under control, the input power factor will be deteriorated due to the filter phase shift. If only the grid side inductor current is under control, an unstable current may appear in the converter side unless a further control block is added [11]. Thus, two current sensors for sensing the two filter inductor currents are needed. Secondly, the high-order filter structure exhibits a resonant characteristic in the AVG-BPFC. Thus, the design of linear control over a wide operating ranges becomes a challenge. In the PFC stage, PI control is a well-known control methodology which is in simple structure and less sensors requirement. In order to alleviate the resonant characteristic of *LCL* filter, an active damping method is generally adopted into the PI control [11] – [14]. However in the digital implementation, the sampling-and-processing delay time in digital control would restrict the control bandwidth and thereby the input power factor and the current THD are deteriorated. On the other hand, non-linear control such as hysteresis and sliding mode control are also commonly applied on the PFC state which can offer stable

performance over a wide range of operation. However, the system performance may still be distorted during the light load condition and some large signal transient conditions [15]-[16]. Therefore to maximize the system performance and to maintain the system stability under different operation conditions, a new system control scheme is required for the new operational characteristics.

An advanced control scheme is proposed in this paper to fulfill the high quality grid current and the good system stability requirement on the AVG-BPFC. In contrast to [9], 1) an high power integrated AVG-BPFC system (1.5 kW) is built instead of using the add-on circuit (300W) as shown in [9] in order to have a better circuit design and effective utilization of controller; 2) grid side inductor current control associating with the proposed non-linear control methodology instead of the converter side current control using conventional linear controller to achieve the purpose of high quality grid current. A triple loop control architecture is built in the digital controller. In the inner loop control, a fast boundary controller with second-order switching surface [16]-[20] is implemented to eliminate the filter resonance in the transfer characteristic and to control the AC voltage. The second-order boundary control is applied to the input stage of the boost-type rectifier under unipolar switching schemes with high sampling frequency. A state machine is integrated into the control loop to solve the zero crossing problem due to the discontinuous mode operation. Thus, both continuous conduction mode and discontinuous conduction mode operation are covered in the controller design and offers an accuracy switching signals. The mid-loop is a deadbeat current controller [21]-[23] which offers high quality input current to enhance the input power factor and reduces the THD. In the outer loop, a PI controller aims to regulate the system output voltage. The approach can keep the advantages of the topology of AVG-BPFC in terms of low leakage current and small magnetic components, and furtherly improve the grid current quality and the system stability. The whole system stability was analyzed with the use of the small signal modelling which demonstrated how the resonant issue in the AVG input filter can be eliminated and the improvement of the power quality. A design guideline was provided for the proposed multi-control loop system. Such integrated control is applied digitally to deal with the complicated control scheme. A 1.5 kW

AVG-BPFC prototype was implemented to verify the control scheme. Experimental results are in close agreement with theoretical predictions.

II. SYSTEM CONFIGURATION

A. Review of AVG-BPFC Topology

Compared to the traditional BPFC, two additional low-frequency-bidirectional switches, S_A and S_B, and one additional filter capacitor, C_{AB}, are added in order to the form the AVG-BPFC. The circuit structure of the AVG-BPFC [9] is symmetrical in both positive and negative line cycles. The corresponding equivalent circuit in the positive half line cycle and the negative half line cycle are shown in Fig. 2 (a) and (b) respectively. Under unipolar switching method, as shown in Fig. 3 (a), only one switch is in high-frequency switching through the system operation. In the positive cycle, as shown in Fig. 2 (a), the switch S_A and the switch S_2 are kept ON and the switch S_1 is switched at high frequency. C_{AB} is linked to the Line of AC grid, the inductor L_1 becomes the converter inductor and the inductor L_2 acts as the grid side inductor. An *LCL* filter structure is formed at the converter input. Likely, in the negative cycle, Fig. 2 (b), the switch S_B and the switch S_1 is kept ON and the switch S_2 is switched at high frequency. C_{AB} is connected to the Neutral of the ac grid and forms another *LCL* filter structure. L_1 becomes the grid inductor and L_2 acts as the converter side inductor. The converter side high frequency current is looped inside the converter through C_{AB}. Therefore less ripple current appears in the grid side inductor. The capacitor voltage and current waveform are shown in Fig. 3 (b).

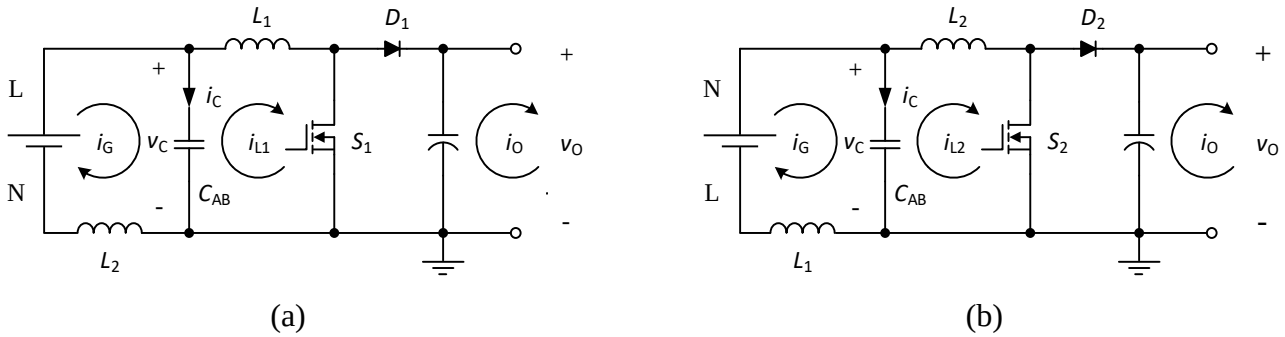
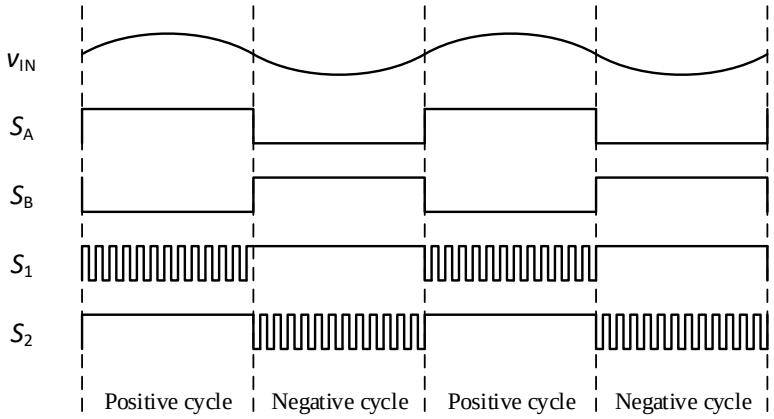
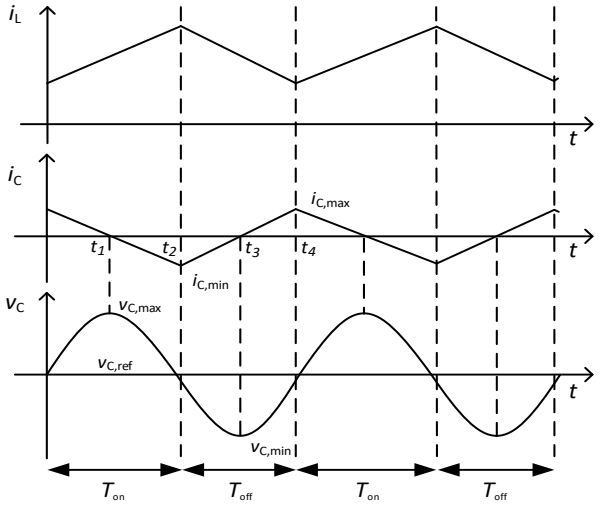


Fig. 2 Equivalent circuit of AVG-BPFC in (a) positive line cycle and (b) negative line cycle.



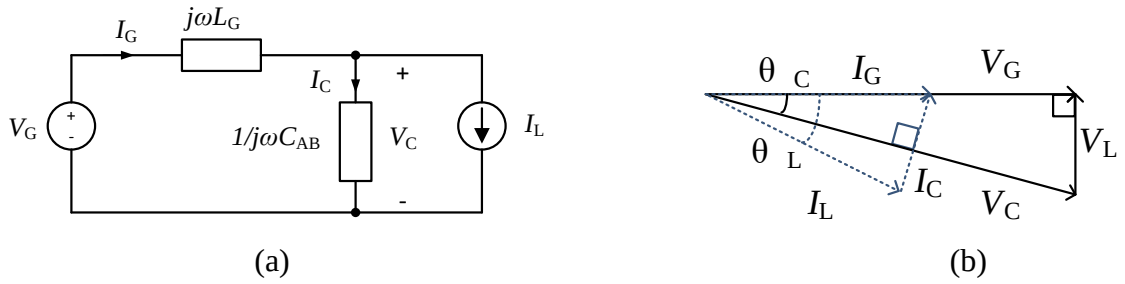
(a)



(b)

Fig. 3 Key waveforms of AVG-BPFC's (a) switches operational sequence and (b) capacitor switching behaviours.

The reconfigurable *LCL* structure can help to filter out the switching frequency components in the grid current loop. Thus, both the grid-side current ripple and the corresponding DM noise are reduced. Due to the filter capacitor clamping the potential difference between the AC power source and the ground, CM noise is able to be minimized. Therefore the large leakage current issue commonly appear in the traditional bridgeless PFC can be solved. Finally, the overall size of the EMI filter can be minimized in size and further optimized on the system CM and DM noises behaviour.



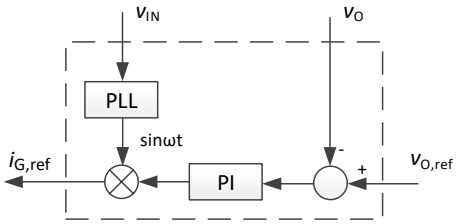
(a) (b)

Fig. 4 AVG-BPFC's (a) phasor domain equivalent circuit and (b) the corresponding vector diagram.

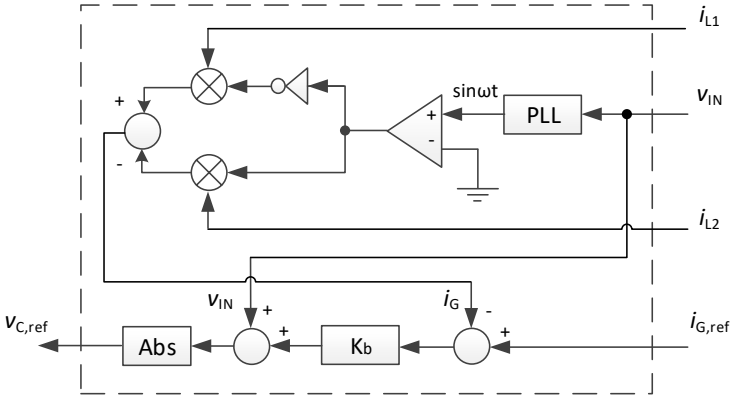
It can be noticed from the *LCL* filter characteristic, there is a phase shift generated between the grid current and the inductor current at the input stage. A line frequency phasor domain equivalent circuit of the AVG-BPFC is formed in Fig. 4 (a) to further elaborate the phase shift issue. Due to the symmetrical structure of the AVG-BPFC, the equivalent circuits of Fig. 2 can be combined together and modified to Fig. 4 (a). This can be done by changing the converter state into a continuous current source and transferring the system from time domain into phasor domain. In addition, a corresponding phasor diagram is shown in Fig. 4 (b). The capacitor voltage is lagging behind the grid voltage in a relative small angle, θ_C, due to the small impedance on between them. In addition, the inductor current is also lagging behind the grid current with a phase angle, θ_L. Especially, at light load condition the phase angle between both inductor current is very significant. Therefore it becomes one of the concern during the controller design of the AVG-BPFC.

B. Control Scheme

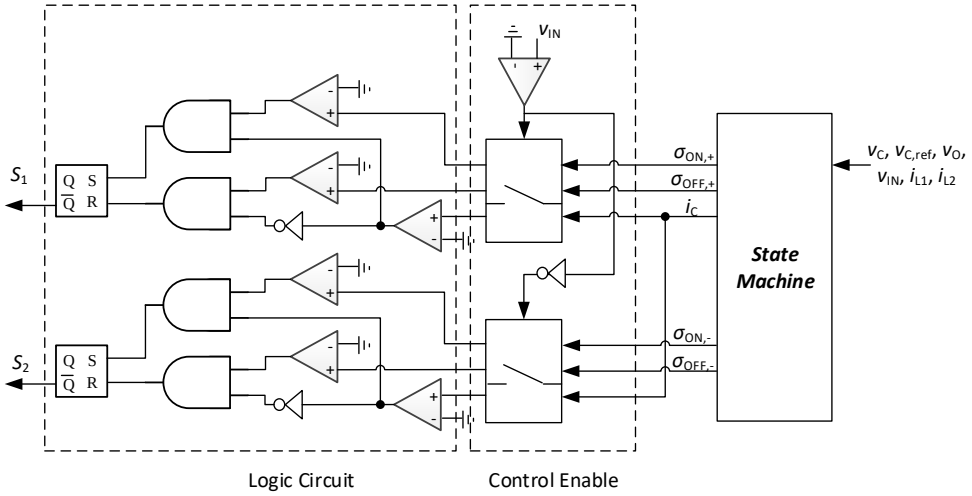
For the proposed control, three sets of voltage sensors are implemented on the system as shown in Fig. 1. The voltage sensors sense for the input voltage, v_{IN}, filter capacitor voltage, v_C, and output voltage, v_O, respectively. In addition, two sets of current sensors are used to measure the currents of the inductor L_1 and L_2, as $i_{L1}$and i_{L2} separately. The detailed block diagram of the proposed triple loop control architecture are shown in Fig. 5. The outer loop is a PI controller, middle loop is a deadbeat controller and the inner is a second-order boundary control loop. The logic flows of the proposed triple loop control architecture are shown in Section III C.



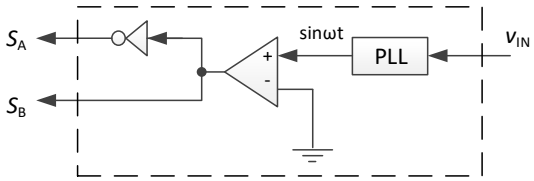
(a) PI Voltage Control



(b) Deadbeat Current Control



(c) Boundary Voltage Control



(d) SA/SB Control

Fig. 5 Flow Chart of the control diagram.

In the outer loop of the proposed control scheme, PI controller is aimed to regulate the output voltage

to the target output voltage, $v_{\mathrm{O,ref}}$, at a relatively slow speed. The corresponding control block diagram is shown in Fig. 5 (a). During dynamic change in the loading value, the rate change of the grid current is limited by the speed of the outer loop. Thus, the output voltage fluctuation level is well controlled within the targeting operation range. The output of the controller is a grid current reference, $i_{\mathrm{G,ref}}$.

A deadbeat controller is adopted as the middle loop to control the grid current, i_{G}. Under the deadbeat control, the phase shift issue which appears in [9] can be solved. The control block diagram is shown in Fig. 1 and the corresponding logic flow is shown in Fig. 5 (b). As the function of L_1 and L_2 is interchanged in each cycle, each of them only has half cycle acting as grid inductor. The grid current information is formed with the positive cycle current in L_2 and negative cycle current in L_1. By using the simple control structure, both fast dynamic current tracking function and high quality input current are achieved. The output of the controller is a filter capacitor voltage reference, $v_{\mathrm{C,ref}}$. In order to linearize the relationship between the grid current and the filter capacitor voltage reference, forward Euler method is applied in the digital control platform to derive the deadbeat controller theory. The equation is found as,

$$v_{\mathrm{C,ref}}[\mathrm{n}] = v_{\mathrm{G}}[\mathrm{n}] + K_{\mathrm{c}}\big(i_{\mathrm{G,ref}}[\mathrm{n}] - i_{\mathrm{G}}[\mathrm{n}]\big) \tag{1}$$

where $K_{\mathrm{C}} = -\frac{L_{\mathrm{g}}}{T_{\mathrm{s}}}$, T_{s} is sampling time, [n] is value at nth sampling point and L_{g} is grid side inductance. A detailed derivation of (1) is given in the Appendix.

The inner loop is implemented by a boundary controller with second-order switching surface to deal with the filter resonance issue and to regulate v_{C}. With the using of boundary controller, it can eliminate the resonance issue generated from the *LCL* input filter by simplifying its order in the transfer function. The details expression of the transfer function will be described in section III. As AVG-BPFC is a boost type rectifier, the boundary control method is applied to the input stage of the system. The corresponding switching surface is generated from the filter capacitor and the converter side inductor information. Unipolar switching method is adopted in this proposed scheme and the converter switching actions are generating from the boundary

controller. The corresponding block diagram is shown in Fig. 1 and the corresponding logic flow is shown in Fig. 5 (c). In the traditional control method, the PWM gate signals are generated by comparing the duty reference obtained from the PI controller with the system pre-set triangular wave. In the boundary control scheme, the switching actions are provided by estimating the state situation of the capacitor with the use of the system information, v_{C}, i_{C}, v_{IN}, and v_{O}. The capacitor current forms from i_{L1} and i_{L2} which is equal to $-i_{\mathrm{L1}} - i_{\mathrm{L2}}$. In every half line cycle, there are the corresponding switching criteria. To obtain the switching criteria, firstly the equation of the capacitor switching surface needs to be developed. In the development, current boundary is applied to handle the fixed frequency operation. In the positive cycle, the on-state equation is developed from the filter capacitor voltage and converter inductor current information. The equation of the capacitor switching surface at the on-state is formulated as,

$$v_{\mathrm{C}}(t) = v_{\mathrm{C,ref}}(t) + \frac{L_1}{2 \cdot C_{\mathrm{AB}} \cdot v_{\mathrm{C}}(t)} \left[i_{\mathrm{C,min}}(t)^2 - i_{\mathrm{C}}(t)^2 \right] \tag{2}$$

where $i_{\mathrm{C,min}}(t)$ is the minimum capacitor current generated from prediction. A detailed derivation of (2) is given in the Appendix.

The equation of the capacitor switching surface at off-state is formulated as,

$$v_{\mathrm{C}}(t) = v_{\mathrm{C,ref}}(t) - \frac{L_1}{2 \cdot C_{\mathrm{AB}} \cdot [v_{\mathrm{O}}(t) - v_{\mathrm{C}}(t)]} \left[i_{\mathrm{C,max}}(t)^2 - i_{\mathrm{C}}(t)^2 \right] \tag{3}$$

where $i_{\mathrm{C,max}}(t)$ is the maximum capacitor current generated from prediction. A detailed derivation of (3) is given in the Appendix.

Due to the symmetric structure of the converter, the capacitor switching surface equation at the negative half cycle is similar to (2) and (3). The only variation in the formula is the inductor term. L_1 is applied to the positive cycle deviation and L_2 is applied to the negative cycle deviation. The equations for negative half cycle are shown as follows,

at on-state,

$$v_{\mathrm{C}}(t) = v_{\mathrm{C,ref}}(t) + \frac{L_2}{2 \cdot C_{\mathrm{AB}} \cdot v_{\mathrm{C}}(t)} \left[i_{\mathrm{C,min}}(t)^2 - i_{\mathrm{C}}(t)^2 \right], \quad (4)$$

and at off-state,

$$v_{\mathrm{C}}(t) = v_{\mathrm{C,ref}}(t) - \frac{L_2}{2 \cdot C_{AB} \cdot [v_{\mathrm{O}}(t) - v_{\mathrm{C}}(t)]} \left[i_{\mathrm{C,max}}(t)^2 - i_{\mathrm{C}}(t)^2 \right]. \quad (5)$$

At the on-state, the control will use the off-state behaviours of the converter to generate the turn-off requirement. Similarly, at the turn-off state, the on-state behaviours will be used to generate the turn-on requirement. From (2) to (5), the system switching criteria can be expressed as (6) to (9). Take (7) as an example, it will predict whether or not the energy in the capacitor is sufficient to support the coming on-state operation. During the positive cycle with positive capacitor current, (7) will be active. Once the system satisfies the defined boundary requirement, the control will give out a switch-on signal to the switch S_1 and respond immediately. Otherwise the detection will be kept on until the conditions are met. The system program flow and the logic of the other three switching actions are shown in Fig. 5 (b) with their corresponding switching criteria.

For the positive cycle switch on criteria,

$$\sigma_{\mathrm{ON,+}}(t) = v_{\mathrm{C}}(t) - v_{\mathrm{C,ref}}(t) - \frac{L_1}{2 \cdot C_{\mathrm{AB}} \cdot v_{\mathrm{C}}(t)} \left[i_{\mathrm{C,min}}(t)^2 - i_{\mathrm{C}}(t)^2 \right] \geqq 0. \quad (6)$$

For the positive cycle switch off criteria,

$$\sigma_{\mathrm{OFF,+}}(t) = v_{\mathrm{C,ref}}(t) - v_{\mathrm{C}}(t) - \frac{L_1}{2 \cdot C_{\mathrm{AB}} \cdot [v_{\mathrm{O}}(t) - v_{\mathrm{C}}(t)]} \left[i_{\mathrm{C,max}}(t)^2 - i_{\mathrm{C}}(t)^2 \right] \geqq 0. \quad (7)$$

For the negative cycle switch on criteria,

$$\sigma_{\mathrm{ON,-}}(t) = v_{\mathrm{C}}(t) - v_{\mathrm{C,ref}}(t) - \frac{L_2}{2 \cdot C_{\mathrm{AB}} \cdot \mathrm{v_C(t)}} \left[i_{\mathrm{C,min}}(t)^2 - i_{\mathrm{C}}(t)^2 \right] \geqq 0. \quad (8)$$

For the negative cycle switch on criteria,

$$\sigma_{\mathrm{OFF,-}}(t) = v_{\mathrm{C,ref}}(t) - v_{\mathrm{C}}(t) - \frac{L_2}{2 \cdot C_{\mathrm{AB}} \cdot [v_{\mathrm{O}}(t) - v_{\mathrm{C}}(t)]} \left[i_{\mathrm{C,max}}(t)^2 - i_{\mathrm{C}}(t)^2 \right] \geqq 0. \quad (9)$$

To generate the *LCL* input filter structure, the switch S_A and S_B are switched alternatively and synchronized with the line frequency. It is implemented by using a polarity detector on the v_C signal. In the positive line voltage cycle, S_A is on and S_B is off. And in the negative line voltage cycle, the switching action is opposite. The grid current ripple is minimized and clamped the CM noise all the time by the AVG circuit. Its control block diagram is shown in Fig. 5 (d).

C. State Machine of the CCM and DCM Operation

By integrated the state machine into the second-order boundary control, it is possible to handle well in both continuous conduction mode (CCM) operation and discontinuous conduction mode (DCM) operation. In addition, by its fast dynamic response characteristics, it can offer a more precise current tracking function than the methodology with linear control. This is especially true during the zero crossing period [24] and the transition between CCM and DCM operation [25] where normally weak point in the traditional controller is located. High input power factor and low current THD can be obtained in the final.

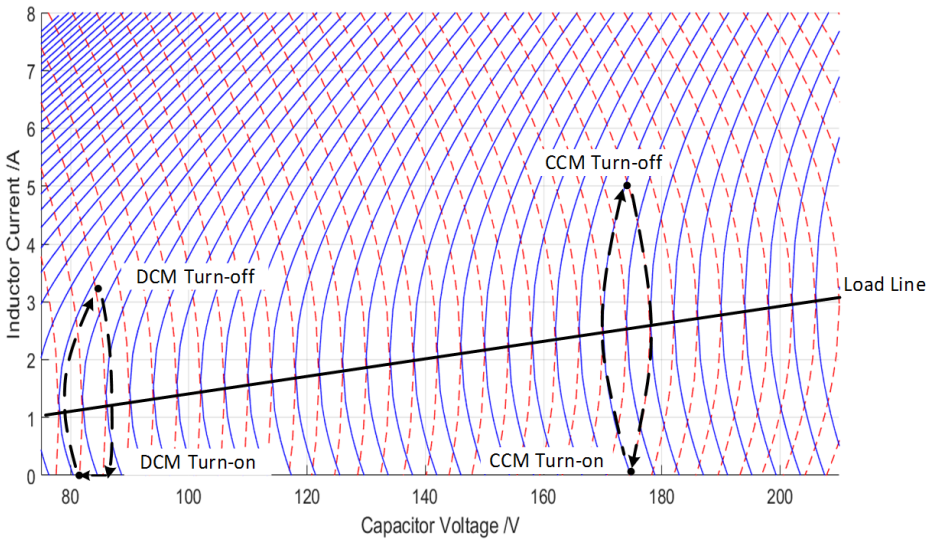


Fig. 6 The switching surface of the boundary control.

From the state equation, the switching trajectories of the AVG-BPFC can be plotted out as Fig. 6. The relationship between the inductor current and the capacitor voltage is demonstrated by the corresponding switching surface figure under the boundary operation. The red dotted line is drawn from the on-state

operation and the blue one is drawn from the off-state operation. Based on the boundary condition, at all time there will be two operation points in the figure and the switching action of the system will be following the trajectory line between them.

During the CCM operation, there are two operation steps in the whole switching period, as shown in Fig. 6. At the turn-on state, it starts from the CCM turn-on point and following the on-state trajectory line until it reach the target CCM turn-off point. Afterwards, the system will enter into the turn-off state and follow the off-state trajectory to return the CCM turn-off point to complete a period of switching. During the CCM operation, the capacitor current boundary can be defined as,

$$i_{\mathrm{C,min,CCM}}(t) = i_{\mathrm{C,max,CCM}}(t) = \Delta i_{\mathrm{C}}(t) = \frac{1}{2} \cdot \frac{v_{\mathrm{IN}}(t)}{v_{\mathrm{O}}(t)} \cdot \frac{v_{\mathrm{O}}(t) - v_{\mathrm{IN}}(t)}{L_{\mathrm{x}} \cdot f_{\mathrm{SW}}} \tag{10}$$

where L_{x} can be either L_1 or L_2 as the value is the same and f_{SW} is the switching frequency.

During the low load condition or low input voltage condition, the system will enter into the DCM operation. As shown in Fig. 6, one switching period is separated into three operation steps in the whole switching period. During the turn-on period, the on-state trajectory line is started from the DCM turn-on point and ended at the target DCM turn-off point. Then the system will enter into the turn-off state and follow the off-state trajectory before the inductor current becomes zero. Afterwards, the converter diode will block the path and avoid the negative current in the inductor. Converter-side inductor current will be zero. It will wait until the capacitor voltage charges up to the target DCM turn-on operation point and completes a period of switching. During the DCM, the capacitor current boundary can be defined as,

$$i_{\mathrm{C,max,DCM}}(t) = i_{\mathrm{G,ref}}(t), \tag{11}$$

$$i_{\mathrm{C,min,DCM}}(t) = 2 \cdot \sqrt{\Delta i_{\mathrm{C}}(t) \cdot i_{\mathrm{G,ref}}(t)} - i_{\mathrm{G,ref}}(t). \tag{12}$$

The state machine diagram is shown in Fig. 7 with the detailed logic flow. Due to the switching action, the voltage across C_{AB} is all the time in a positive sign and equals to a rectified sine waveform. In the circuit, L_1 and L_2 are set to the same inductance value. Therefore, the on-off state equations in the positive and the

negative half line cycle, (6) – (9), will be totally the same. $\sigma_{\mathrm{ON},+}(t)$ and $\sigma_{\mathrm{ON},-}(t)$ are combined as $\sigma_{\mathrm{ON}}(t)$ and $\sigma_{\mathrm{OFF},+}(t)$ and $\sigma_{\mathrm{OFF},-}(t)$ are combined as $\sigma_{\mathrm{OFF}}(t)$. Based on the switching state equation, the controller will determine whether changing the switching action or keep staying by using the same state. Also it will base on the value of $\Delta i_{\mathrm{C}}(t)$ and $i_{\mathrm{G,ref}}(t)$ to determine whether the DCM or CCM boundary should be applied. So that a precise control is achieved.

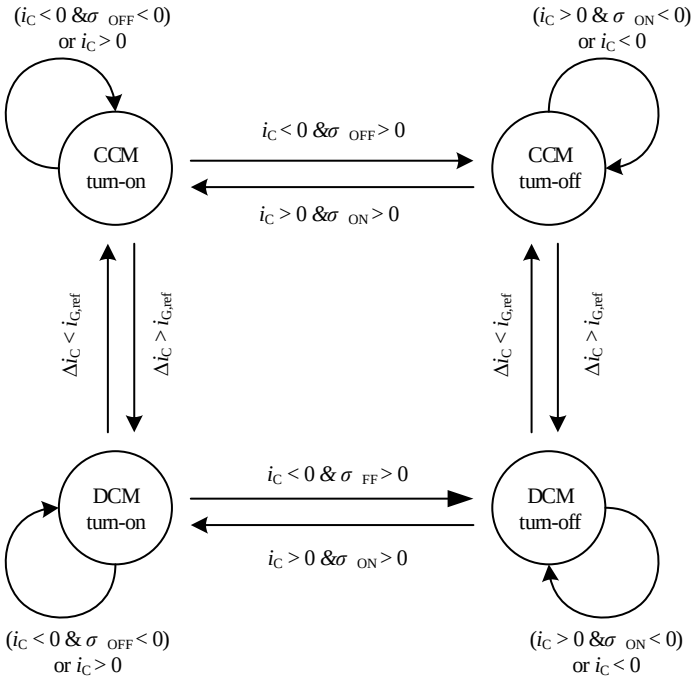
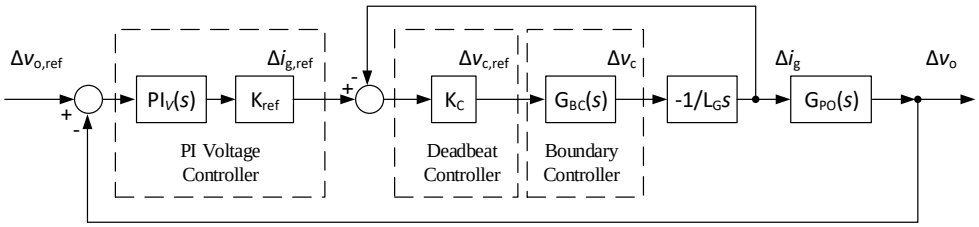


Fig. 7 The logic flow of the mode operation.

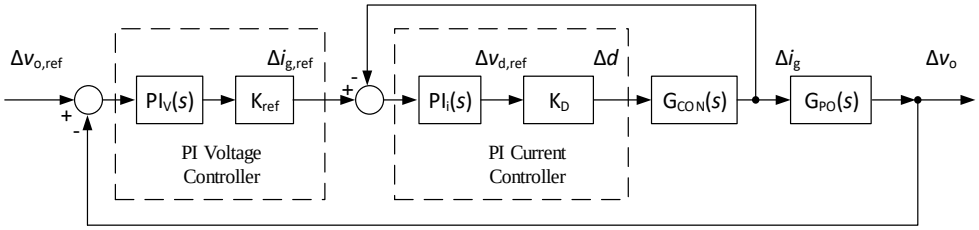
III. SYSTEM MODELLING AND IMPLEMENTATION

To analyze the system stability, small signal analysis method is applied. From the proposed control scheme as shown in Fig. 1, the corresponding small signal model is determined and is shown in Fig. 8 (a). At the same time, a small signal model of traditional PI controller is generated as a reference and is shown in Fig. 8 (b). In both cases, PI controller is used to implement in the outer loop to regulate the output voltage with the same set of controller parameter. The difference between the proposed control scheme and the traditional PI control scheme is in the inner loop which is the grid current loop. On the traditional control scheme, a linear PI controller aims to control the grid current. It generates the duty reference in the output and compares with

triangular wave in the PWM block to produce the switching signals. With the proposed scheme, a deadbeat controller is implemented to control the grid current together with a boundary controller inside to regulate the AC voltage. The inner loop is a nonlinear block and the switching signals are provided from its boundary controller. The inner loop cut off frequency, 1.1 kHz, is used as a reference point for both of the proposed control scheme and the PI control scheme.



(a)



(b)

Fig. 8 Block diagram of (a) the proposed control scheme and (b) PI control scheme

A. Proposed Current Loop

In order to study the stability of the PI current loop, both of the system and controller transfer functions are required. Due to the symmetric structure of the AVG-BPFC, only the positive half line cycle information is used to generate the model for the following system analysis. In the positive cycle, the grid current, $i_{\mathrm{G}}(t)$, is equal to the current appearing on the inductor L_2, $i_{L2}(t)$. L_1 acts as the converter side inductor and uses for the converter energy transfer. The capacitor C_{AB} is connected to the Line and the negative bus.

In the proposed control scheme, there are two controllers inside the grid current loop. They are boundary controller and a deadbeat controller. Under the proposed control scheme, all of the filter components

information are well under control. The grid side current is controlled by the deadbeat controller, and the capacitor voltage and the converter side inductor current are regulated by the boundary controller. By such method, the resonant issue appeared in the PI current control loop is eliminated. In order to analyze the system stability of the proposed control scheme, both of the system transfer function and the second-order boundary controller's transfer function are required.

Based on the method described in [16], the transfer function of the voltage boundary loop, $G_{\mathrm{BC}}(s)$, in the boost type rectifier can be developed and the boundary equation is found as,

$$G_{\mathrm{BC}}(s) = \frac{\Delta v_{\mathrm{c}}(s)}{\Delta v_{\mathrm{c,ref}}(s)} = \frac{1}{\frac{T}{4}s+1} \tag{13}$$

where T is switching period. A detailed derivation of (13) is given in the Appendix.

Based on the derived deadbeat controller theory, the corresponding transfer function of the deadbeat controller, $G_{\mathrm{DB}}(s)$, is found as,

$$G_{\mathrm{DB}}(s) = K_{\mathrm{C}} \tag{14}$$

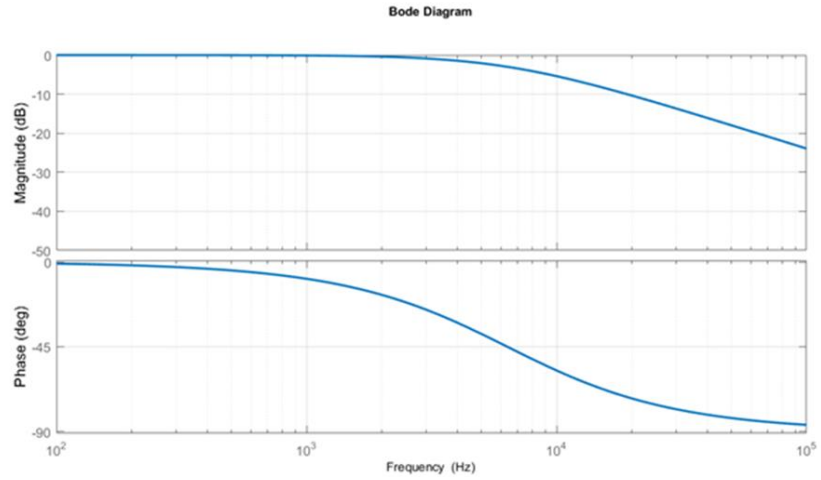
where a detailed derivation of (14) is given in the Appendix.

From the expression of (14), it shows that only a single proportional gain, K_{C}, is shown on its transfer function. Thus a simple and fast dynamic control is provided by the deadbeat controller. In addition, from the state equation of the filter capacitor, the transfer function between $\Delta i_{\mathrm{g}}(s)$ and $\Delta v_{\mathrm{c}}(s)$ can be formed as,

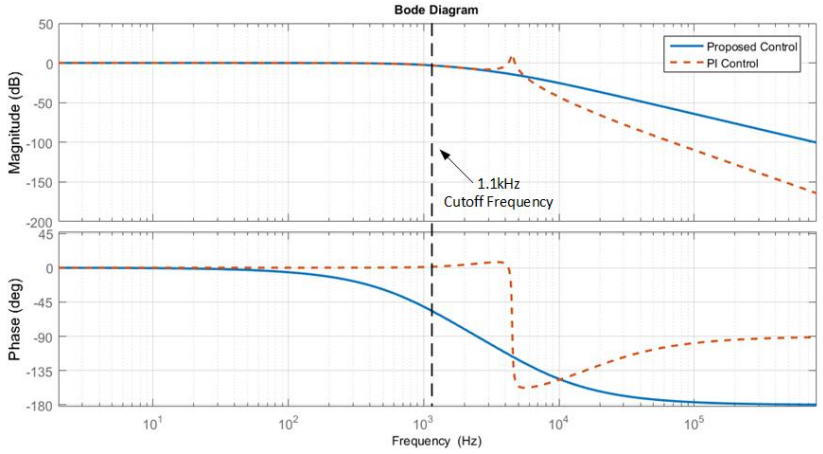
$$\frac{\Delta i_{\mathrm{g}}(s)}{\Delta v_{\mathrm{c}}(s)} = -\frac{1}{L_{\mathrm{g}} \cdot s}. \tag{15}$$

Therefore, by using (13) - (15), the overall closed loop transfer function of the proposed current control scheme, $G_{\mathrm{CC,new}}(\mathrm{s})$, is derived as,

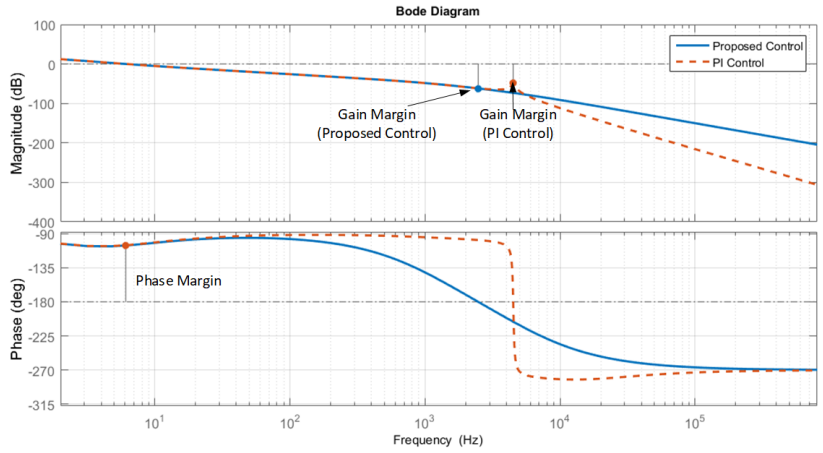
$$G_{\mathrm{CC,new}}(\mathrm{s}) = \frac{\Delta i_{\mathrm{g}}(s)}{\Delta i_{\mathrm{g,ref}}(s)} = \frac{K_{\mathrm{C}}}{\frac{T}{4} \cdot L_{\mathrm{g}} \cdot s^2 + L_{\mathrm{g}} \cdot s + K_{\mathrm{C}}}. \tag{16}$$



(a)



(b)



(c)

Fig. 9 Frequency plot of (a) the boundary block, (b) the current closed loop transfer function and (c) the overall open loop system transfer function.

In the reference PI control method, due to the *LCL* input filter structure, the converter transfer function becomes complicated and with a lot of poles in the expression [11]. A third order system will be generated in the inner loop of the PI control scheme together with a resonant pole. The current open loop Bode diagram of the Fig. 8 (b) is shown in Fig. 9 (b) with red color dotted line. Based on the targeted cut off frequency, a set of PI parameter is generated for the system performance analysis where Kp and K_{i} in the inner loop are 0.0325 and 3250 respectively. Moreover, the detailed derivation of the converter block, $G_{\mathrm{CON}}(s)$, is given in the Appendix as a reference.

With the proposed system, the boundary control helps to simplify the system order and offers a first order system in the inner loop as (13). Therefore the current closed loop transfer function becomes simple and the *LCL* resonant issue is also eliminated. A much simpler and more stable control loop is provided under the proposed control scheme. The corresponding frequency plots of $G_{\mathrm{BC}}(s)$ and $G_{CC,new}(s)$ are shown in Fig. 9 (a) and the blue line in Fig. 9 (b) respectively. It showed that the system is stable under the proposed control scheme, which eliminated the resonance issue from the converter stage. Therefore the design of the system bandwidth no longer contradicts the *LCL* resonant frequency. A 4.3 kHz *LCL* resonant frequency will appear on the system structure. However under 1.1 kHz control bandwidth in current loop, the system can still maintain stable operation as the resonance is eliminated by the boundary control method. The controller design is more fixable.

From the expression of (13) and (16), it shows that the current loop stability is available to support wide range of operation including varying loading condition and the output voltage jumping. The inner loop transfer functions no longer depends on the system parameter but only relates to the switching frequency and the variation of the passive components. As a result, a stable phase margin is obtained all the time. Also under the proposed control methodology, more system parameters are available to control but in a simpler structure.

B. Overall system stability of the proposed control scheme

In order to analyze the overall system stability, a whole system open loop Bode diagram is required. K_{ref}, as shown in the outer loop in Fig. 8, is a proportional gain which correlates with the input voltage value.

The transfer function of the outer loop, $G_{\mathrm{PO}}(s)$, is expressed as:

$$G_{\mathrm{PO}}(s) = \frac{\Delta v_{\mathrm{o}}(s)}{\Delta i_{\mathrm{g}}(s)} = \frac{V_{\mathrm{IN}}}{V_{\mathrm{O}}} \cdot \left(\frac{R_{\mathrm{O}}}{2+R_{\mathrm{O}} \cdot C_{\mathrm{O}} \cdot s}\right) \tag{17}$$

where C_{O} is output capacitor, R_{O} is output resistance. A detailed derivation of (17) is given in the Appendix.

Lastly, the transfer function of PI voltage controller, $G_{\mathrm{PIv}}(\mathrm{s})$, in the outer loop can be expressed as:

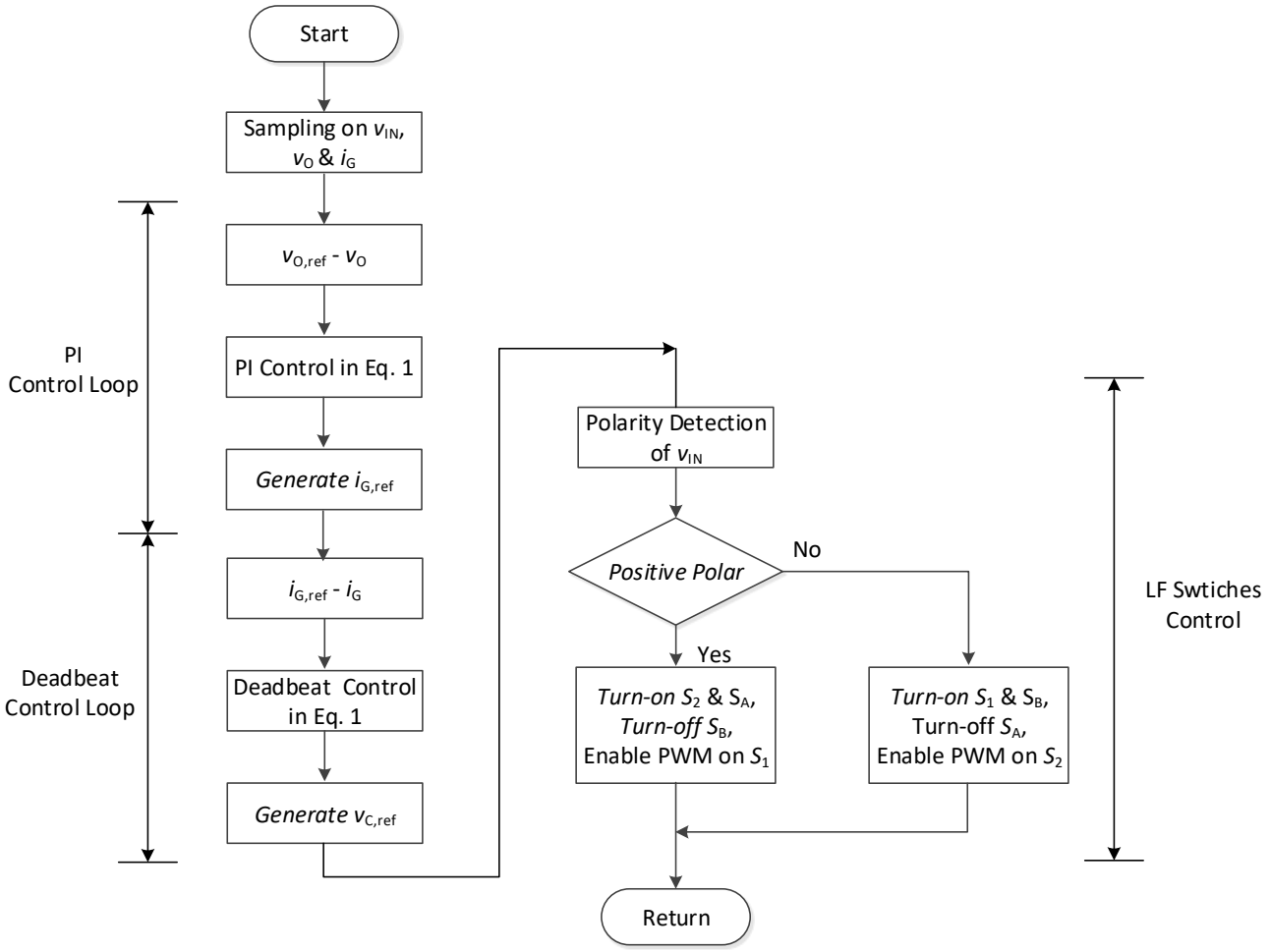
$$G_{\mathrm{PIv}}(\mathrm{s}) = \frac{K_{\mathrm{p}} \cdot \mathrm{s} + K_{\mathrm{i}}}{\mathrm{s}}. \tag{18}$$

By using K_{ref}, (16), (17) and (18), the overall open-loop characteristic of both control schemes are found. To achieve the phase margin in the system on the PI control scheme, an extra low pass filter is also implemented into the digital control. The system stability can be observed from the Bode diagram which is shown Fig. 9 (c) where the Kp and K_{i} in the outer loop are 0.02352 and 0.000706 respectively. The proposed control scheme is in the blue straight line with 61.9 dB gain margin together with 74.6° phase margin. The PI control scheme is in red dotted line with 48.7 dB gain margin together with 74.6º phase margin. It showed that the output voltage can regulate well under both of the system. In the proposed control scheme, the gain margin is more than the PI control scheme due to the elimination of the resonant characteristic. Also no more resonance pole appeared in the voltage control loop. Therefore with the use of the proposed control scheme, a stable operation system can be built.

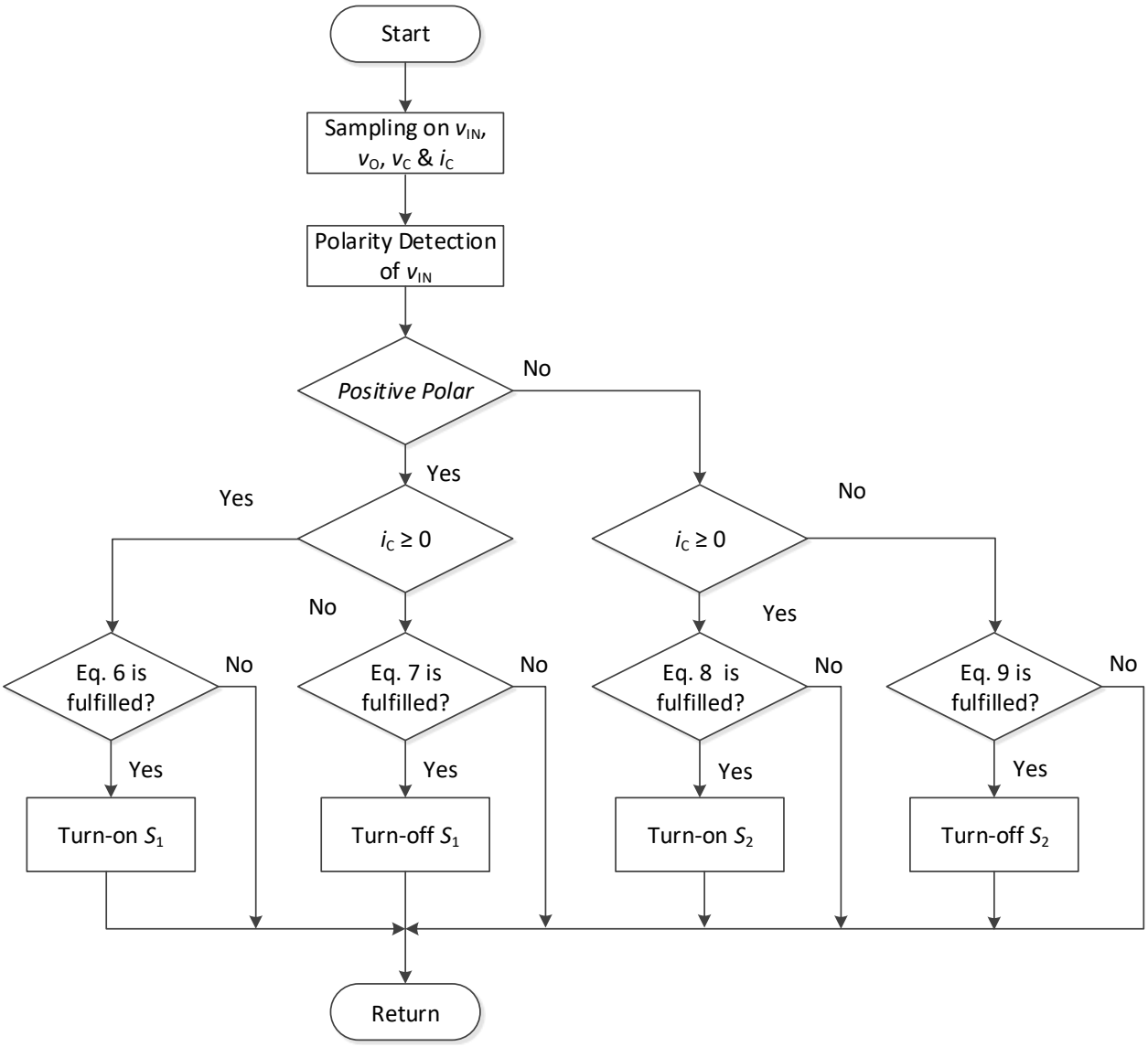
C. Implementation of the Digital Control

The whole controller system is built in the TI TMS320F28375S microcontroller. The details program flow of the digital control system is shown in Fig. 10. The outer loop is written in the CPU by converting (18), the transfer function of the PI controller, into z-domain to regulate the output voltage. In the middle loop, the relationship between the grid current error and the capacitor voltage is linearized by the deadbeat controller.

Thus, a precise current tracking is able to be done in a simple way. Finally in the inner loop, the switching criteria is generated from the CLA calculation and does comparison in the EPWM block to generate switching action. As a result, the whole system is implemented in the digital platform in a simple way.



(a) PI voltage control and deadbeat current control loop



(b) Boundary voltage control loop

Fig. 10 Program flow diagram of the proposed control scheme.

As the switching action comes from predication, a cycle delay is usually existed in the digital platform. Therefore, the sensor updating rate in the digital control platform should be kept 80 to 100 times faster than target switching speed. This can help to maintain the accuracy of the switching action and to generate a very precise $\boldsymbol{v_C}$ control in the inner loop. In the design, the inner loop frequency is targeted to 1MHz and the target operation frequency is selected to 10 kHz under the 100 times sampling criteria.

IV. EXPERIMENTAL VERIFICATION

A 1.5 kW AVG-BPFC prototype is implemented as shown in Fig. 11 with the specification shown in TABLE I. The system code is written in the TI TMS320F28375S microcontroller. The AVG capacitor, C_{AB}, value is chosen as 3.3 µF which is based on the criteria of circuit resonance frequency and target leakage current requirement [9]. The steady state performance of the proposed AVG-BPFC control scheme is proofed under different power ratings operation and the dynamic performance is proofed by the transient performance during an instantaneous load change and varying input voltage. A FFT analysis is applied to the inductor current. From the resulted frequency spectrum, as shown in Fig. 12 (a), it demonstrates that the proposed control scheme is able to fix the system switching frequency to the target value as 10kHz which able to proof the control theory. If any tolerance appears in the converter-side inductance, the switching time period will be changed. In addition, referred to [26], a 470pF capacitor is applied to the system as the parasitic capacitor between the system ground point and the Natural point of the grid in order to demonstrate the low leakage current of the system. The HF common mode noise voltage generated by the system is limited to a low amplitude level and the leakage current is able to limit mA level which fulfills the theory mentioned on [9]. The measured result leakage current is shown in Fig. 12. In addition, a conductive EMI test is done in order to demonstrate the advantage of the AVG-BPFC over the traditional BPFC as shown in Fig. 13. The result matched with the prediction in [9] which is very clear that the noise level in the traditional BPFC is much higher than the AVG-BPFC in the range within 2MHz. At the MHz frequency range, the noise level is varying as both topologies have different input filter components.

TABLE I VALUE OF THE SYSTEM CONDITION USED IN THE DESIGN

Parameter	Value	Parameter	Value
Input Voltage	120 Vac	Output Voltage	380 Vdc
Input Frequency	60 Hz	Max. Output Power	1.5 kW
Switching Frequency	10 kHz	Output Capacitor	1.2 mF
Inductor (L_1 & L_2)	0.78 mH	Capacitor (C_{AB})	3.3 µF

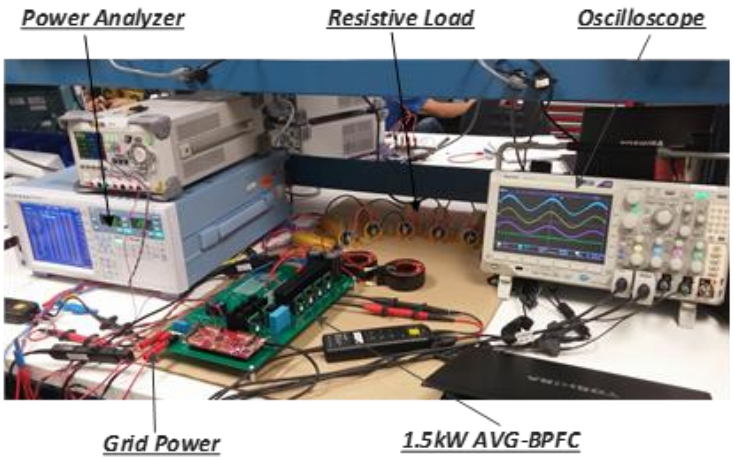
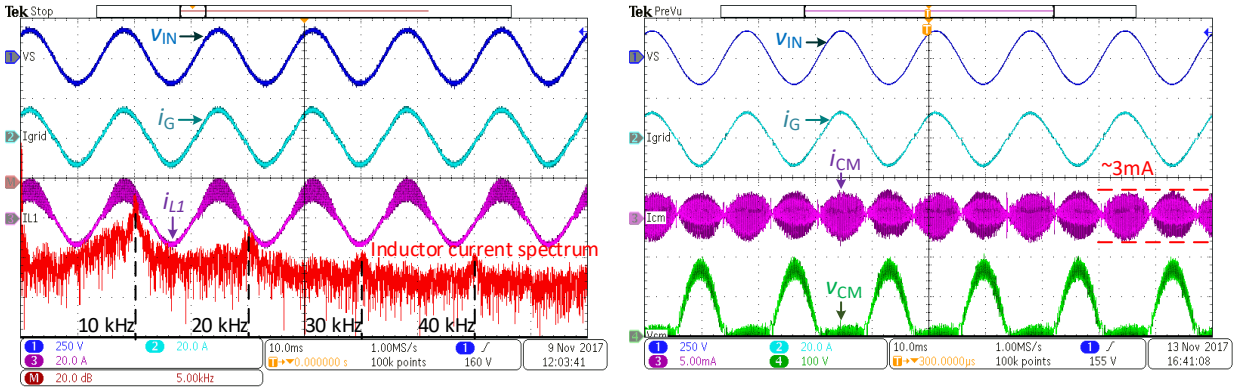


Fig. 11 Experimental test setup.



(a) (b)

Fig. 12 Experimental waveforms of the proposed control scheme with (a) the inductor current's FFT analysis and (b) the leakage current measurement at 1kW output.

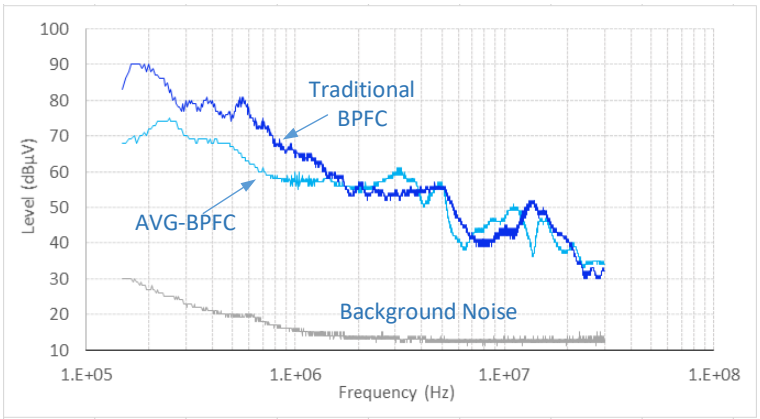
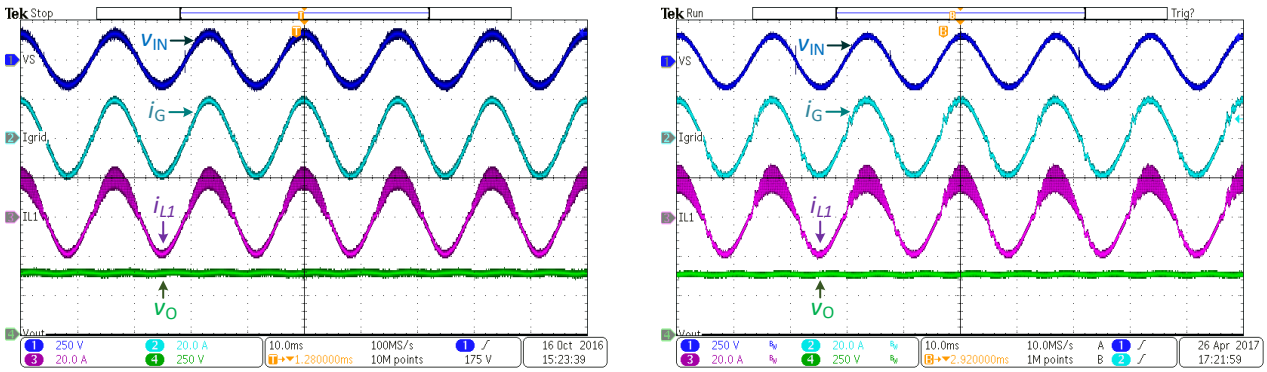


Fig. 13 Conductive EMI measurement of the traditional BPFC and AVG-BPFC at 1kW output.



(a) (b)

Fig. 14 Experimental waveforms of (a) the proposed control scheme and (b) the PI control scheme at 1.5kW output.

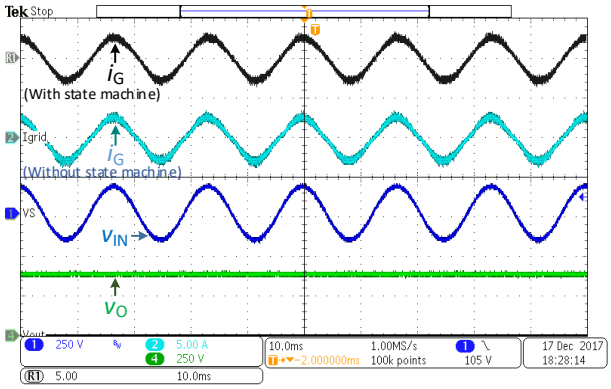


Fig. 15 Experimental waveforms of the proposed control scheme at 230W with and without state machine.

The steady state waveforms of the AVG-BPFC with the proposed control scheme are shown in Fig. 14 (a) and Fig. 15. Fig. 14 (a) was operated in the CCM mode with 100% loading condition and Fig. 15 was operation in the DCM mode with 15% loading condition. All of them showed that under the proposed control methodology, a stable waveform can be obtained together with a good system performance. From those steady state waveforms, it demonstrated the system can operate correctly. During the positive line cycle, L_1 carried a large HF current ripple as it was the converter side inductor. While a relatively small HF current ripple appeared on the grid due to the generated input *LCL* structure. In the negative half line cycle, the function of L_1 and L_2 were interchanged, the inductor L_1 became the grid side inductor. Thus, the current ripple that

appeared in L_1 was the same as the grid current ripple. These waveforms were matched with the behaviours of input *LCL* filter and the converter characteristics.

Under the proposed control scheme, the input power factor was above 0.996 among the whole power range. From the waveforms, it demonstrated that the phase shift problems were solved. Also a good power and current quality system were obtained as the resonant issue was eliminated by the proposed control scheme. At the full load condition, the system efficiency was 94.32% and the voltage THD was 0.11% together with 3.48% current THD, where Fig. 14 (a) was the corresponding operation waveform. At light load DCM mode, the system can still maintain good power quality and high efficiency. At 15% power rating, 96.20% efficiency was achieved and the system was stable as shown in Fig. 14. The corresponding voltage THD and current THD were 0.022% and 2.80% respectively. The current harmonic spectrum of Fig. 14 (a) and Fig. 15 (b) are shown in Fig. 16 and Fig. 17 respectively. Under the proposed scheme, the AVG-BPFC could fulfill the IEEE 519 class A standard requirement and all harmonics are under the limitation line [27].

Comparing with the waveforms generated by the conventional PI method, as shown in Fig. 14 (b), the waveforms from the proposed control system were more promising. As shown in Fig. 14 (b), although the system output was able to regulate at a stable value, current distortion appeared in the grid current waveform, especially in the zero current point together with some small oscillation. Therefore the input power factor and the THD were also affected. It degraded the system performance and generated stability concerns. In the 1.5kW test case, the total voltage harmonic and the current harmonic of PI control method were 0.24% and 5.77% respectively. The current harmonic was at least 2.2% more than the proposed scheme. The corresponding input current harmonic spectrum is shown in Fig. 16. Due to the resonance issue in the PI control loop, the current harmonics of 13rd to 19th in of the PI control scheme were higher than the proposed control scheme. In the meantime, the measured values were over the limitation of the industry standard. Moreover the harmonics may influence the system stability causing abnormal operations under the resonant issue. To limit the harmonic contents, the control bandwidth needs to be decreased or an extra input filter is

required. However, the dynamic performance will be influenced. With the proposed control scheme, it can successfully eliminate the resonant pole from the *LCL* system input structure.

In Fig. 15, it showed the performance different between using and not using the state machine under the proposal method. During light load operation, the system was operated in DCM condition. When the proposed control system didn't integrate with the state machine, once the inductor current reached ~~will meet the~~ zero and the switch would be immediately turned on. Therefore the grid current waveform was distorted and the frequency was varying. The total voltage harmonic and the current harmonic were 0.024% and 6.20% respectively. Also a higher 3rd and 5th order harmonics were resulted. Due the current distortion issue, the current harmonics in the 15% loading condition was at least 3.4% lower when the state machine didn`t integrated on top of the proposed control scheme. The corresponding input current harmonic spectrum is shown in Fig. 17. Under the implementation of the state machine, high grid current quality is able to achieve in both CCM and DCM condition. The system was well controlled by the digital controller and the power quality was improved.

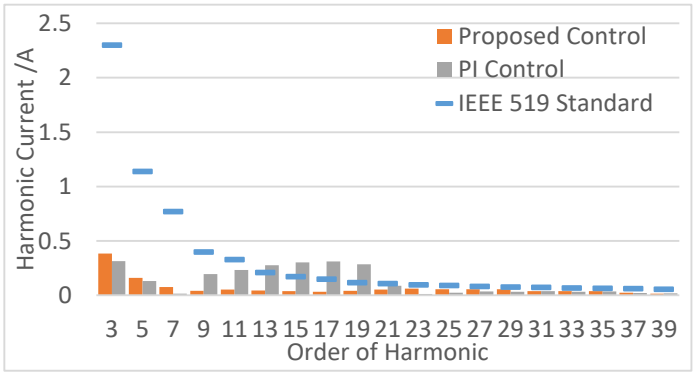


Fig. 16 Input current harmonic comparison between the proposed control scheme and the PI control scheme at 1.5kW

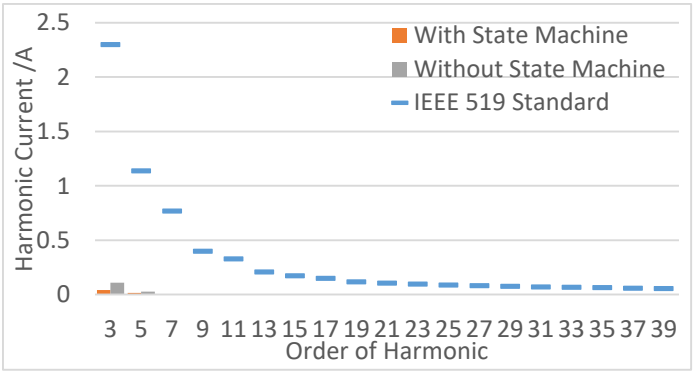
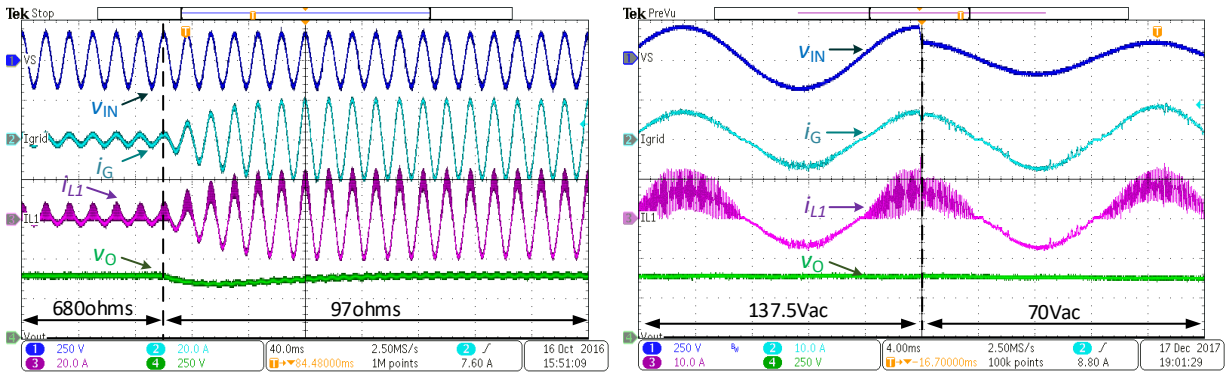
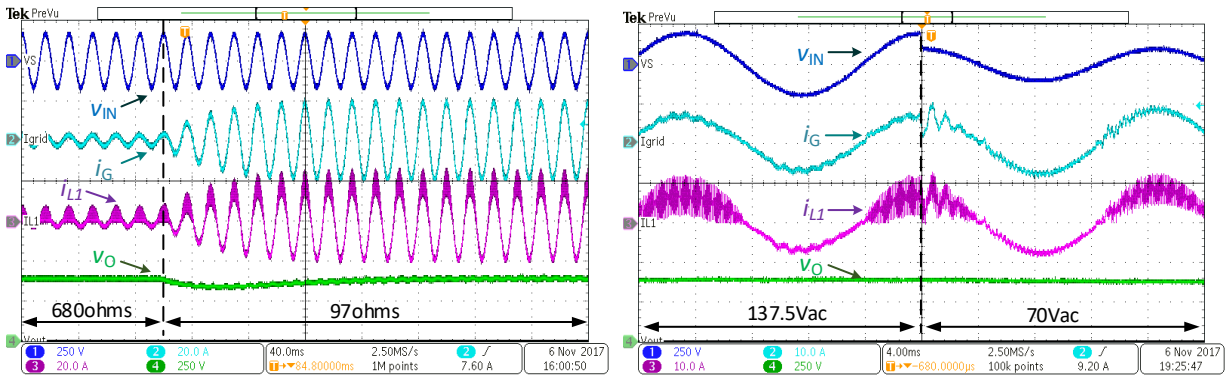


Fig. 17 Input current harmonic comparison between the proposal control scheme with and without state machine at 230W.

During the steady state operation, the system was performed well and this also happened in the transient operation. In Fig. 18 (a) showed out the system performance during the load transient in which the load was jumping from 680ohms to 97ohms. Another transient test was the grid voltage jumping, as shown in Fig. 18 (b), the input voltage was jumping from 137.5V to 70V. In both test cases, the system was also stable and was able to convert into the steady state in a short moment of time after the change appeared. For comparison, the same set of transient test is applied to the PI control scheme. The load transient waveform is shown in Fig. 18 (c) and the grid voltage jumping waveform is shown in Fig. 18 (d). In both situations, the system can still keep stable on the output voltage regulation.



(a) (b)



(c) (d)

Fig. 18 System transient response waveforms, the proposed control scheme at (a) load change and (b) input voltage sag, and the PI control scheme at (c) load change and (d) input voltage sag.

In the load transient test, the transient action influences to the system power level and the main effect appears on the outer loop of the system. The same output voltage transient performance is observed in the proposed control scheme and the PI control scheme, as the same set PI controller is applied in both control scheme. In the grid voltage jumping test, the transient action influences to the system grid current magnitude and the main effect appears on the inner loop of the system. In the proposed control scheme, the inner loop can provide a fast response to the system and smooth the action in the transient period. However, in the PI control scheme, the response was lower and a larger oscillation was appeared on the grid current waveform. Also low frequency harmonics were observed in the steady state.

All of the results of the proposed control scheme had a very good alignment with the theoretical control principle and fulfill the target design specification. Finally a stable system was provided from such triple loop control architecture for an AVG-BPFC system.

V. CONCLUSIONS

The paper has presented an advanced digital control scheme for the Active Virtual Ground-bridgeless PFC. The system implementation and detailed small signal model are given in this paper. Such proposed

control scheme improves the system stability and enhances grid current quality under various loading conditions. In addition, it performs well in the system transient response. As a result, under the proposed control structure, the advantages of the AVG-BPFC can be maximized in order to achieve high system efficiency, low leakage current, small magnetic components and high current quality. The performance of the AVG-BPFC and the proposed control methodology was demonstrated with the experimental results. A 120 V, 60 Hz, 1.5 kW prototype has been implemented in order to verify the presented concept. There was a good agreement between theoretical concept and experimental results.

VI. DISCUSSION OF THE DESIGN LIMITATION

In practice, there always has an upper limit on the maximum system control bandwidth and the available system operation frequency which are limited by program computation time and the ADC sampling rate. Different from PI control, more instruction codes are required in the proposed control method. Therefore a longer computation time is needed. In order to minimize the computation time, CLA (control law accelerator) is used. The CLA is applied to handle the sensor data and to compute the boundary control criteria. It can work parallel with the main CPU which is used to handle the system program flow. Thus, by separating the work systematically, the overall computation time can be maintained in a minimized time and the loop frequency is within MHz range.

For the selected controller, TMS20F28377S, 2 ADC channels are offered and each of them has a maximum sampling rate of 3.5MHz. However, in the proposed control architecture, 5 sensor signals are required which means that the actual maximum sampling rate is downscale to 1.19MHz. Therefore, based on the program length and the ADC updating speed, 1MHz is finally selected as the platform inner loop operation frequency. In addition, under the 100 sample point criteria, 10 kHz is selected at the target switching frequency. On the existing digital control platform, if the operation frequency is increased, the accuracy of the control will be reduced. Therefore, if higher frequency operation is required, a digital controller with a faster

ADC is recommended.

APPENDIX

A. *Derivation of (1)*

From equivalent circuits on Fig. 2, state equation of the system input can be found as,

$$L_{\mathrm{G}} \frac{di_{\mathrm{G}}(t)}{dt} = v_{\mathrm{IN}}(t) - v_{\mathrm{C}}(t) \qquad \text{(A 1)}$$

where L_{G} is the grid inductor which is equal to L_1/L_2 as both are having the same value.

By applying forward Euler method on (A1) under discrete time domain, the equation is modified as,

$$L_{\mathrm{G}} \frac{i_G[n+1]-i_G[n]}{T_{\mathrm{S}}} = v_{\mathrm{IN}}[n+1] - v_{\mathrm{C}}[n+1] \qquad \text{(A 2)}$$

Under the prediction of deadbeat control, $i_{\mathrm{G}}[n+1]$ is equal to $i_{\mathrm{G,ref}}[n]$ and $i_{\mathrm{G}}[n+1]$ is equal to $i_{\mathrm{G,ref}}[n]$. Also the variation of v_{IN} is small between each sampling period, therefore $v_{\mathrm{IN}}[n+1] \cong v_{\mathrm{IN}}[n]$. As a results, (1) can be obtained.

B. *Derivation of (2)*

From the on-state circuit in the positive line cycle, the equation of capacitor current and the voltage are defined as,

$$\frac{\mathrm{d}i_{\mathrm{C}}(t)}{\mathrm{d}t} = -\frac{\mathrm{d}i_{\mathrm{L1}}(t)}{\mathrm{d}t} = -\frac{v_{\mathrm{C}}(t)}{L_2} \Longrightarrow \mathrm{d}t = -\frac{L_1}{v_{\mathrm{C}}(t)} \cdot \mathrm{d}i_{\mathrm{C}}(t) \qquad \text{(A 3)}$$

and

$$C_{\mathrm{AB}} \frac{\mathrm{d}v_{\mathrm{C}}(t)}{\mathrm{d}t} = i_{\mathrm{C}}(t) \Longrightarrow C_{\mathrm{AB}} \cdot \mathrm{d}v_{\mathrm{C}}(t) = i_{\mathrm{C}}(t) \cdot \mathrm{d}t. \qquad \text{(A 4)}$$

By combining (A3) and (A4) together with the predicating values at t_2, (2) can be obtained.

C. *Derivation of (3)*

The off-state equation in the positive line cycle is derived under the same method of deviation in the

on-state. The same voltage equation (A4) is used and the corresponding current equation of the capacitor is renewed as,

$$\mathrm{d}t = -\frac{L_1}{v_{\mathrm{C}}(t)-v_{\mathrm{O}}(t)} \cdot \mathrm{d}i_{\mathrm{C}}(t). \tag{A 5}$$

By combining (A4) and (A5) with predicating values at t_4, (3) can be obtained.

D. Derivation of (13)

In the boundary control, the capacitor voltage reference, $v_{\mathrm{C,ref}}$, is defined as,

$$v_{\mathrm{C,min}}(t_{\mathrm{OFF}}) + v_{\mathrm{C,max}}(t_{\mathrm{ON}}) = 2 \cdot v_{\mathrm{C,ref}}(t). \tag{A 6}$$

Similar to (2) and (3), with the prediction value at t_1 and at t_3 respectively, another set of capacitor switching surface equations is formulated as,

at on-state,

$$v_{\mathrm{C}}(\mathrm{t}) = v_{\mathrm{C,max}}(\mathrm{t}) + \frac{L_1}{2\cdot[v_{\mathrm{C}}(t)-v_{\mathrm{O}}(t)]\cdot C_{\mathrm{AB}}} \cdot i_{\mathrm{C}}(\mathrm{t})^2 \tag{A 7}$$

and off-state,

$$v_{\mathrm{C}}(\mathrm{t}) = v_{\mathrm{C,min}}(\mathrm{t}) + \frac{L_1}{2\cdot v_{\mathrm{C}}(t)\cdot C_{\mathrm{AB}}} \cdot i_{\mathrm{C}}(\mathrm{t})^2. \tag{A 8}$$

By considering $\Delta v_{\mathrm{o}}(t)$, $\Delta i_{\mathrm{L1}}(t)$, $\Delta v_{\mathrm{c}}(t)$, $\Delta v_{\mathrm{c,ref}}(t)$, $\Delta i_{\mathrm{g}}(t)$ and Δd as the small-signal perturbations of v_{O}, i_{L1}, v_{C}, $v_{\mathrm{C,ref}}$, i_{G} and D respectively for the (A7) – (A8). In the AVG-BPC, the circuit is symmetric in each half line cycle. (13) can be formed with the same method descripted in [16] for the boost state converter.

E. Derivation of (14)

By considering $\Delta v_{\mathrm{c,ref}}[n]$, $\Delta v_{\mathrm{g}}[n]$, $\Delta i_{\mathrm{g,ref}}[n]$ and $\Delta i_{\mathrm{g}}[n]$ as the small-signal perturbations of $v_{\mathrm{C,ref}}$, v_{G},$i_{\mathrm{G,ref}}$ and i_{G} respectively in the small signal analysis model, (1) can be rearranged into the small-signal perturbations equations in frequency domain as,

$$\Delta v_{\mathrm{c,ref}}(s) = K_C\big(\Delta i_{\mathrm{g,ref}}(s) - \Delta i_{\mathrm{g}}(s)\big). \tag{A 9}$$

By rearranging (A9), (14) can be obtained.

F. Derivation of $\mathrm{G_{CON}}(s)$

The averaged state equations of the AVG-BPFC are listed in the following,

$$C_{\mathrm{O}} \frac{dv_{\mathrm{O}}(t)}{dt} = -\frac{v_{\mathrm{O}}(t)}{R_{\mathrm{O}}} + i_{L1}(t) \cdot (1 - D) \quad \text{(A 10)}$$

$$L_1 \frac{di_{\mathrm{L1}}(t)}{dt} = v_{\mathrm{C}}(t) - v_{\mathrm{O}}(t) \cdot (1 - D) \quad \text{(A 11)}$$

$$C_{\mathrm{AB}} \frac{dv_{\mathrm{C}}(t)}{dt} = i_{\mathrm{G}}(t) - i_{L1}(t) \quad \text{(A 12)}$$

$$L_2 \frac{di_{\mathrm{G}}(t)}{dt} = v_{\mathrm{IN}}(t) - v_{\mathrm{C}}(t) \quad \text{(A 13)}$$

where *D* is duty cycle.

By considering $\Delta v_{\mathrm{o}}(t)$, $\Delta v_{\mathrm{c}}(t)$, $\Delta i_{L1}(t)$, $\Delta i_{\mathrm{g}}(t)$ and Δd as the small-signal perturbations of v_{O}, v_{C},i_{L1}, i_{G} and *D* respectively in the small signal analysis model, (A10) – (A13) can be rearranged into the small-signal perturbations equations in frequency domain as:

$$C_{\mathrm{O}} \cdot s \cdot \Delta v_{\mathrm{o}}(s) = \frac{-1}{R_{\mathrm{O}}} \cdot \Delta v_{\mathrm{o}}(s) - I_{L1}(s) \cdot \Delta d + \overline{D} \cdot \Delta i_{L1}(s) \quad \text{(A 14)}$$

$$L_1 \cdot \Delta i_{L1}(s) \cdot s = \Delta v_{\mathrm{c}}(s) + V_{\mathrm{O}} \cdot \Delta d - \overline{D} \cdot \Delta v_{\mathrm{o}}(s) \quad \text{(A 15)}$$

$$C_{\mathrm{AB}} \cdot \Delta v_{\mathrm{c}}(s) \cdot s = \Delta i_g(s) - \Delta i_{L1}(s) \quad \text{(A 16)}$$

$$\Delta i_{\mathrm{g}}(s) \cdot L_2 \cdot s = -\Delta v_{\mathrm{c}}(s) \quad \text{(A 17)}$$

where $\overline{D}$ equals to 1-*D*.

By combining (A 14) - (A 17), the transfer function of the converter stage, $\mathrm{G_{CON}}(s)$, can be obtained as,

$$\mathrm{G_{CON}}(s) = \frac{\Delta i_{\mathrm{g}}(s)}{\Delta d(s)} = \frac{2 \cdot V_{\mathrm{O}} \cdot (C_{\mathrm{O}} \cdot s + \frac{1}{R_{\mathrm{O}}})}{C_{\mathrm{O}} \cdot Z_{\mathrm{T}} \cdot s^4 + \frac{Z_{\mathrm{T}}}{R_{\mathrm{O}}} \cdot s^3 + [C_{\mathrm{O}} \cdot (L_1 + L_2) + \overline{D}^2 \cdot C_{\mathrm{AB}} \cdot L_2] \cdot s^2 + \frac{L_1 + L_2}{R_{\mathrm{O}}} \cdot s + \overline{D}^2}. \quad \text{(A 18)}$$

G. Derivation of (17)

The system power equations are listed as following,

$$p_{\mathrm{IN}}(t) = p_{\mathrm{O}}(t) + p_{\mathrm{C}}(t) \quad \text{(A 19)}$$

$$p_{\mathrm{IN}}(t) = v_{\mathrm{IN}}(t) \cdot i_{\mathrm{G}}(t) \quad \text{(A 20)}$$

$$p_{\mathrm{O}}(t) = \frac{v_{\mathrm{O}}(t)^2}{R_{\mathrm{O}}} \quad \text{(A 21)}$$

$$p_{\mathrm{C}}(t) = \frac{1}{2} \cdot C_{\mathrm{O}} \frac{dv_{\mathrm{O}}(t)^2}{dt} \quad \text{(A 22)}$$

where $p_{\mathrm{IN}}(t)$ is input power, $p_{\mathrm{O}}(t)$ is output power and $p_{\mathrm{C}}(t)$ is capacitor power.

By considering $\Delta p_{\mathrm{in}}(t)$, $\Delta p_{\mathrm{o}}(t)$, $\Delta p_{\mathrm{c}}(t)$, $\Delta i_{\mathrm{g}}(t)$ and $\Delta v_{\mathrm{o}}(t)$ as the small-signal perturbations of $p_{\mathrm{IN}}(t)$, $p_{\mathrm{O}}(t)$, $p_{\mathrm{C}}(t)$, $i_{\mathrm{G}}(t)$ and $v_{\mathrm{O}}(t)$ respectively in the small signal analysis model, (A19) - (A22) can be updated into frequency domain small-signal perturbations equations as,

$$\Delta p_{\mathrm{in}}(s) = \Delta p_{\mathrm{o}}(s) + \Delta p_{\mathrm{c}}(s) \quad \text{(A 23)}$$

$$\Delta p_{\mathrm{in}}(s) = V_{\mathrm{IN}} \cdot \Delta i_{\mathrm{g}}(s) \quad \text{(A 24)}$$

$$\Delta p_{\mathrm{o}}(s) = \frac{2 \cdot V_{\mathrm{O}} \cdot \Delta v_{\mathrm{o}}(s)}{R_{\mathrm{O}}} \quad \text{(A 25)}$$

$$\Delta p_{\mathrm{c}}(s) = C_{\mathrm{O}} \cdot V_{\mathrm{O}} \cdot s \cdot \Delta v_{\mathrm{o}}(s). \quad \text{(A 26)}$$

By putting (A24) – (A26) into (A23), (17) can be obtained.

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