Title : Manitoba Inverter – Single Phase Single-Stage Buck-Boost VSI Topology

Authors : Carl Ngai Man Ho (Corresponding author), *Senior Member, IEEE*
Ken King Man Siu, *Student Member, IEEE*

Address: University of Manitoba,
75 Chancellors Circle,
Winnipeg, MB, R3T 5V6,
Canada.

Tel. : +1 204 474 7061

Fax. : +1 204 474 7522

Email : carl.ho@umanitoba.ca

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Manitoba Inverter – Single Phase Single-Stage Buck-Boost VSI Topology

Carl Ngai Man Ho, and Ken King Man Siu

Abstract— The paper presents a new transformerless single-phase single-stage buck-boost grid-connected voltage source inverter (VSI) topology. The topology can achieve efficient power conversion with a wide input voltage range, number of magnetic devices reduction and low leakage current. The proposed VSI topology consists of high frequency semiconductors for shaping inductor currents, and low frequency semiconductors to form grid *CL* filter structure for different conditions. This *CL* filter uses the same buck-boost inductor, thus no additional line frequency inductor is required. Besides, Common Mode (CM) voltage, a main problem of transformerless grid-connected VSI, is mitigated, since the capacitor in the *CL* filter clamps the voltage between the grid and the bus terminal. The performance of the proposed VSI is experimentally verified. The results show that the proposed VSI guarantees sinusoidal output current and wide input voltage range, and has a good agreement with the theoretical findings.

Keywords— VSI, Buck-Boost, AVG, Common mode, Filter.

I. INTRODUCTION

Technology of single-phase (1-phase) grid-connected Voltage Source Inverter (VSI) has been rapidly developed in the last decade associates to the product development of uninterrupted power supply (UPS) [1] - [2], Photovoltaic (PV) inverter [3] and regenerative motor drive [4]. Advanced topology facilitates the increments of system efficiency and power density which leads researchers and engineers to propose and develop novel topologies. As well as efficiency and power density, material cost is another critical performance index to be minimized particular in low power products. Thus, topology is the fundamental component of a VSI to achieve optimal performance. And it is also the key to satisfy industrial standards for Power Electronics products.

Particularly for 1-phase transformerless PV inverters technology, most of low rated power (e.g. 1kW, 120V) PV inverters on the market are using two power stages, a dc-dc MPPT tracker and a VSI such as shown in the upper diagram of Fig. 1. Since output voltage of PV panel (e.g. 70V – 200V) in that low power range is sometimes not high enough to be over the peak value of grid voltage (e.g. 170V) [5]-[6]. It typically requires a boost converter to step up the voltage in a DC link (e.g. 250V - 400V) for a buck-type VSI to deliver power to the gird. Although the two-stage structure is straight forward for controller design and power processing, it is inefficient and bulky, as requiring two high frequency (HF) switching power stages to process the conversion. Besides, leakage current, which is led by HF Common Mode (CM) voltage, is generated if the topology or the modulation is not specifically designed for PV systems. Notice that leakage current is limited by industrial standards [7]-[8] due to safety and reliability issues. Therefore, some VSI topologies as second power stage in a transformerless 1-phase PV inverter have been proposed based on a buck-type full bridge inverter mainly for providing efficient switching and the leakage current reduction, such as H5 [9], Heric [10] and Active Virtual Ground (AVG) [11]. However the drawbacks are that they require more semiconductors in the circuit to disconnect or bypass the HF CM current path during the switching process. Although they solved the CM current problem, cost increases and the system efficiency are influenced, especially operating in a two-stage

power processing. Thus, single power stage topologies become attractive for low power transformerless products.

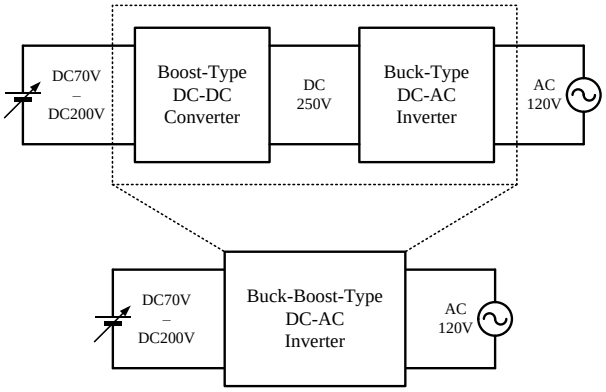


Fig. 1 Typical power inverter sturctures with a variable and low input dc voltage.

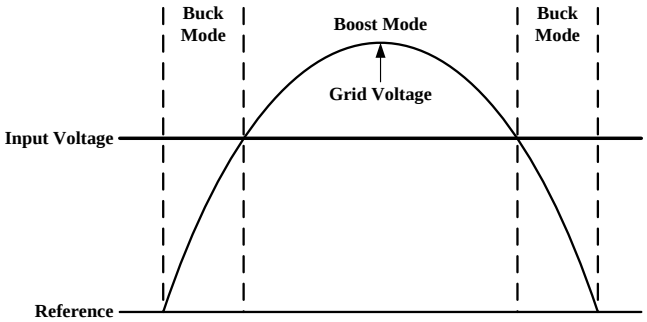


Fig. 2 Input and output voltages of a inverter and its operating modes.

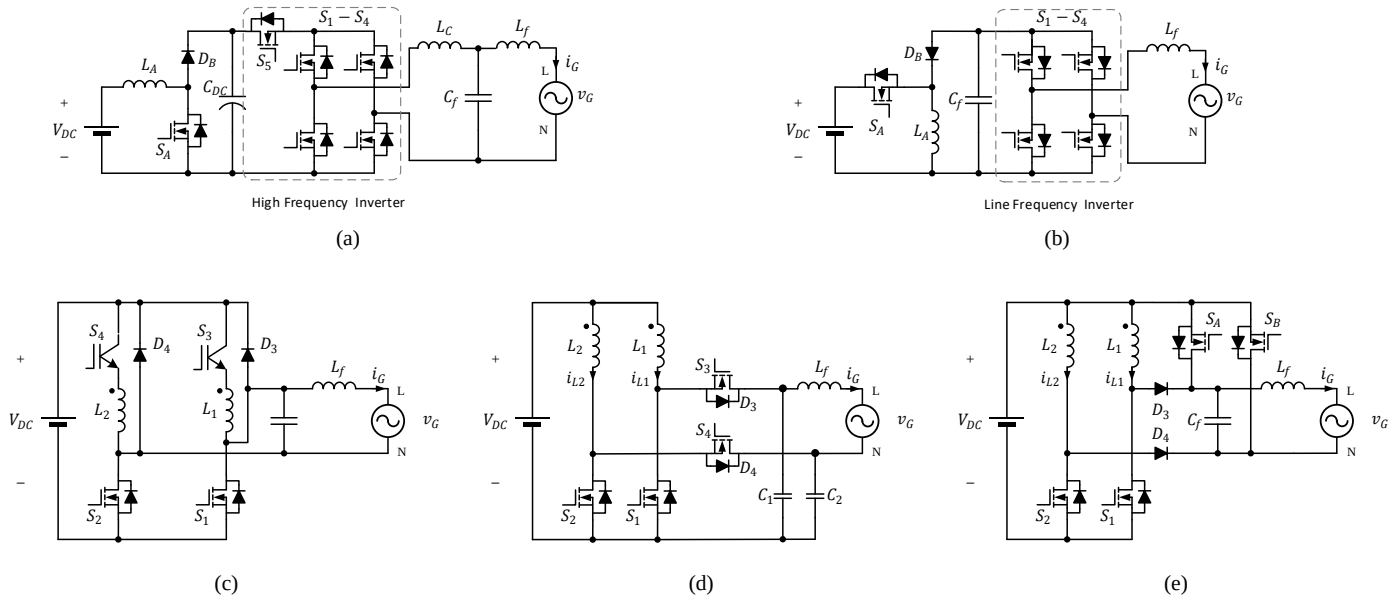


Fig. 3 The piror-arts of transformerless buck-boost inverter, (a) [5], (b) [14], (c) [18], (d) [19] and (e) [20].

TABLE I SUMMARIZE NUMBER OF SEMICONDUCTOR DEVICES AND PASSIVE COMPONENTS INVOLVED IN THE TOPOLOGIES

Topologies	No. of components in the circuit						No. of operating semiconductors	
	LF Switch	HF Switch	HF External Diode	Inductor	DC Cap	Filter Cap	Conducting in the main current path	Switching at the same time
Fig. 3a [5]	2	4	1	3	1	1	4	3
Fig. 3b [14]	4	2	1	2	0	1	3	1
Fig. 3c [18]	2	2	2	3	0	1	2	1
Fig. 3d [19]	0	4	0	3	0	2	2	2
Fig. 3e [20]	2	2	2	3	0	1	2	1
Fig. 4 (proposed)	4	2	0	2	0	1	2	1

A single power stage PV inverter requires a buck-boost-type dc-ac inverter such as shown in the bottom diagram in Fig. 1. A typical input and output voltage waveform is shown in Fig. 2. It shows that the inverter operates as buck mode when the input voltage is higher than the grid voltage and as boost mode when they are opposite. It creates challenges for designing a single stage inverter which can operate in the modes and satisfy the mentioned industrial standards at the same time. Fig. 3 shows some prior-art solutions including dual-stage and single-stage power processing. A summary of components count is shown in Table I which is used to indicate the major difference between those reviewed topologies. In Fig. 3 (a), it is a typical dual-stage topology [5], it requires a boost converter to create a high voltage dc link and uses a high frequency buck-type inverter, such as H5, Heric and AVG, to inject the power to the grid. There are two high frequency power stages in the system, high switching loss and high conduction loss are expected. There is another topology which is a time-sharing cascaded dual mode inverter [12] - [13]. On top of [5], a bypass diode is adding into the circuit which links up the DC input and the DC bus together. Based on the output voltage level, either boost conversion or buck conversion is applied. With the time-sharing technique, the number of high frequency switches are less in each half line cycle operation. The size of the DC link capacitor is reduced. However, the conduction loss is kept in a high magnitude as at least three semiconductors in the current path. Fig. 3 (b) shows a buck-boost converter with an unfolding inverter [14] - [15]. The buck-boost converter creates a rectified sinewave voltage across the filter capacitor and uses a line frequency inverter to convert it to a sinewave. Although only two high

frequency components are required, high conduction loss is created as three semiconductors in the current path. Sometimes a diode is in series to the switch in the line frequency inverter to ensure the reliability, it will furtherly increase to five semiconductors in the current path [16], [17]. In Fig. 3 (c), it consists of two individual buck-boost cells [18]. When the grid is in positive high cycle, switch S1 is at high frequency switching with freewheeling diode D4. The disadvantage is that it has at least two power semiconductors, e.g. S3 and S1, in the current path which will increase conduction losses of the converter. In Fig. 3 (d), it uses two boost converters to create two capacitor voltages and the difference of the converters makes sinusoidal output voltage and current [19]. This requires two high frequency converters operating at the same time, thus overall switching loss is high. Fig. 3 (e) shows a very interesting buck-boost inverter topology, it uses an additional switch to bypass an idle buck-boost switching cell for half line cycle [20]. It effectively steps up and down the voltage and clamps the CM voltage by the additional switches. However, the drawback is similar to other mentioned topologies, it is required a bulky filter inductor to filter out the high frequency components in the grid current, power density and cost are the issues. Other possible topologies have been well documented in the literature and they are based on the above five topologies with additional features [21] - [24].

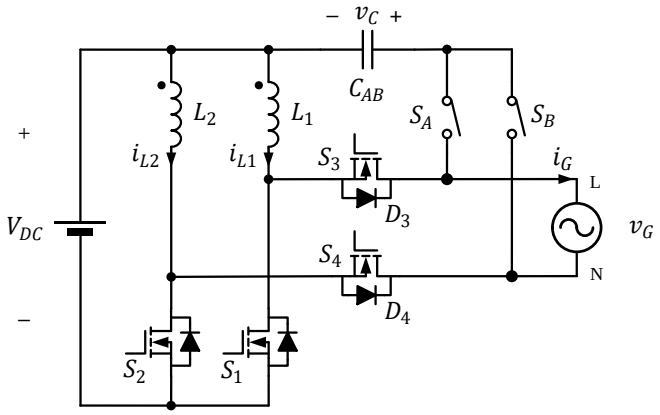


Fig. 4 The proposed Manitoba Inverter topology.

This paper proposes a new transformerless single-phase single-stage buck-boost grid-connected VSI circuit to transform DC voltage to AC voltage, namely Manitoba Inverter. The main advantages of the proposed topology are 1) wide input range with a single power stage, 2) sinusoidal continuous grid current and without

additional grid inductor requirement, 3) low CM voltage with transformerless design, and 4) only one switch under HF operation in each half line cycle. Since Manitoba Inverter is able to support very wide input DC voltage range, it is very promising for PV applications. In Fig. 4, it shows the proposed circuit. The VSI consists of two buck-boost switching cells and a configurable *CL* filter circuit. The switches for configuring the *CL* filter is based on the recently proposed AVG concept [11], [25]. The configurable *CL* filter circuit can change the output filter to different *CL* structures depending on grid voltage polarities by using the built-in buck-boost inductors. This approach eliminates a bulky grid inductor in the system. In addition, since the VSI uses the AVG concept, it mitigates the CM voltage issue by using the capacitor in *CL* filter to clamp the voltage between the grid and the positive terminal of DC bus. Thus, leakage current is minimized, it is important for PV inverters due to industrial standards [7]-[8]. In each switching cycle, only one switch is operating under high frequency switching and the others are under line frequency operation. Therefore the overall switching loss is minimized. In Table I, it can be seen that the proposed inverter can keep the minimum number count of HF semiconductors and passive devices, and the minimum number of semiconductors in the main current path and high frequency switching during operation. This paper will define the problems, explain operating principle of the proposed inverter, provide static characteristics, and use experimental results to verify the proposed concept. An 800W, 120V laboratory prototype has been implemented and is used to demonstrate the performance of the proposed topology.

II. PRINCIPLES OF OPERATION

The proposed buck-boost VSI is shown in Fig. 4, which is able to convert a DC bus voltage into an AC grid voltage either the DC bus voltage higher or lower than the peak value of AC grid and to deliver sinusoidal grid current to the grid. The circuit includes two buck-boost switching cells and a configurable *CL* filter circuit, namely AVG circuit. The configurable *CL* filter circuit filters out switching frequency components which are generated by the buck-boost cells, and issues a continuous sinusoidal current to the grid. The AVG circuit consists of two bi-directional switches (S_A and S_B), and they are connected to Line (L) and Neutral (N) of the grid separately. The bi-directional switches, namely AVG switches, can be realized by connecting two back-to-back low cost MOSFETs in series or in other configurations to provide bi-directional blocking and conducting. The AVG switches operate at line frequency and their gating actions are synchronized with the zero-crossing points of the grid voltage. The switches switch alternatively which are depending on the polarity of the grid voltage. The circuit also includes a capacitor (C_{AB}), namely AVG capacitor, that is coupled between the junction point of two bi-directional switches and the positive terminal of DC bus (V_{DC}). It is used to clamp the potential difference between the DC bus and the AC ground in order to minimize the CM voltage and it is used to form a *CL* filter as an output grid filter.

A. Operating Mode: Positive half line cycle

In Fig. 5 (a), the proposed buck-boost VSI works in positive half line cycle. In this half line cycle, C_{AB} is connected to Line (L) of the grid voltage through the bi-directional switch (S_A), the main switch (S_2) is always open and the main switch (S_1) is switching at a high frequency for shaping the inductor current i_{L1}. Fig. 6 (a) is the corresponding equivalent circuit of Fig. 5 (a), note that S_A and S_4 are always conducting and S_2 is always open in this half cycle thus they are not shown in the circuit. It can be seen that the inverter forms a buck-boost converter with L_1, and a *CL* filter is formed with C_{AB} and L_2 between the grid and the buck-boost converter. In this case, L_2 takes the role of grid inductor, then low grid differential mode (DM) current ripple is achieved.

The corresponding inductor current waveform is shown in Fig. 7. The equivalent circuit in Fig. 6 (a) is basically the same as that of Fig. 3 (b), there is only one semiconductor (S_4) in the grid current path in the proposed VSI, but there are two MOSFETs in the grid current path due to the use of unfolding inverter. Specifically for PV applications, a parasitic capacitor presents in between PV cells and AC ground. In Fig. 5 and Fig. 6 , a capacitor, C_{CM}, represents the parasitic capacitor of the system [11]. This capacitor is the main contributor of the HF leakage current when a HF potential difference changes across the capacitor. Thus, the voltage, v_{CM}, should be kept as stable and avoid to be affected by the switching actions in the main converter circuit. In the proposed system, C_{AB} is coupled between Line (L) and the positive terminal of DC bus, the CM capacitor voltage can be determined by,

$$v_{CM}(t) = v_G(t) - v_C(t) - V_{DC} \quad (1)$$

where v_{CM} is CM voltage, v_C is capacitor voltage of C_{AB}, and v_G is grid voltage with positive value.

According to (1), there are no high frequency voltage changes in the terms, the potential difference of the parasitic capacitor C_{CM} is clamped. Therefore, low HF leakage current is achieved. Furthermore, from the HF signals point of view, the impedance of the voltage source in (1) is very low, it looks like the DC bus terminal is connecting to the AC ground, therefore the technology is namely Active Virtual Ground (AVG) [11], [25].

B. Operating Mode: Negative half line cycle

In Fig. 5 (b), the proposed buck-boost VSI works in negative half line cycle. In this half line cycle, the AVG capacitor (C_{AB}) is connected to Neutral (N) of the grid voltage through the bi-directional switch (S_B), the main switch (S_1) is always open and the main switch (S_2) is switching at a high frequency for shaping the inductor current i_{L2}. Fig. 6 (b) is the corresponding equivalent circuit of Fig. 5 (b), note that S_B and S_3 are always conducting and S_1 is always open in this half cycle thus they are not shown in the circuits. As well as

the system in the positive half line cycle that the inverter forms a buck-boost converter with L_2, and a *CL* filter is formed with C_{AB} and L_1 between the grid and the buck-boost converter. In this case, L_1 takes the role of grid inductor, then low grid differential mode (DM) current ripple is achieved. The corresponding inductor current waveform is shown in Fig. 7. C_{AB} is coupled between Neutral (N) and the positive terminal of DC bus, the CM capacitor voltage can be determined by,

$$v_{CM}(t) = -V_{DC} - v_C(t) \tag{2}$$

According to (2), there are no high frequency voltage changes in the terms, the potential difference of the parasitic capacitor C_{CM} is clamped, therefore, low HF leakage current is achieved. However, $v_C(t)$ presents in the equation and it is a line frequency varying component, thus line frequency component presents in the CM voltage.

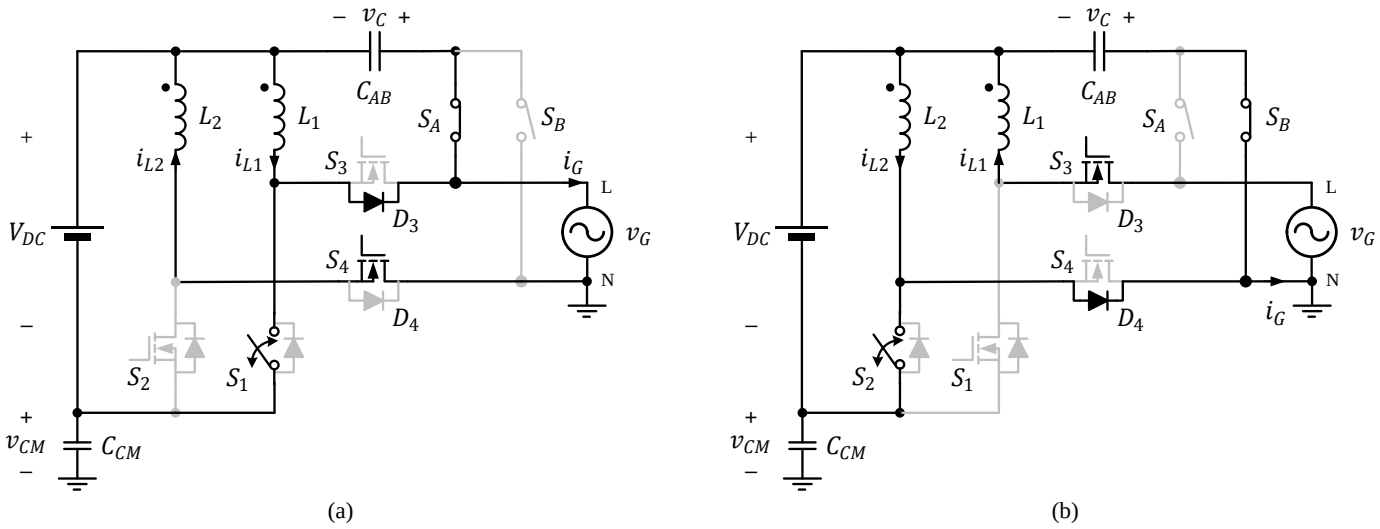


Fig. 5 Current conducting paths of the proposed VSI in (a) positive line cycle, and (b) negative line cycle.

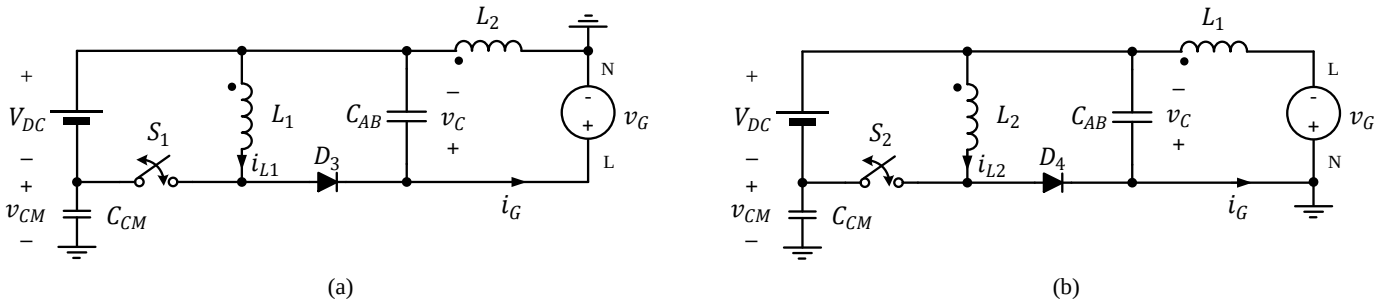


Fig. 6 Equivalent circuits of the proposed VSI in (a) positive line cycle, and (b) negative line cycle.

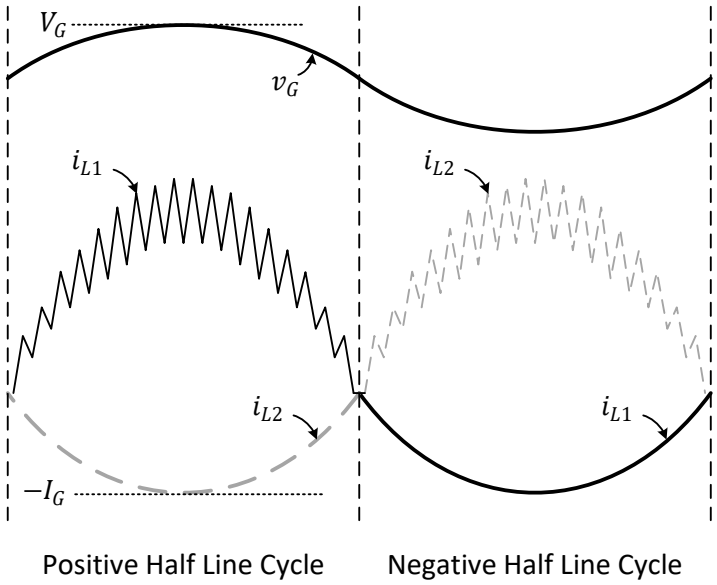


Fig. 7 Ideal inductor current waveforms.

III. STEADY-STATE CHARACTERISTICS

The equivalent circuits in Fig. 6 show that the system could be modelled as a simple buck-boost converter in each half line cycle, thus steady-state characteristics can be determined by using buck-boost converter characteristics with time varying output voltage and current. The corresponding characteristics waveforms are shown in Fig. 8.

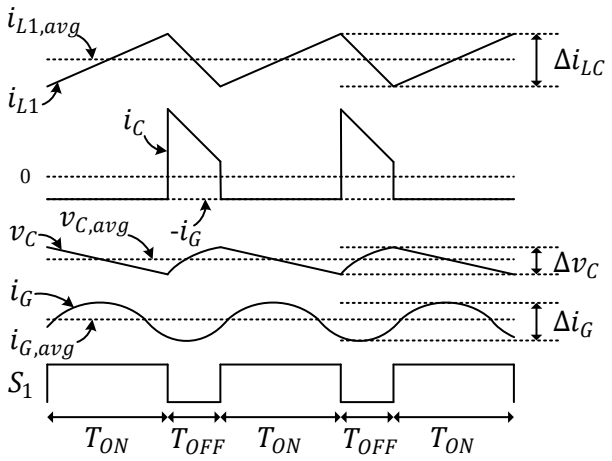


Fig. 8 Steady-Stage waveforms.

In order to simplify the topology analysis, the inductors are assumed as identical, thus,

$$L_X = L_1 = L_2 \tag{3}$$

where L_X is inductance of the inductors in the Manitoba Inverter topology.

By using the power flow transfer equation from v_C to v_G in Fig. 6, output power of the inverter can be obtained as,

$$P = \frac{V_C V_G}{\omega L_X} \sin \delta \tag{4}$$

where V_C and V_G are the peak amplitude of capacitor (C_{AB}) voltage and grid voltage, respectively, ω is the angular line frequency and δ is the relative phase angle between the two voltage sources.

A. Grid Votlage and AVG Capacitor Voltage

It can be seen that from (4), δ is proportional to the inductance if the transferring power is constant. The inductor is half line cycle working as a grid inductor and half line cycle working as a buck-boost converter inductor, the value is typically in micro-Henry (μH) scale. Thus, the phase angle is small and the voltage drop on the grid inductor can be neglected in order to simplify the calculations. By assuming the AVG capacitor voltage v_C is almost the same as the rectified grid voltage. It can expressed as,

$$v_C(t) \approx |v_G(t)| = V_G|\sin \omega t| \tag{5}$$

B. Grid Current

The control objective of grid-connected inverter is to inject power to the grid and to keep the output current is in-phase with the grid voltage, thus the grid current can be expressed as,

$$i_G(t) = I_G \sin \omega t \tag{6}$$

where I_G are the peak amplitude of grid current.

C. Duty Ratio

Fig. 6 shows the buck-boost converter transferring energy from the DC source to the AVG capacitor. The operation of the inverter is the same as a simple buck-boost converter. Thus, the duty ratio *D* can be expressed by,

$$D(t) = \frac{|v_G(t)|}{|v_G(t)|+V_{DC}} \tag{7}$$

It shows that the duty ratio is time varying in a line cycle following the change of grid voltage.

D. Low Frequency Buck-Boost Inductor Current

The inductor energy is transferring to the grid during the OFF-state operation as shown in Fig. 9 (b). During the steady state situation, the OFF-state inductor current will equal to the average grid current over a completed duty cycle. Therefore the low frequency buck-boost inductor current, $i_{LC}(t)$, can be expressed as,

$$i_{LC}(t) = \frac{|v_G(t)||i_G(t)|(|v_G(t)|+V_{DC})}{V_{DC}|v_G(t)|} \tag{8}$$

E. Buck-Boost Inductor Current Ripple

By making assumptions that the inverter works with a constant switching frequency and continuous-conduction mode inductor current, the converter-side current ripple Δi_{LC} can be found from the inductor ON-state equation as following,

$$v_{LC} = L_X \frac{\Delta i_{LC}}{T_{ON}} \tag{9}$$

where v_{LC} is the voltage across the switching inductor and T_{ON} is the turn-on period in a switching cycle,

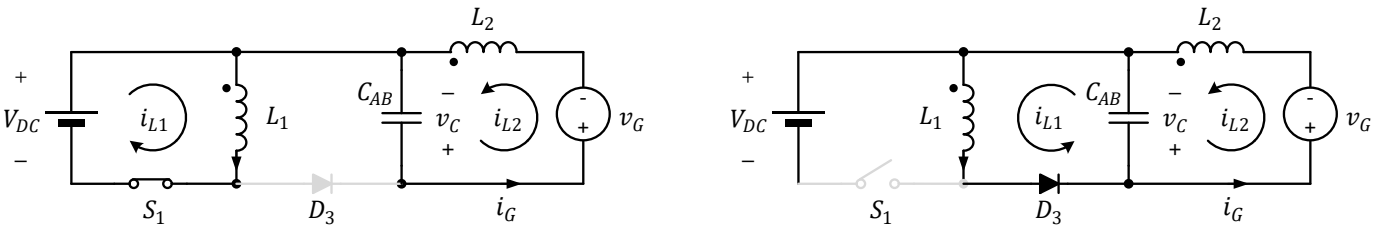
As shown in Fig. 9 (a), v_{LC} is equal to V_{DC} during the ON-state operation. By using the relationships between the duty ratio D, the switching frequency f_{sw} and the time period and T_{ON}, the buck-boost inductor current ripple can be determined as,

$$\Delta i_{LC}(t) = \frac{V_{DC}D(t)}{L_X f_{sw}} \tag{10}$$

And by putting (7) into (10), the instantaneous inductor ripple equation of Δi_{LC} can be obtained as,

$$\Delta i_{LC}(t) = \frac{1}{L_X f_{sw}} \frac{|v_G(t)|V_{DC}}{|v_G(t)|+V_{DC}} \tag{11}$$

It shows that the current ripple size is time varying in a line cycle.



(a) (b)

Fig. 9 Operating modes of a buck-boost converter, (a) ON-state Mode and (b) OFF-state Mode.

F. AVG Capacitor Voltage Ripple

The voltage ripple of AVG capacitor is created by charging the capacitor with the discontinuous diode current. The buck-boost inductor releases the current to the capacitor during the OFF-state of the HF switching switch. During the ON-state, the capacitor current is the same as the grid inductor current which can be simplified as a constant current in a short switching period. Thus, the capacitor voltage ripple peak to peak value Δv_C is defined as,

$$i_C = C_{AB} \frac{\Delta v_C}{T_{ON}} \tag{12}$$

where i_C is current of AVG capacitor.

$$\Delta v_C(\mathrm{t}) = \frac{D(t) \cdot |i_G(t)|}{C_{AB} f_{sw}} \tag{13}$$

By putting (7) into (13), the following equation can be obtained.

$$\Delta v_C(\mathrm{t}) = \frac{|v_G(t)||i_G(t)|}{|v_G(t)|+V_{DC}} \frac{1}{C_{AB} f_{sw}} \tag{14}$$

It shows that the voltage ripple size is time varying in a line cycle.

G. Grid Inductor Current Ripple

From the *CL* filter characteristic, the grid side inductor will face the same high frequency voltage ripple as the one appeared on the AVG capacitor. As shown in Fig. 8, the capacitor ripple voltage is much closed to a triangular wave. Therefore under triangular wave approximation, the grid inductor current ripple, $\Delta i_{LG}(t)$, can be expressed as,

$$\Delta i_G(t) \approx \frac{\Delta v_C(t)}{8 \cdot L_X \cdot f_{SW}} \tag{15}$$

By putting (14) into (15), the following equation can be obtained.

$$\Delta i_G(t) \approx \frac{1}{8 C_{AB} L_X f_{sw}^{\ 2}} \frac{|v_G(t)||i_G(t)|}{|v_G(t)|+V_{DC}} \tag{16}$$

It shows that the grid current ripple size is smaller than the buck-boost inductor current ripple and also time varying.

H. High Frequency CM Voltage Amplitude

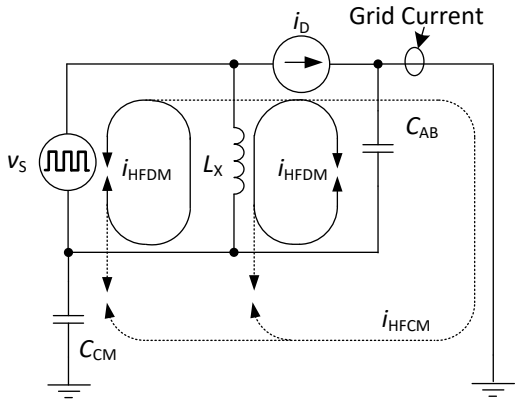


Fig. 10 High frequency equivalent model.

By applying the high frequency analysis to Fig. 6, the corresponding high frequency equivalent model is generated as shown in Fig. 10. On the model, a capacitor, C_{CM}, is used to represent the parasitic capacitor between the Earth and the Negative bus terminal of the inverter. The voltage generated on the C_{CM} presents the

CM voltage and the current passing through C_{CM} is defined as the leakage current. In the analysis model, C_{CM} is always paralleled to the filter capacitor C_{AB}, there CM voltage ripple is guaranteed as the filter capacitor helps to clamp the potential difference between the DC bus and the AC ground. By modifying (14), the CM voltage, $\Delta v_{\mathrm{CM}}(t)$, can be expressed as,

$$\Delta v_{\mathrm{CM}}(t) = \frac{|v_G(t)||i_G(t)|}{|v_G(t)|+V_{DC}} \frac{1}{(C_{AB}+C_{CM})f_{sw}} \tag{17}$$

I. Leakage Current Amplitude

From Fig. 8, it shows that a discontinuous current is passing through the filter capacitor current in every completed switching cycle. As C_{CM} is paralleled to $C_{AB,}$ the leakage current amplitude, $\Delta i_{\mathrm{CM}}(t)$, that appears in C_{CM} can be found under the current divider theory as,

$$\Delta i_{\mathrm{CM}}(t) = \frac{C_{\mathrm{CM}}}{C_{\mathrm{AB}}+C_{\mathrm{CM}}} (i_{LG}(t) + \frac{\Delta i_{LG}(t)}{2}) \tag{18}$$

By putting (11) and (16) into (18), the following equation can be obtained.

$$\Delta i_{CM}(t) = |v_G(t)||i_G(t)| \frac{C_{CM}}{C_{AB}+C_{CM}} (\frac{1}{V_{DC}|v_G(t)|} + \frac{1}{16C_{AB}L_X{f_{sw}}^2(|v_G(t)|+V_{DC})}) \tag{19}$$

The capacitor value of C_{AB} is always much larger than the capacitor value of C_{CM}, therefore the leakage current amplitude is able to minimize into a small level.

IV. System Design and Implementation

A. *Varients of Topology*

Fig. 4 is one topology of the Manitoba Inverter topology family. The family is defined as a buck-boost inverter using the AVG circuit which can create the equivalent circuits as Fig. 5. Another topology example is shown in Fig. 11. The functionality of the circuit is the same as Fig. 4. However the circuit is mirrored, the inductors connect to the negative terminal of the DC input source. Other variants can be using separated two capacitors instead of one C_{AB}, each capacitor is in series with one AVG switch (S_A or S_B) . Nevertheless, all variants of the Manitoba Inverter would provide similar electrical performance.

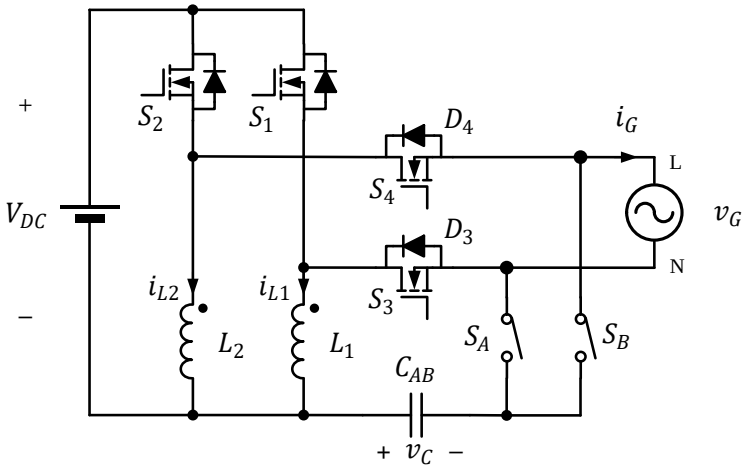


Fig. 11 Mirrored topology of Fig. 4.

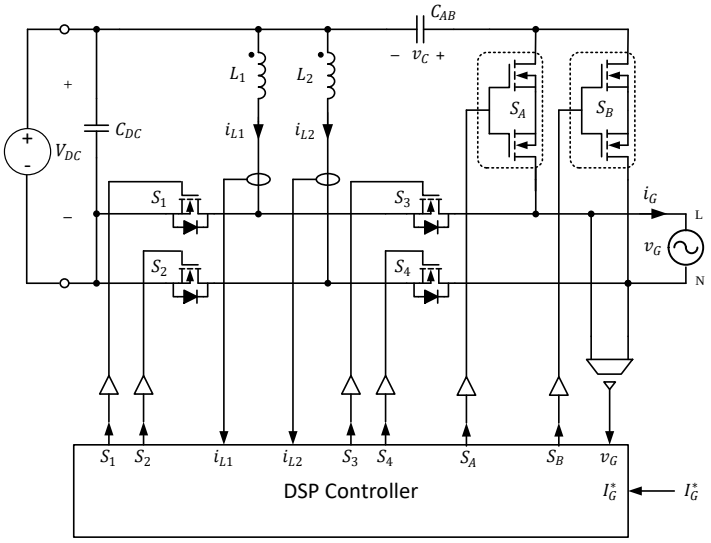
B. *System Implmentation*

An 800W, 120V AC output buck-boost grid-connected VSI prototype has been implemented to evaluate the proposed topology in Fig. 4. Table II shows the specification and key parameters of the prototype. The prototype is used to verify the operating principle and feasibility of the proposed topology. The prototype can manage a wide input dc voltage range from 60 V to 200V, which covers the range of lower and higher of the output voltage peak value (170V). Fig. 12 (a) shows the connection block diagram of the prototype. There are 6 gate signals from the DSP, and two inductor current and grid voltage sensing signals to the DSP for control

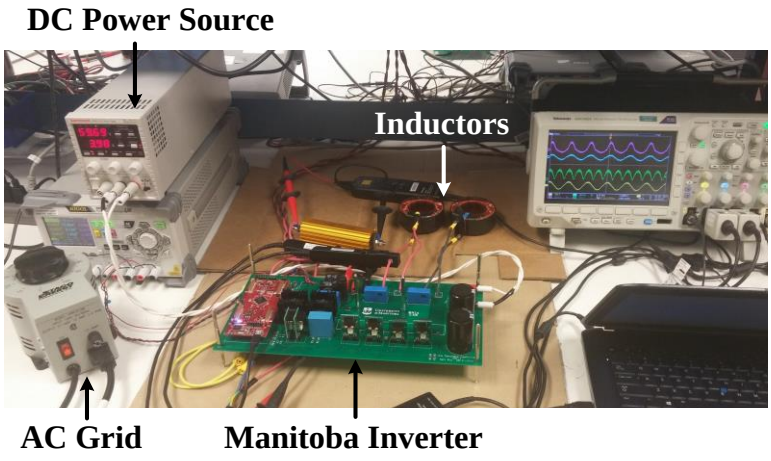
and protection purposes. Fig. 12 (b) shows the single PCB Manitoba Inverter prototype and the experimental setup in the laboratory.

TABLE II
SPECIFICATION OF THE PROTOTYPE OF MANITOBA INVERTER

Parameter	Value	Parameter	Value
Input DC Voltage	60 – 200 V	Grid AC Voltage	120 V (60 Hz)
Max. Output Power	800 W	Switching Frequency	20 kHz
L_1 & L_2	780 µH	C_{AB}	6.8 µF



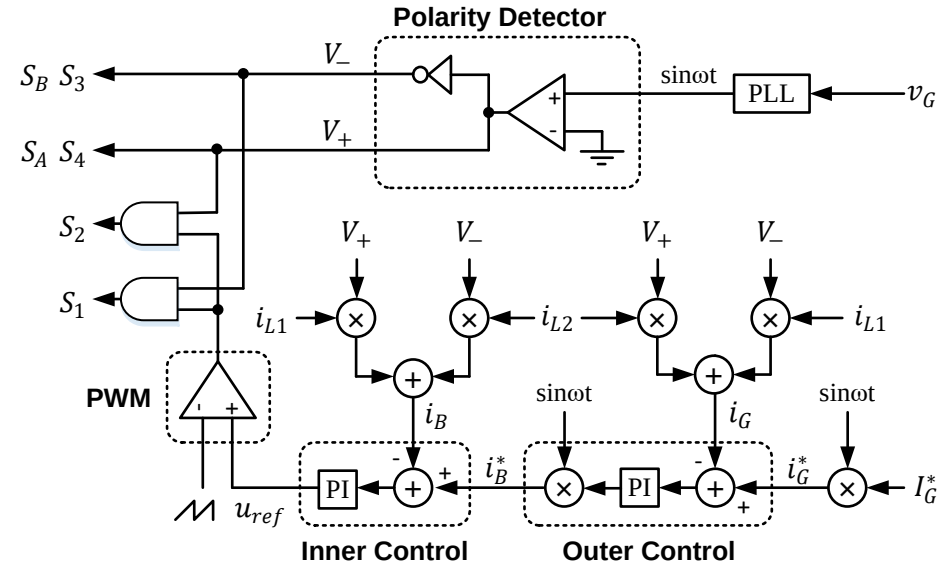
(a)



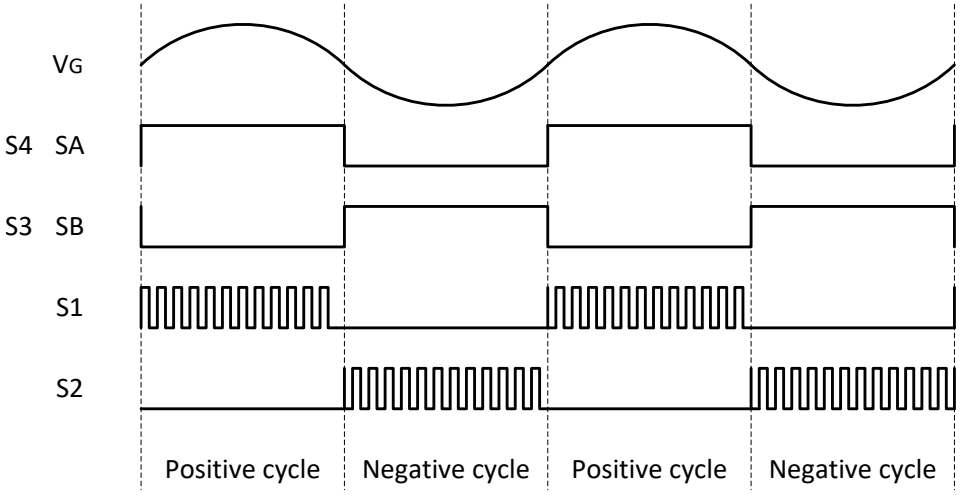
(b)

Fig. 12 Testbed, (a) connection block diagram, and (b) laboratory setup.

C. Controller Design



(a)



(b)

Fig. 13 Control and modulation, (a) Controller block diagram, and (b) Gate signals.

The roles of inductors L_1 and L_2 are interchanged in every half line cycle as buck-boost inductor and grid inductor, thus additional line filter inductors are not required in the topology. Furthermore, only two current sensors are required for providing current signals to the controller. Fig. 13 (a) shows a simplified control block diagram of the proposed Manitoba Inverter topology. There are two control loops in the system with Proportional Integral (PI) controllers. The outer loop is to regulate the grid inductor current to be sinusoidal

and to synchronize with the grid voltage, and the inner loop is to control the buck-boost inductor current to balance the input and output powers in the inverter. The inner loop is running in high control bandwidth so that a precise accurate switching action is resulted. The outer loop operates under a low frequency control which only requires to synchronize the grid current and grid voltage in line frequency domain. To avoid the interaction in both current loops, the loop frequency is set with a 5 times difference between both loop. The parameter of the controller is set based on the target cut off frequency point.

The gate signals of AVG switches are obtained by a simple polarity detector by sensing the grid voltage. Fig. 13 (b) shows simplified gate signals for the switches in the proposed Manitoba Inverter topology. It can be seen that there is always only one switch working in high frequency switching, others operate at line frequency switching and change states at the zero crossing of the grid voltage. Therefore, the semiconductor switching losses can be minimized.

D. Selection of Filter Compoment

In every half line cycle, one of the inductors acts as the converter-side inductor for energy conversion. The other one acts as the grid-side inductor to form a *CL* filter with the capacitor C_{AB}. With the use of (11) and a predefined current ripple magnitude, the converter inductance is found. In the prototype, a 7.8mH inductor is to limit the current ripple into 6A. On the selection of filter capacitor, there are two major concerns. One is the resonant frequency, f_{res}, which is defined as (20).

$$f_{res} = \frac{1}{2\pi\sqrt{L_x \cdot C_{AB}}} \tag{20}$$

In order to avoid the interaction between resonant frequency and switching frequency, the resonant frequency is required 10 times lower than the switching frequency. Another criteria is the magnitude of leakage current which is defined in (11). In order to meet the standard requirement [7], the magnitude of leakage current needs to be within 300mA. To fulfill both criteria, a 6.8μF capacitor is selected in the prototype.

E. Selection of Semiconductor

The switches S_A and S_B for configuring the *CL* filter are implemented by two back-to-back connecting MOSFETs, the main switches S_1 and S_2 are Si MOSFETs, and S_3 and S_4 are IGBTs with antiparallel SiC Diodes. This combination of semiconductors can form fast switching cells to give efficient switching. In order to optimize the design, components losses in the converter are estimated. Reference to [5], semiconductor and inductor losses are the key components that require special attention. Table III shows the selected semiconductors in the presented prototype. Also a chart of loss estimation during 130Vdc-600W is given in Fig. 14 as a design reference.

TABLE III
SEMICONDUCTORS IN THE PROTOTYPE

Switch	Type	Manufacturer	Part Number
$S_1 \sim S_2$	Si MOSFET	Infineon	IPW60R070P6
$S_3 \sim S_4$	IGBT + SiC Diode	STMicroelectronics	STGW30H60DFB
S_A & S_B	Si MOSFET	Infineon	IPW60R070C6

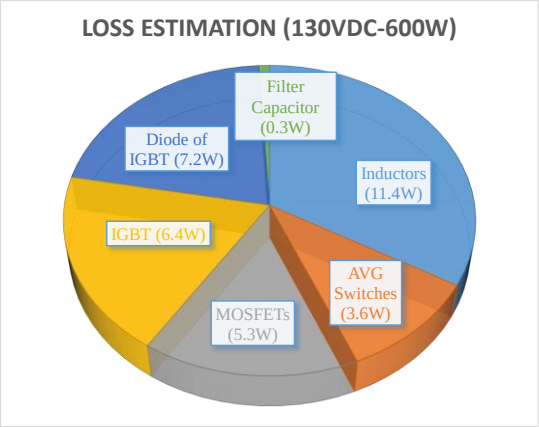
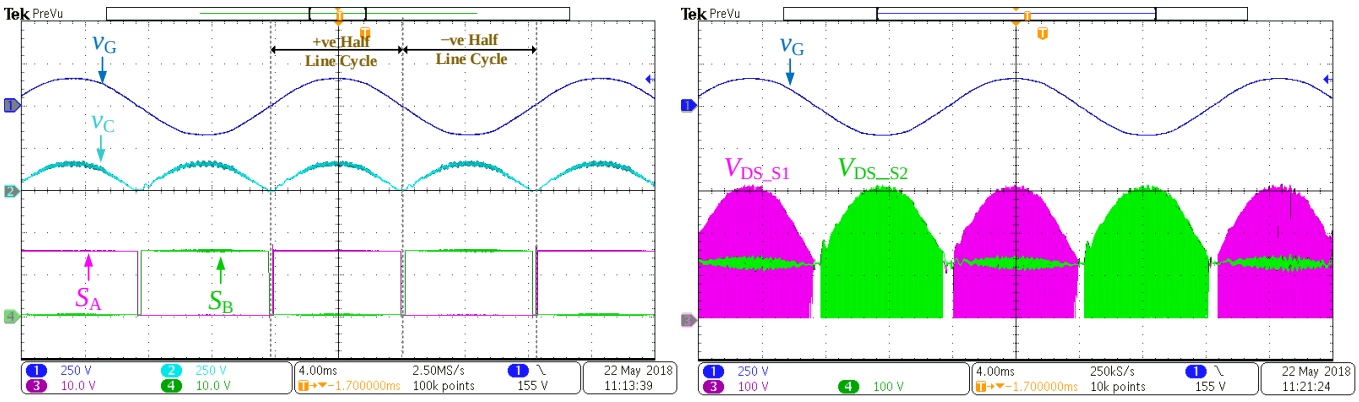


Fig. 14 Loss estimation in 130Vdc-600W.

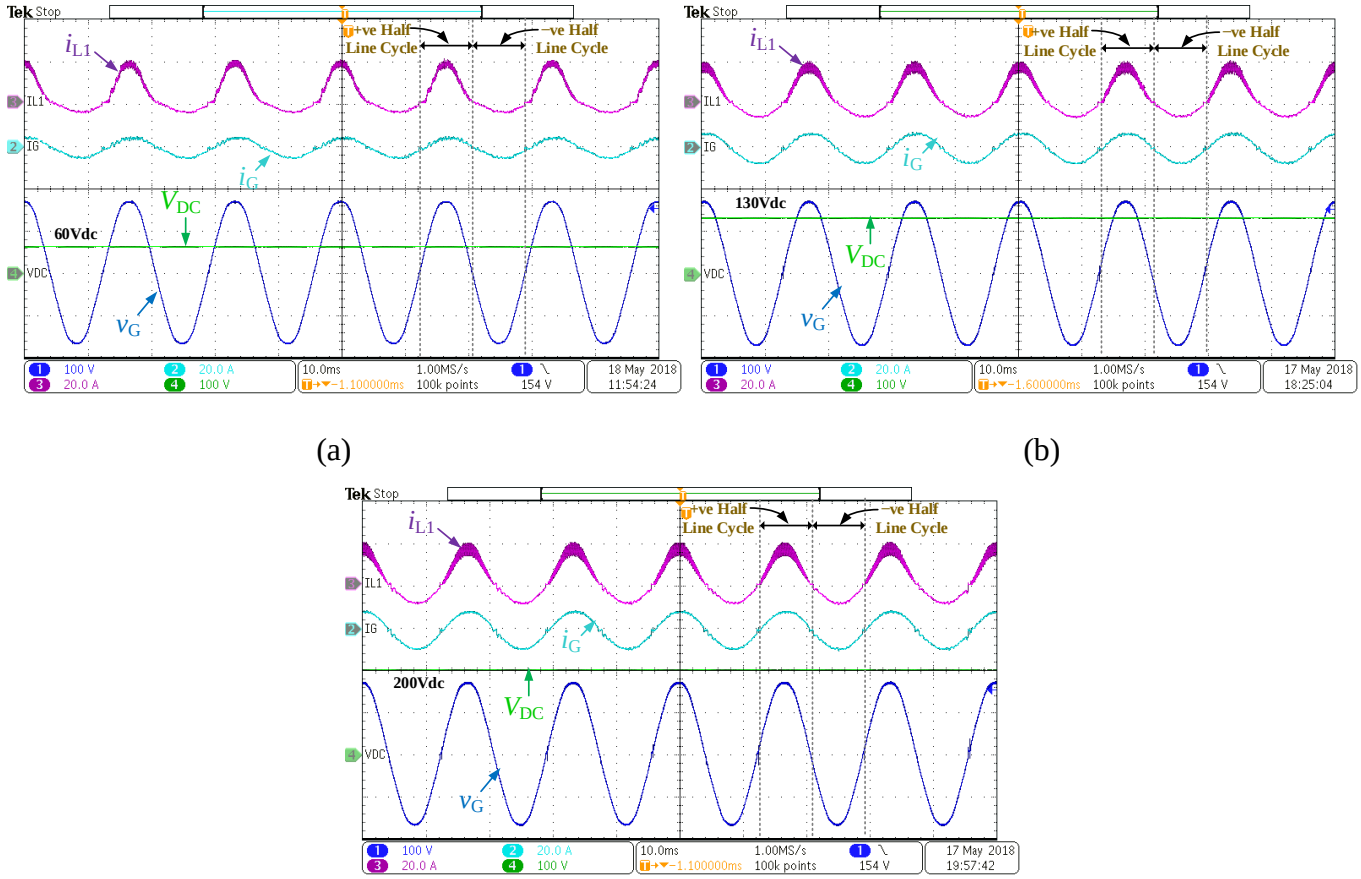
V. EXPERIMENTAL VERIFICATIONS

Fig. 15 and Fig. 16 shows experimental results of the proposed buck-boost VSI. The waveforms show the gate signals of S_A and S_B are synchronized with the grid voltage and switching alternately as shown in Fig. 15 (a). There is a short dead time at the grid voltage zero-crossing to avoid shoot-through issue between S_A and S_B. The capacitor, C_{AB}, voltage is a rectified sinewave, since the polarity of the capacitor is changed in every half line cycle. It can be seen in Fig. 6 (a) and (b), the capacitor is always connecting to the "Positive Terminal" of the grid. According to the buck-boost characteristic, the voltage stress on S_1 and S_2 are equal to the sum of input and output voltage which is shown in Fig. 15 (b).



(a) (b)

Fig. 15 Experimental results, (a) gating signals of S_A and S_B and (b) drain to source voltage waveforms of S_1 and S_2 at 130V dc input.



(a) (b)

(c)

Fig. 16 Experimental results, (a) 60V dc input, (b) 130V dc input, and (c) 200V dc input.

Fig. 16 (a), (b) and (c) show experimental results of the prototype working with different input DC voltage levels and power levels, they are 60Vdc – 400W, 130Vdc – 600W, and 200Vdc – 800W, respectively. The corresponding current reference of Fig. 16 (a), (b) and (c) are 3.3A, 5A and 6.6A, respectively. The maximum inductor current is limited to 20A. Fig. 16 (a) shows the VSI prototype is in the buck-boost mode, the input DC voltage is lower than the peak value of grid voltage. The grid current, i_G, is controlled as sinusoidal current with small current ripple. The inductor current is an asymmetrical waveform, it is because inductor are changing roles in the positive and negative line cycles which can be seen in Fig. 6 (a) and (b). During the positive half line cycle, L_1 is the buck-boost inductor, it is charged up energy from the DC source and releases the energy to the capacitor, C_{AB}. Since it is a discontinuous process for the input source and the capacitor, the inductor current amplitude is higher than that of the grid current. During the negative half line cycle, L_1

becomes the grid inductor. Thus the inductor current waveform of L_1 is identical to the grid current in the negative half line cycle. Fig. 16 (b) shows similar experimental results, but with higher voltage and higher power values. The grid current can keep as a sinewave. Fig. 16 (c) shows the VSI prototype is in the buck mode, the input DC voltage is higher than the peak value of grid voltage. The grid current, i_G, keeps as sinusoidal current. The inductor current ripple in positive half cycle is larger than that in buck-boost mode. This is because the voltage across the inductor is larger, di/dt of the inductor current is larger as well. Thus the current ripple becomes larger with the same switching frequency. The experimental results show that the proposed system works well with wide input voltage and ensures high quality grid current output. The results also show the prototype can deliver energy from the DC source to the grid no matter what input voltage level. Moreover sinusoidal output current is provided. In order to verify the accuracy of the proposed control loop, current references are also extracted from the controller to compare with the measured current waveforms, as shown in Fig. 17. From the figure, it shows that the measured one and the reference one are synchronized in both frequency and magnitude which results a stable control.

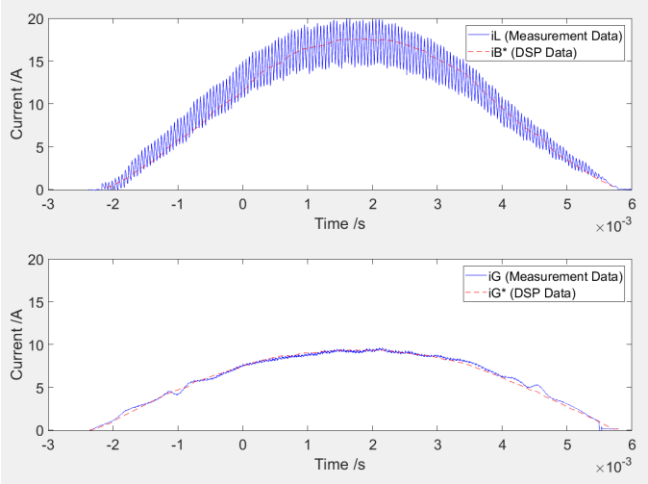


Fig. 17 Comparison between measurement signals and controller reference signals.

An efficiency curve is provided in Fig. 18 with varying testing conditions. In the measurement, only the converter stage is taken into the consideration. The auxiliary power is excluded in the measurement. It demonstrated that the system design is optimized from the medium voltage to high voltage scale, (130V dc to

200V dc). At the full loading condition of 130V dc, 93.7% system efficiency was achieved. The power factor was kept higher than 0.98. The voltage harmonic was 1.31% and the current harmonic was 4.71%. During 20% loading condition of 200V dc, the efficiency can be up to 95.7%. In addition, at the full loading condition of 200V dc, 93.82% system efficiency was able to achieve. The power factor was also kept higher than 0.98. The corresponding voltage harmonic was 1.34% and the corresponding current harmonic was 4%. The highest system efficiency for the prototype was 95.7% which appeared in 20% loading condition. A details current harmonic spectrum of the system operating in the buck-boost mode (130Vdc) and the buck mode (200Vdc) are shown in Fig. 19 (a) and (b) respectively. In all cases, the current quality satisfies the IEEE 519 standard.

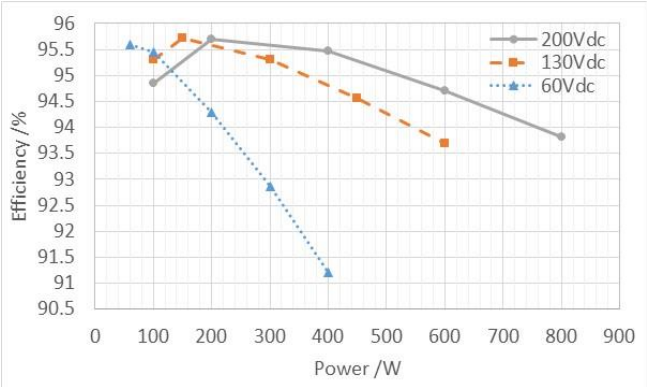
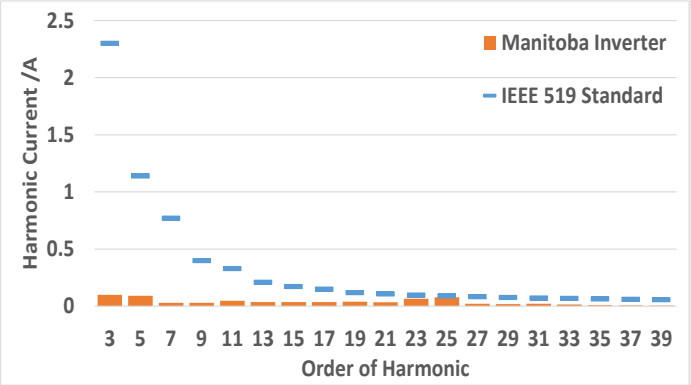
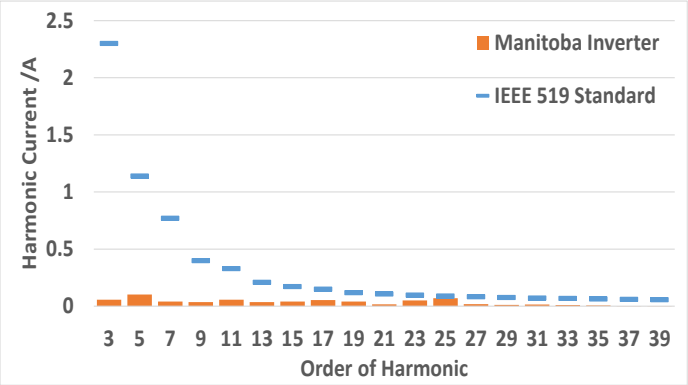


Fig. 18 System efficiency graph.



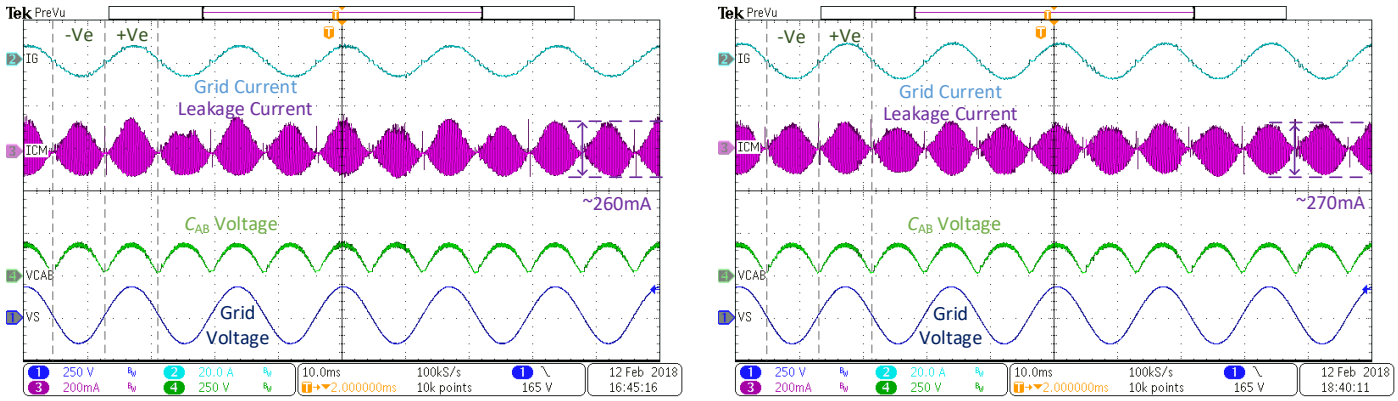
(a)



(b)

Fig. 19 Current Harmonic specturms, (a) 130V dc input and (2) 200V dc input.

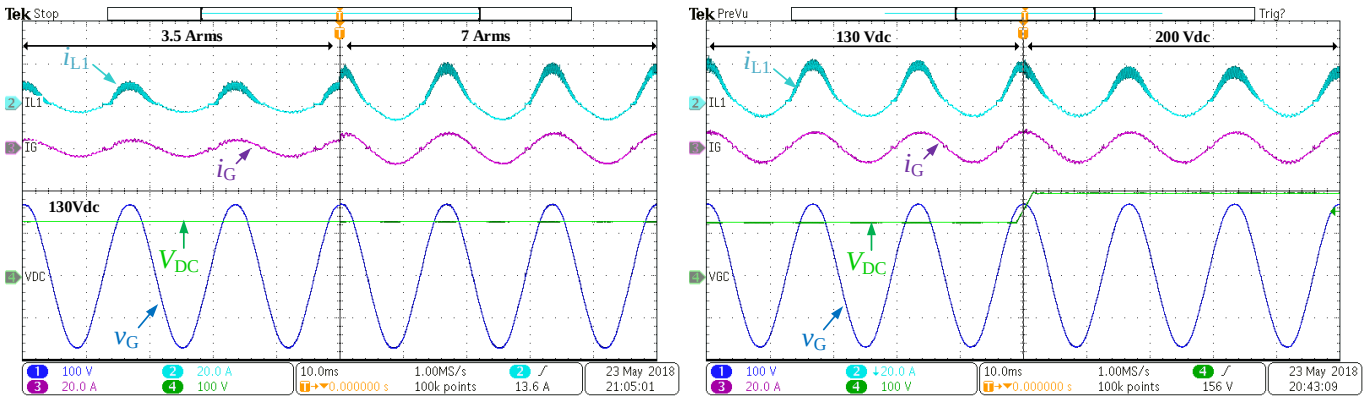
Fig. 20 (a) and (b) show the leakage current measurement of the inverter under the full loading condition in the 130V dc and 200V dc. A 100nF capacitor is added to the testbed to simulate the parasitic capacitor C_{CM} of the inverter. In both case, the leakage current level were also close to the expected value and were within the standard requirement of 300mA [7]. Low CM voltage and low leakage current is able to be guaranteed by the proposed topology.



(a) (b)

Fig. 20 Leakage current measurements, (a) 130V dc input and (b) 200V dc input.

Fig. 21 (a) and (b) show the transient performance of the proposed inverter under different testing conditions. In Fig. 21 (a), the reference of grid current was changed from 3.5 A to 7 A with a smooth transient action. Afterwards, grid current was quickly settled into a new targeting value under the proposed control scheme. In Fig. 21 (b), input voltage was jumped from 130Vdc to 200Vdc. Grid current wasn't influenced during the transient action. The only variation was shown in inductor current as it related to input voltage magnitude. In both situations, system can keep stable and provide a fast dynamic response during transient period. A stable system is able to be guaranteed.



(a) (b)

Fig. 21 Transient waveform, (a) step change in input voltage and (b) step change in grid current reference.

VI. CONCLUSIONS

The paper presented a new transformerless single-phase single-stage buck-boost grid-connected VSI topology. The VSI guaranteed the performance with small grid current ripple, low leakage current, a wide input voltage range, no additional grid inductor, and only one high frequency switch operates in the process. The concept is to use a low frequency switching circuit to reconfigure the *CL* filter in positive and negative half line cycles. Since the filtering capacitor always connects between the DC link and one of the grid terminals, the high frequency common mode voltage is minimized. The switching states of the proposed topology were explained in details. The performance of the VSI was demonstrated by experimental results. It showed that there is a good agreement between the concept and the experimental results.

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