A Four-Quadrant Single-phase Grid-connected Converter with only Two High Frequency Switches

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Post Conference Paper

***Abstract*— This paper presents a new four-quadrant boost type converter with the use of Active Virtual Ground (AVG) technology. The presented topology can step up the ac grid voltage to a regulated dc voltage under a stable bidirectional current flow and support the power transmission in either real power or reactive power delivery. With the use of the proposed modulation method, only two high frequency switches are required through the four-quadrant operation. Under a full bridge converter structure, an efficient system can be guaranteed. Also, benefiting from the AVG technology, a *LCL* filter is formed at the system input over the four-quadrant operation. Both magnitude of leakage current and grid current ripple are also minimized into a small value. Thus, a high efficiency and low noise four-quadrant converter is guaranteed. The presented topology is successfully implemented on a 750 VA prototype and the performance is experimentally verified on it which shows good agreement with the theoretical knowledge.**

***Index Terms*—Power Factor Correction, Reactive Power, Bidirectional Converter**

I. INTRODUCTION

RECENTLY, controlling reactive power plays an important role in power applications for smart grids. Especially, in a Plug-In Electric Vehicle (PEV) system, by using a bidirectional rectifier charger, it is able to support both grid-to-vehicle and (G2V) and vehicle-to-grid (V2G) applications for both charging and discharging operations. The V2G function can help to optimize the energy distribution over a power transmission system. Thus, the cost of an energy distribution system is lower as the system offers more flexibility in energy delivery and more stability in available energy capacity [1] - [3]. Meanwhile, in smart homes and smart grids, [4] - [6], sometimes a certain percentage of reactive power (Q) may be generated. They are caused by the connection of reactive electrical loads, such as motor or fluorescent lamps with inductive ballast. With the use of a four-quadrant (4Q) converter, these reactive powers can be compensated. A better grid power quality is achieved with a unit power factor through the overall system and a more efficient power transmission system is obtained.

In the past few years, many researchers and scientists have been working on the 4Q converter designs. Some soft switching isolated ac-dc converter solutions were presented in [7], [8] with the aim of high efficiency and low common mode (CM) noise. However, transformer is required and the soft switching control lets the system design become more complicated. Generally, the non-isolation type 4Q converters are built by different kinds of full bridge converter designs [9] - [22]. In order to generate a low leakage current system in the conventional full bridge converter, as shown in Fig. 1 (a), 2-level switching scheme is usually applied on it [9] - [11]. Under bipolar switching scheme, reactive power injection is achieved and the system leakage current can be maintained in a small value. However, high switching losses appear in those devices which limit the increment of system efficiency. At the same time, a fast recovery diode is required for all the high frequency (HF) switches which will limit the selection of devices. IGBT is one of the options, but the tail current limits the maximum switching frequency of the converter. Totem pole converter [12], [13], as shown in Fig. 1 (b), is another possible solution on a 4Q converter design. The topology is in a simple structure and the resultant CM noise is minimized. Compared to other topologies, the switching pair of totem pole converter is always kept in the left leg. Therefore the power dissipation per HF device is higher. Also shoot-through issue and reverse recovery problem are required to be considered in the selection of devices. In this case, MOSFET is only suitable for discontinuous mode or critical mode operation. Thus, for a high frequency application, the latest wide-bandgap semiconductor, GaN HEMT, would be required. Half bridge dual buck system, [14], is another reactive power solution which is shown in Fig. 1 (c). The working principle is similar to a half bridge converter where each inductor is only responsible to handle the power conversion in half of the line

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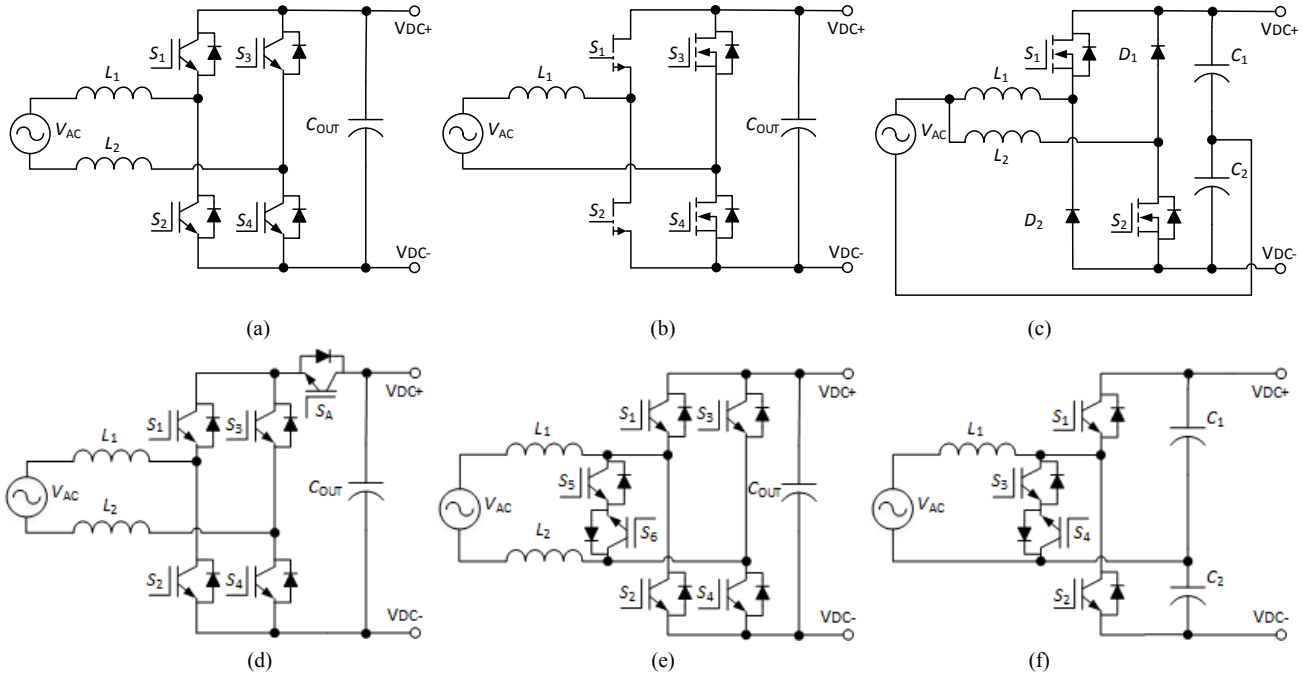


Fig. 1. Different kinds of four-quadrant (4Q) converter, (a) full bridge, (b) Totem pole, (c) half bridge dual-buck, (d) H5, (e) Heric and (f) Conergy-NPC.

TABLE I
SUMMARY OF NUMBER OF SEMICONDUCTOR DEVICES AND PASSIVE COMPONENTS INVOLVED IN THE TOPOLOGIES

Topology	No. of Switches			No. of Diodes	No. of components in the main current path (rectifier mode)		I/P filter	O/P Capacitor
	HF and need freewheeling diode	HF and need not freewheeling diode	LF		Turn-on	Turn-off		
Fig. 1 (a)	4	0	0	0	2	2	*L*	*C*
Fig. 1 (b)	2	0	2	0	2	2	*L*	*C*
Fig. 1 (c)	0	2	0	2	1	1	*L*	*2C*
Fig. 1 (d)	5	0	0	0	2	3	*L*	*C*
Fig. 1 (e)	6	0	0	0	2	2	*L*	*C*
Fig. 1 (f)	4	0	0	0	2	1	*L*	*2C*
Fig. 2	0	2	10	0	2	2	*LCL*	*C*

cycle. Although only two active switches are required, however a higher breakdown voltage is required. Meanwhile, the utilization of devices are lower than others topologies. H5, as shown in Fig. 1 (d), is another topology that supports with reactive power injection. It provides an effective power conversion and is electrically isolated the system from CM noise. Based on the foundation of [23] and [24], a reactive power modulation scheme was proposed in [15], [16]. However, one more switch is involved in the current conduction path which results in higher conduction loss than others. Similar to H5, there are another two types of converters which is called H6 [17], [18] and FB-DCB [19]. H6 has the similar operation principle as H5 but more device is required. In FB-DCB, extra switches and diodes are added to build the DC bypass circuit. However higher semiconductor conduction losses are generated. Heric, as shown in Fig. 1 (e), is another type of electrically isolation topology which is available to support reactive power capability. Based on the foundation of [25] and [26], a reactive power modulation scheme was proposed by [16]. However, higher switching losses are resulted in the entire system. Also similar to Heric, there is another variant which is called HB-ZVR [20]. It replaces the bi-directional switch by a single MOSFET and a diode bridge. Also an extra diode is added to clamp the common mode noise. Conergy-NPC, [21], [22], is another type of topology that can support reactive power injection and with less semiconductor requirements. The topology diagram is shown in Fig. 1 (f). One end of the grid is always connected to the middle point of the dc to eliminate the common mode noise of the system. However, the devices breakdown voltage is double. Also similar to others, fast recovery diodes are required on the active switches, the usage of MSOFETs are limited. Therefore, either the device utilization is low or the requirement of fast recovery diode limits the selection of devices. A topology summary is given in TABLE I.

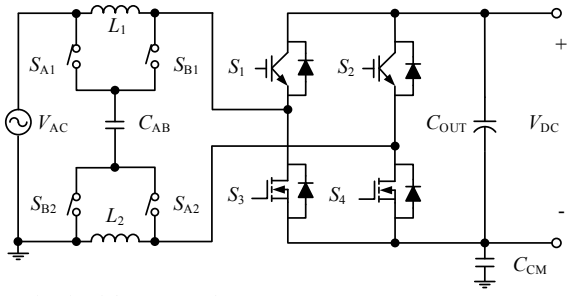


Fig. 2. Circuit of the proposed 4Q AVG converter.

In this paper, a new 4Q boost type converter is presented, as shown in Fig. 2, under the Active Virtual Ground (AVG)

converter family [27] - [29]. Different from [27] and [28], the proposed 4Q AVG converter is in another type of connection method. Based on the proposed modulation scheme, only two HF semiconductor switches are required. The circuit freewheeling path is not located in the HF switch, thus, MOSFET can be used in the circuit as a main switch. Without the tail current in the switching device, the switching frequency of the overall system can be increased and a reduction in power density is achieved. Also, all the time only two semiconductors are conducting in the main current path and only either one of them are in HF switching. A highly efficient system can be realized. Moreover, during the circuit operation, a *LCL* input filter is generated at the front state which helps to clamp CM noise generated by the system and to minimize HF ripple in the grid current. As a result, the overall HF noise is reduced [27]. The system operation can be divided into four different operation modes. Based on the phase requirement, it can be in either real power conversion (*P*) or reactive power injection. The proposed modulation scheme and the circuit operation are presented in details. Also the controller design is described in this paper. A 750 VA prototype is successfully implemented to verify the proposed topology. Those experimental results are matched with theoretical findings.

II. Proposed Reactive Power Modulation Scheme in Active Virtual Ground Converter

A. Operation Principle of the Proposed System

In Fig. 2, it shows that in the proposed topology, the main circuit is a traditional full bridge converter circuit. On top of that, an AVG circuit is implemented at the front state and is combined together as a new topology. The AVG circuit is formed by four bidirectional switches (S_{A1}, S_{A2}, S_{B1} and S_{B2}) and one HF capacitor (C_{AB}). S_{A1} and S_{A2} are synchronized together and are grouped as S_A. S_{B1} and S_{B2} are synchronized together and are grouped as S_B. By changing the switching status of the AVG switches, different *LCL* filters are formed between the grid terminals and the switching legs. Under the proposed modulation method, only switches S_3 and S_4 are required to operate at high voltage (HV) and HF. The others are all line frequency (LF) switches. Switches S_1 and S_2 are with HV but in LF operation which can be implemented by IGBT. Likewise, the bidirectional switches are in LF operation which can be implemented by a pair of low voltage switches with a source-to-source connection. In Fig. 2, a capacitor, C_{CM}, is applied to simulate the parasitic capacitor of the system. It is located between the dc bus terminal and the ac ground.

Based on different application requirements, system operation mode can be changed from real power delivery to either capacitive or inductive modes easily by varying the phase inside the system controller. The detail operations of capacitive mode are shown in Fig. 3 (a) which is separated into four different operation sections and the detail switching actions of the modulation are shown in Fig. 4. Similarly, there are 4 sections as well in inductive mode as shown in Fig. 3 (b). By applying the proposed 3-level modulation scheme, there is only one HF switch, which is used to process the power conversion in each switching state. Based on the switching sequence in Fig. 4, the corresponding switching diagram and the corresponding equivalent circuit of the proposed topology are able to be found and are shown in Fig. 5 and Fig. 6, respectively. The operation mode selection are determined by both current and voltage direction. The amount of real power through the system is controlled by the phase angle. From the apparent power (S) equation, the rms value of grid current, $I_{G,rms}$, can be expressed as,

$$I_{\mathrm{G,rms}} \cdot V_{\mathrm{AC,rms}} \cdot \cos\theta = P_{\mathrm{O}} \rightarrow I_{\mathrm{G,rms}} = \frac{P_{\mathrm{O}}}{V_{\mathrm{AC,rms}} \cdot \cos\theta}, \quad (1)$$

where $V_{\mathrm{AC,rms}}$ is rms value of grid voltage , θ is phase angle between the grid voltage and current and P_{O} is DC output power.

In Mode I, according to Fig. 4, both input voltage and grid current are also positive. S_3 works with HF ON-OFF as a converter switch and S_4 is always ON to provide a circuit current returning path, which is shown in Fig. 5 (b). The operation is equivalent to a boost converter as Fig. 6 (b). S_A is always ON at this operation mode and connects C_{AB} to the LINE (L) terminal and the drain of S_4. At the input, a *LCL* filter is formed in which inductor L_1 becomes a converter side inductor and inductor L_2 becomes a grid side inductor. C_{AB} help to clamp the HF voltage ripple coupling to the grid.

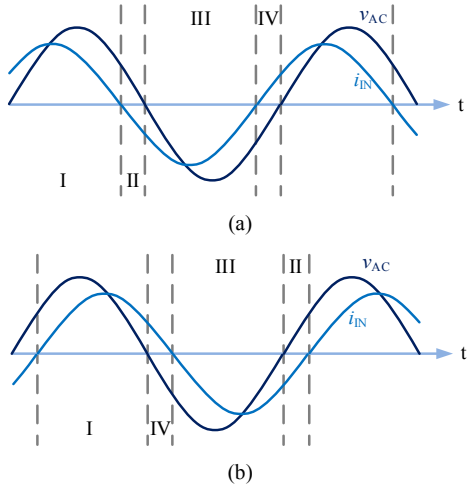


Fig. 3. Grid current and voltage waveforms at (a) capacitive mode and (b) inductive mode.

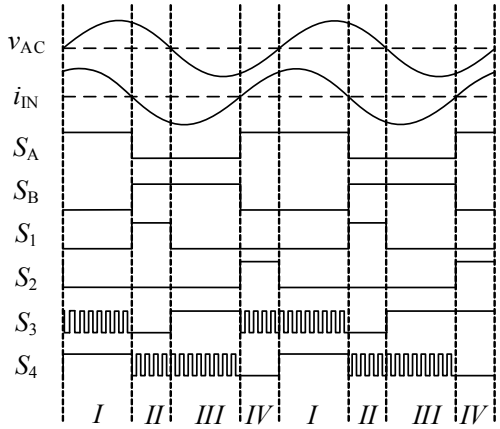


Fig. 4. Detail switching actions in capacitive mode operation.

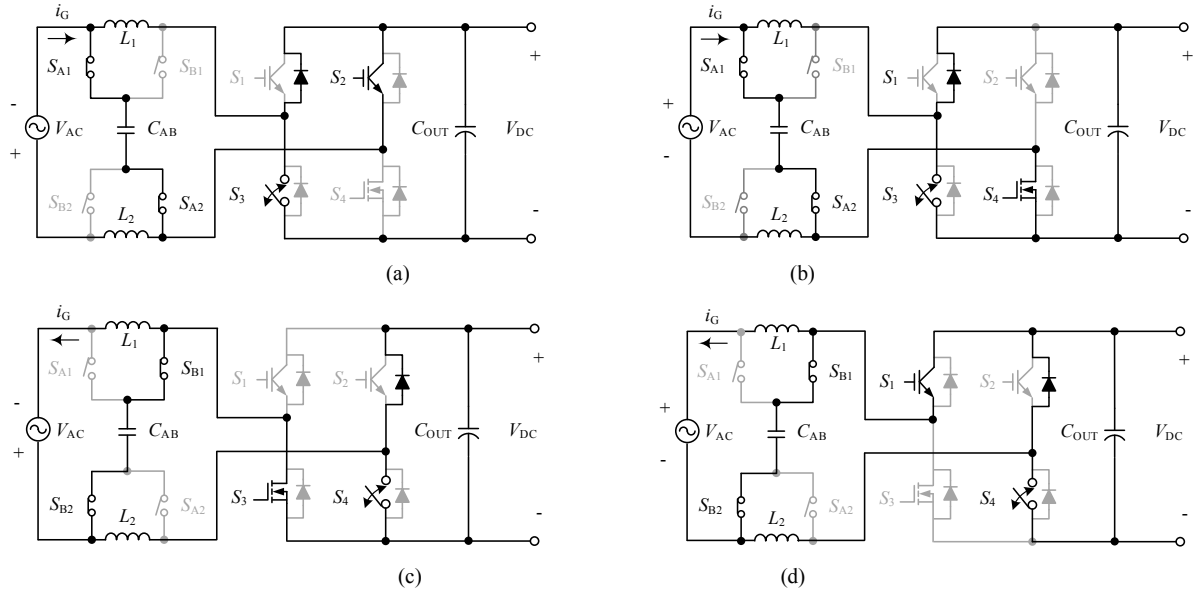


Fig. 5 Switching diagrams in (a) Mode IV, (b) Mode I, (c) Mode III and (d) Mode II.

In Mode II, according to Fig. 4, input voltage is positive with a negative grid current. S_4 works with HF ON-OFF as a converter switch and S_2 is always ON to provide a circuit current returning path, which is shown in Fig. 5 (d). The operation is equivalent to an inverted buck circuit as Fig. 6 (d). Different from Mode I, the *LCL* filter is generated by connecting C_{AB} to the NEUTUAL (N) terminal and the drain of S_3 through conduction of S_B. L_1 acts as a grid inductor and L_2 acts as a converter inductor. The voltage of C_{AB} keeps following the ac voltage and clamps the HF voltage ripple in the grid.

In Mode III, according to Fig. 4, both input voltage and grid current are also negative. S_4 works with HF ON-OFF as a converter switch and S_3 is always ON to provide a circuit current returning path, which is shown in Fig. 5 (c). The operation is equivalent to a boost converter as Fig. 6 (c). S_B is always ON at this operation mode and C_{AB} has the same connection as Mode II. Therefore comparing to Mode II, the same *LCL* filter is from in which L_2 becomes a converter side inductor and L_1 becomes a grid side inductor. And C_{AB} help to clamp the HF voltage ripple coupling to the grid.

In Mode IV, according to Fig. 4, input voltage is negative with a positive grid current. S_3 works with HF ON-OFF as a converter switch and S_1 is always ON to provide a circuit current returning path, which is shown in Fig. 5 (a). The operation is also equivalent to an inverted buck circuit as Fig. 6 (a). Same as Mode I, the same *LCL* filter is generated by conducting S_A where C_{AB} is used as filter capacitor to clamp the HF voltage ripple, L_2 becomes a grid inductor and L_1 act as a converter inductor.

The system duty is varying over the four-quadrant operation. At modes I and III, the circuit is operated as a boost converter where the corresponding duty cycle, $D_{I/III}$, can be expressed as,

$$D_{\mathrm{I/III}} = 1 - \frac{V_{\mathrm{AC}} \cdot \sin\omega t}{V_{\mathrm{DC}}}, \tag{2}$$

where ω is angular line frequency, V_{AC} is peak input voltage and V_{DC} is output voltage.

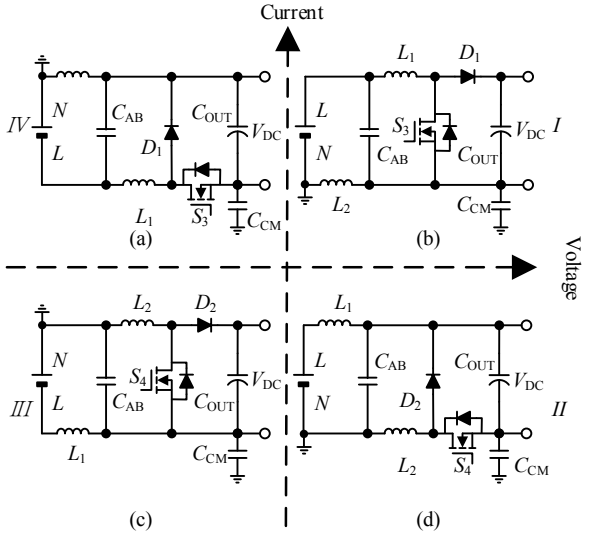


Fig. 6. Equivalent circuits of the proposed 4Q system in (a) Mode IV, (b) Mode I, (c) Mode III and (d) Mode II.

At modes II and IV, the circuit is operated as a boost converter where the corresponding duty cycle, $D_{II/IV}$, can be expressed as,

$$D_{\mathrm{II/IV}} = \frac{V_{\mathrm{AC}} \cdot \sin\omega t}{V_{\mathrm{DC}}}. \tag{3}$$

From (2) and (3), they show that the duty is different in each operation mode. When the operation mode exchanges between real power and reactive power operation, the duty cycle is totally inverted. So an extra care is required when designing the system controller.

B. High Frequency Models

By applying HF analysis method to the equivalent circuits in Fig. 6, the corresponding HF models are obtained as shown in Fig. 7 [30]. In the analysis, ac source and dc load is

considered as short-circuit, MOSFET is considered as the noise source of the system and grid-side inductor is considered as open-circuit. Accordingly, regardless of the ground tapping point on the DC link, there is no change in the HF model. In all four modes of operation, the system result the same set of HF equivalent models. The models are used to analyze the EMI performance of the system. On the EMI analysis, system noises can be classified into two types which are differential mode (DM) noise and CM noise. The DM noise is related to the magnitude of HF grid current ripple. The CM noise is related to the leakage current induced in C_{CM}.

From the characteristic of the proposed 4Q AVG converter, at every operation modes, there is always a *LCL* filter structure generated in the circuit input. Those HF DM current information, i_{HFDM}, is passing through C_{AB} and circulate inside the converter. The grid side inductor only carries LF current. As a result, in DM noise part, the influence from the HF inductor current ripple can be minimized.

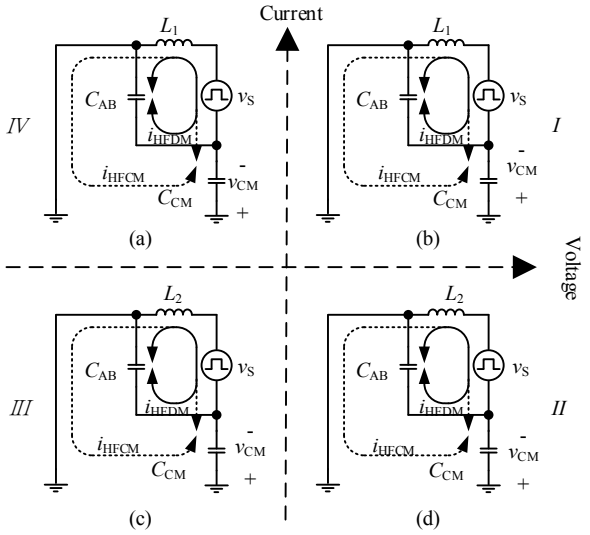


Fig. 7. High frequency models of the proposed 4Q system in (a) Mode IV, (b) Mode I, (c) Mode III and (d) Mode II.

In a general unipolar full bridge converter, C_{CM} is parallel to a converter inductor in which a high leakage current is resulted from the HF and HV switching [30]. The HF leakage current is considered as CM noise current, i_{HFCM}. In the presented circuit, due to the input filter structure, C_{CM} is always paralleling to C_{AB}. The voltage waveform of C_{AB} is always synchronized with V_{AC} and the voltage ripple is always maintained in a small value, thus, the induced system leakage current can be controlled in a small value. Referred to [27], magnitude of the HF leakage current can be calculated as,

$$\Delta i_{HFCM}(t) = \frac{C_{CM}}{C_{AB}+C_{CM}} \Delta i_L(t), \qquad (4)$$

where Δi_L is magnitude of HF inductor current.

As a result, the CM noise issue in a converter is mitigated. The overall system noise can be maintained at a low magnitude level.

III. Controller Design And Implementation

A. Controller Design

In the control architecture, as shown in Fig. 8, a double loop control methodology is applied to generate the proposed 3-level modulation switching signals. The outer loop is an output dc voltage loop and the inner loop is an inductor current loop. The whole control is implemented digitally in a DSP. Two sets of voltage sensors are applied to sense the output voltage, V_O, and the grid voltage, V_G. Also two sets of current sensors are applied to sense both of the inductor currents, I_{L1} and I_{L2} respectively.

In the design, a PLL is applied to the input voltage and is used to generate a synchronized sinusoidal reference for the controller. With the use of the sinusoidal reference and a predefined phase angle, an input current reference is resulted and is applied to the inner loop control. Through the polarity detector, both voltage and current directions are identified. So that all four modes are distinguished. S_1 and S_2 are under LF operation. They are only assigned with a switching signal when reactive power operation is required. Both S_3 and S_4 are under HF operation individually. The corresponding control signals are generated from the selection of operating mode and the assigned duty reference. The control signals of S_A and S_B are LF operation and depended on the polarity of the grid current direction. By switching the AVG switches alternatively, various *LCL* filters are built at the system input and are constructed by different connection methods of C_{AB}, L_1 and L_2 in every half line cycle. All the time only one switch is under HF operation and the others are in LF operation.

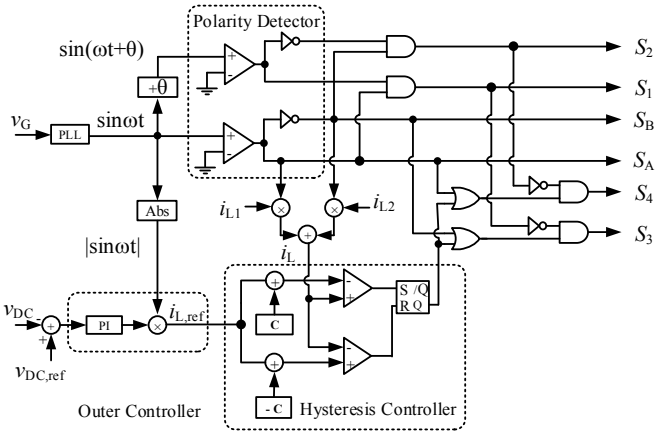


Fig. 8. Control circuit of the proposed 4Q AVG converter.

In the control scheme, the outer loop is an output voltage control where PI controller is applied. Reference to [29], Kp and Ki are selected as 0.00051 and 0.047 respectively. Its major control objective is to maintain a stable dc bus voltage during power conversion and to avoid a large voltage fluctuation during any transient conditions. The output of the outer loop is an inductor current reference. The system inner loop is an inductor current control. During the mode exchange, there is a dramatic change in duty ratio between (3) and (4). However, obtaining a step change is a challenge for a linear control method. A certain time period is required to handle the transient process. As a result, the current shape is distorted before the time that the controller can lock back the reference.

In order to provide a fast current response in the system inner loop, hysteresis controller is applied to control inductor current, I_L, and to maximize the power quality of the system. I_L is combined from the current information of L_1 and L_2, I_{L1} and I_{L2}, by synchronizes with the target current polarity. Benefit from the non-linear characteristics of controller, fast dynamic switching action is able to be guaranteed. It can provide a precise current tracking function which promises the high quality input current. Especially on the transition between real power and reactive power operations, the advantage of hysteresis control is more obvious. Therefore the system power factor is enhanced and a better system THD is obtained.

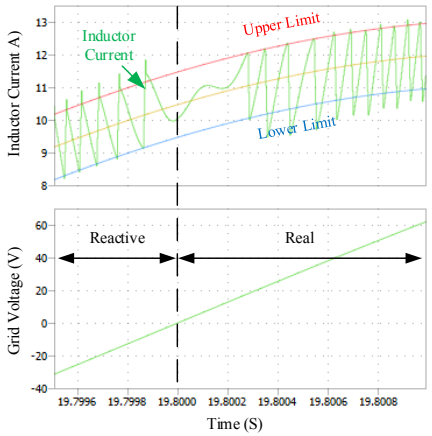


Fig. 9. Simulation waveform of capacitor mode operation.

In a digital platform, during the mode exchange between the power and reactive power operations, two possible current distortions are generated. The first one is came from digital sampling error, as shown in Fig. 9. At the zero voltage point, duty cycle of real power transfer is close to one and the corresponding duty cycle of reactive power transfer is close to zero. In the digital control, the ADC sampling point is fixed and the sampling frequency is limited. During the fast changing of current magnitude, sampling error is generated. Also, it results that the inductor current is easier to excess the current band. Especially at the voltage zero crossing position, an obvious current step is generated by the sampling error after the operation mode is exchanged and a grid current distortion is resulted due to a slightly mismatching on the average current magnitude. From the inductor off-state equation during real power operation and the inductor on-state equation during real power operation, the maximum current sampling error, Δi_{error}, can be found as,

$$\Delta i_{\text{error}} = \frac{2V_{\text{DC}}}{f_{sampling} \cdot L_{\text{X}}}, \tag{5}$$

where L_{X} is inductance of converter side inductor and $f_{sampling}$ is sampling frequency of digital controller.

Another distortion is generated from energy point of view. Similar to the current distortion as a general boost stage PFC [17] and [31]. During the voltage zero crossing region, the input voltage becomes zero but a large current magnitude is needed on the inductor to satisfy the energy demand in power conversion. Therefore it is not enough energy to magnetizing the converter inductor and leads that the current waveform is distorted for a certain period. The distortion period can be shorter by either reducing the inductance value to shorten the magnetizing time or limiting the boundary width in the hysteresis control in order to smooth the waveform. According to [31], the distortion period during zero crossing, β, is calculated as,

$$\beta = \frac{2}{\omega} \cdot \tan^{-1}\left(\frac{2 \cdot \omega \cdot L_{\text{X}} \cdot S \cos\alpha}{V_{\text{AC}}{}^2 + 2 \cdot \omega \cdot L_{\text{X}} \cdot S \sin\alpha}\right). \tag{6}$$

where α is angle that the applied in the current reference.

B. Selection of the Current Ripple Magnitude

In order to choose a suitable current ripple magnitude, ΔI, in the hysteresis control, the maximum available switching frequency, f_{SW}, is required to know. The expression of switching frequency can be found from the steady state characteristic of each mode. During real power operation, the corresponding on-state inductor voltage, $V_{\text{L,ON,I/III}}$, is,

$$V_{\text{L,ON,I/III}} = V_{\text{AC}} \cdot \sin\omega t = L_{\text{X}} \cdot \frac{\Delta I \cdot f_{\text{SW}}}{D_{\text{I/III}}}. \tag{7}$$

By combining (2) and (7), f_{SW} can be obtained as,

$$f_{\text{SW}} = \frac{V_{\text{AC}} \cdot \sin\omega t}{V_{\text{DC}}} \cdot \frac{V_{\text{DC}} - V_{\text{AC}} \cdot \sin\omega t}{L_{\text{X}} \cdot \Delta I}. \tag{8}$$

During reactive power operation, the corresponding on-state inductor voltage, $V_{\text{L,ON,II/IV}}$, is defined as,

$$V_{\text{L,ON,II/IV}} = V_{\text{DC}} - V_{\text{AC}} \cdot \sin\omega t = L_{\text{X}} \cdot \frac{\Delta I \cdot f_{\text{SW}}}{D_{\text{II/IV}}}. \tag{9}$$

By combining (3) and (9), the switching frequency has the same expression as (8). Therefore under the same boundary value, the mode transition between real power and reactive power can have a smoothly interaction. From (8), it shows that under a constant current band, the maximum switching frequency point is located at the maximum input voltage point. As a result, by putting in the system parameters and the maximum available switching frequency into (8), a suitable current band can be found. The hysteresis band is inversely proportional to the switching frequency, it means that increasing switching frequency could reduce current ripple but lower in system efficiency due to increased switching loss at each device. Thus, device with low parasitic capacitance and fast transient behavior is recommended for S_3 and S_4 in HF applications. In our design, the inductor is selected to 1.2 mH. Therefore, 2 A is selected as the current band which helps to limit the switching frequency within a 30 kHz range.

C. Selection of Components

In each state, only one semiconductor switch is under HF switching. S_3 is in HF switching during positive current flow and S_4 is forced to be in HF switching during negative current condition. MOSFETs, IPW60R070C6, are selected to implement as the HF and HV switches of S_3 and S_4. S_1 and S_2 are both LF switches which only operate at modes II and IV to provide a current returning path for the delivery of reactive power. In order to provide a fast reverse recovery performance during the freewheeling process, IGBTs with fast recovery anti-parallel diode, IKW20N60H3, are selected to implement as S_1 and S_2. All of AVG switches are implemented by LF MOSFETs, STB46NF30, in source-to-source configuration as

shown in Fig. 10. The path of the AVG circuit is only required to handle the HF current ripple, therefore, losses on the AVG switches are not that significant. An estimated loss breakdown is shown in Fig. 11, which is done at the full power rating condition in rectifier mode operation. It shows that under 2A current band, the devices loss in the AVG switches are only contributed 1% of the overall loss. Thus, losses on top are little and no extra heatsink is required. All the AVG switches can be mounted on a daughter board and do the cooling through the PCB.

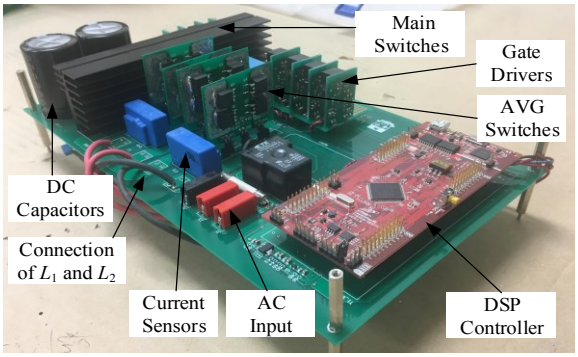


Fig. 10. Experimental prototype.

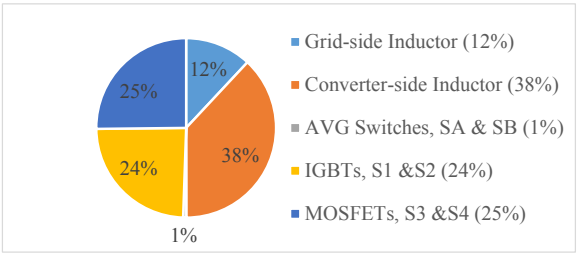


Fig. 11. Loss breakdown in proposed converter under full power rating.

IV. Experimental Verification

A 750 VA test platform, as shown in Fig. 10, is built to verify the proposed 4Q AVG converter and the conditions of the system is shown in TABLE II. In our design, 2 A is selected as the inductor current band and the maximum switching frequency is 26 kHz. According to [27], a 3.3 µF film capacitor is selected as the circuit filter capacitor.

Fig. 12 shows that the converter has a stable operation under different operation modes where all the testing points are with full rated power rating. When the power direction is positive, an ac source, ac output mode of Keysight AC6803A, is applied as the input and a group of resistive loading is applied to the output. In Fig. 12 (a), it shows the steady state performance of the system during 750 W real power test case. Under the same apparent power rating, waveform that operating at capacitive shown in Fig. 12 (c) where a positive 60˚ is applied to the reference grid current. In Fig. 12 (d), it demonstrates the system operation at inductive mode operation with a negative 60˚ on the reference grid current. When the power direction is inverted, a dc source, dc output mode of Keysight AC6803A, is applied to C_{OUT} and the input side is directly connected to the grid with a pre-defined current magnitude. In Fig. 12 (b), it shows out the system steady state performance at inverter mode operation.

As shown in Fig. 12 (a) – (d), under the hysteresis control, a fast dynamic response is provided. The inductor current was all the time switching within the boundary. During the operation, an *LCL* was formed at the converter input. In the positive current cycle, the set of AVG switch S_A were ON. Inductor L_1 acted as a converter side inductor and took care of the HF ripple. Inductor L_2 acted as a grid side inductor and carried the 60 Hz current information. Both inductors were connected with the filter capacitor C_{AB} to form a *LCL* input filter. During the negative current cycle, the inductor role was changed. With the connection of C_{AB} through S_B, another set of *LCL* was formed. Inductor L_1 became a grid side inductor and carried the 60 Hz current information. Inductor L_2 became a converter side inductor and took care of the HF ripple.

TABLE II
VALUE OF THE SYSTEM PARAMETERS THAT USED IN THE DESIGN

Parameter	Value	Parameter	Value
Input Voltage	120 Vac	Output Voltage	250 Vdc
Input Frequency	60 Hz	Output Power	750 W
Current Band	2 A	Output Capacitor	1.2 mF
Inductor (L_1 & L_2)	1.2 mH	Capacitor (C_{AB})	3.3 µF

TABLE III
SUMMARY OF THE TEST RESULTS

Operation Mode	Fig. 12	I_{rms} /A	P /W	Q /VA	η/%	THD /%	PF
Rectifier	(a)	6.49	771	0	96.98	3.63	0.997
Inverter	(b)	6.48	-780	0	96.83	3.85	0.990
Capacitive	(c)	6.54	393	-676	93.84	4.81	0.503
Inductive	(d)	6.55	380	684	93.48	4.91	0.485

By switching the AVG switches alternatively, the filter capacitor voltage was following to the grid voltage. A set of experimental test are done to verify the operation of the AVG switch. S_A is monitored during the test and the result is shown in Fig. 13. As shown in Fig. 13 (a), the control signal of S_A is under LF operation. S_A was ON when the current polarity is positive. The current passing through S_A was the filter capacitor current which was equal to the HF current ripple in the converter-side inductor. Under the hysteresis control, the ripple was kept within the current band. S_A was OFF when the current polarity was negative. As shown in Fig. 13 (b) and (c), the voltage stress on S_{A1} and S_{A2} are different. The voltage applied on top of S_{A1} was equal to the voltage ripple on top of the grid-side inductor which was generated from the difference between grid voltage and filter capacitor voltage. The voltage applied on S_{A2} was the same as the voltage ripple appeared on the converter-side inductor. The voltage stress on S_{A2} was more significant than the voltage stress on S_{A1}, as the converter-side inductor was aimed for energy transfer. Similarly, the same performance was occurred in S_B.

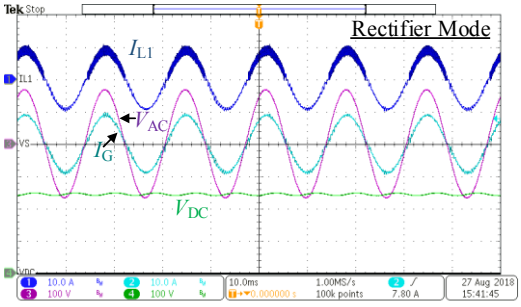
During the operation, the HF voltage ripple was kept in a relatively small value. Thus, the resultant system CM noise would be small as well. Reference to [29], [32], a 330 pF capacitor was applied to the system to simulate the parasitic capacitance of the system. The resultant leakage current of the system during rectifier mode, inverter mode, capacitive mode and inductive mode operation are measured and are shown in Fig. 14 (a), (b), (c) and (d) respectively. In all the cases, the magnitudes of the leakage current were also maintained in 2

mA range. All the results have a very good alignment with the topology concept and meet the design target.

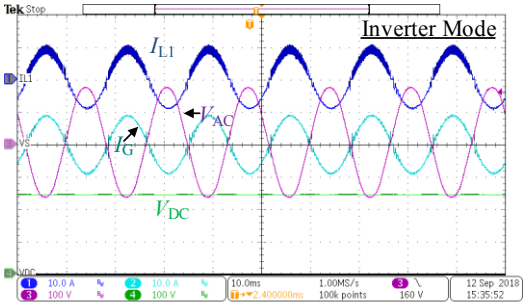
Under the steady state situation, the system was performance well. In both rectifier mode and inverter mode operations, the system power factor (PF) was always kept higher than 0.9. In rectifier mode, the PF was 0.997. Meanwhile, in inverter mode, the PF was 0.990. At the full power operation, the efficiency in rectifier mode was 96.98 % where the current THD was 3.632 %. Similarly, in inverter mode operation, the system efficiency was 96.83 % together with a 3.85 % current THD. In both cases, each THD magnitude was also within the requirement of IEEE 519 [33]. A summary of the test results is shown in TABLE III.

In reactive power operation, the system performance were also maintained well. In Fig. 12 (c), during capacitive mode testing, a positive 60˚ was applied to the reference grid current. In contract, during inductive mode testing in Fig. 12 (d), a negative 60˚ was applied to the reference grid current. In both cases, the apparent power was 750 VA and real power was half of it. The system efficiency in capacitive mode and inductive mode were 93.84 % and 93.48 % respectively. The system efficiency was slightly reduced when reactive power injection was required. Under the same apparent power level, the input current amplitude remained the same, which caused the device losses on these switches and inductors to keep in a similar level. However, during capacitive mode or inductive mode operation, the real power consumption was reduced. Therefore, the overall system efficiency was relatively low. An efficiency figure is shown in Fig. 15, which demonstrates the relationship between system efficiency and system phase angle under the same apparent power condition. Meanwhile, in both test cases of Fig. 12 (c) and (d), the current THD can also be kept in the 5 % range. The current THD in capacitive modes and inductive were 4.81 % and 4.91 % respectively. An effective power conversion can be achieved in all the four operation modes.

Apart from steady state, the system was also stable during transient operation. In Fig. 16 shows out the system performance during load transient changing from 170 Ω to 85 Ω. The system was able to return to steady state within a short moment of time after the change appeared and the output voltage was always kept higher than 200 V. Therefore, a stable system was able to be guaranteed.



(a)



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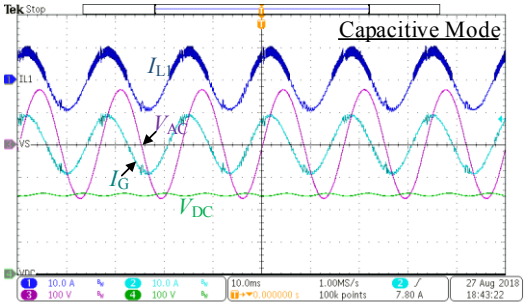
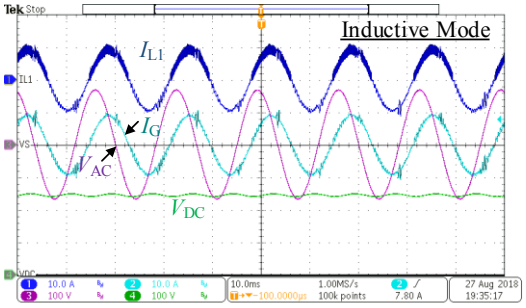
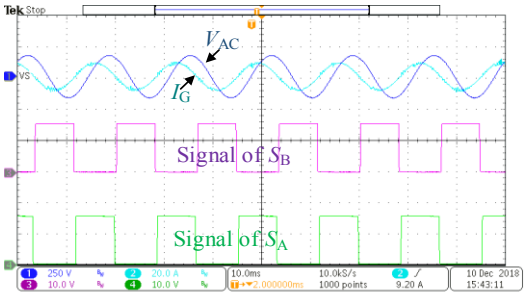


(c)

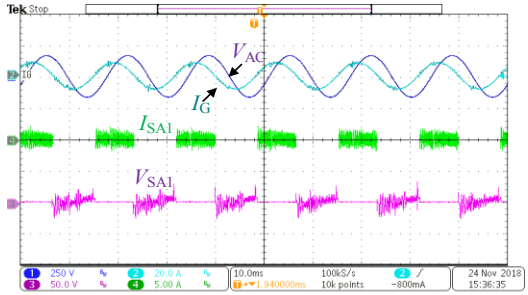


(d)

Fig. 12. Experimental results of steady state performance: (a) rectifier mode, (b) inverter mode, (c) capacitive mode and (d) inductive mode.



(a)



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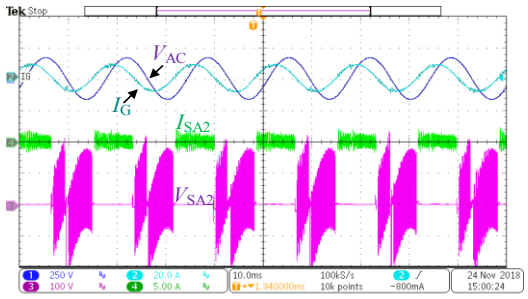
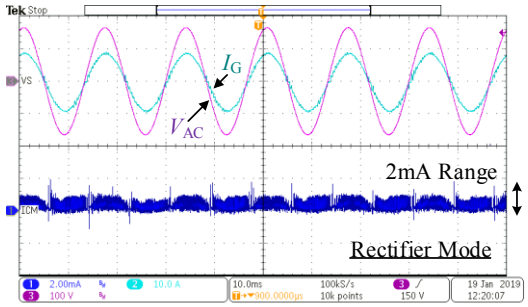
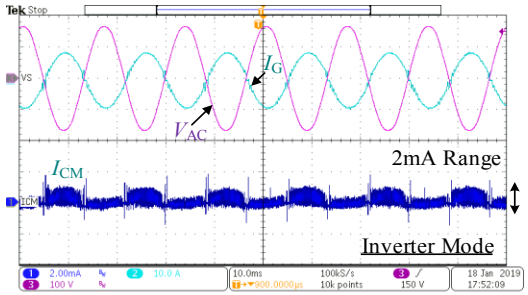


(c)

Fig. 13. Experimental results of S_A: (a) control signal, (b) device stress in S_{A1} and (c) device stress in S_{A2}.



(a)



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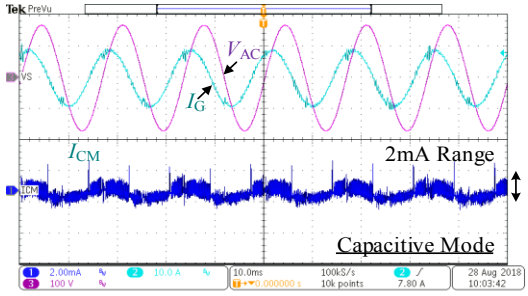
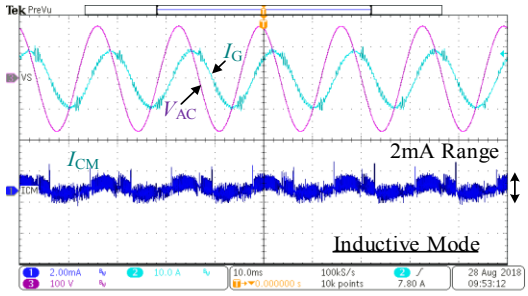


(c)



(d)

Fig. 14. Experimental results of leakage current measurement: (a) rectifier mode, (b) inverter mode, (c) capacitive mode and (d) inductive mode.

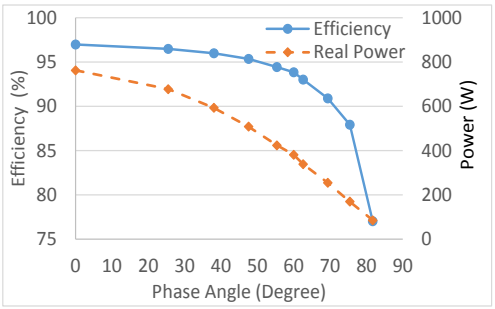


Fig. 15. Efficiency plot of prototype under varying phase conditions.

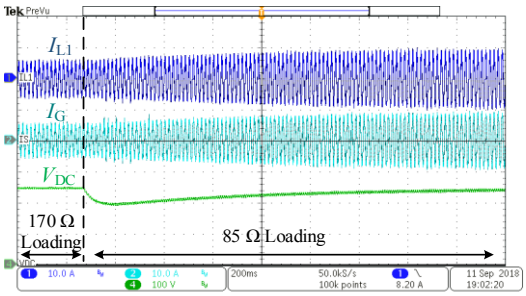


Fig. 16. Experimental results of transient performance of load change.

V. Conclusion

The paper presented a new four-quadrant converter with the use of Active Virtual Ground technique. Under the proposed modulation scheme, it is able to support both real power and reactive power delivery with the use of two HF and HV switches only. The circuit freewheeling paths are located in the LF switches, so no extra device stresses are added onto the HF switches. During the system operation, a reconfigurable *LCL* filter is generated at the system input. The filter capacitor helps to build up a connection between the DC link and the grid, thus, the HF CM noise and generated leakage current of the system is always maintained in a low level. The operating principles and the steady state characteristics of the proposed topology are explained in details. A 750 VA prototype has been built to verify the presented concept. The performance of proposed 4Q AVG converter is demonstrated by experimental results which shows a good agreement with the theoretical concept.

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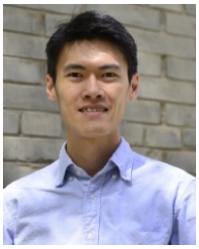

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