A Method for Solving Current Unbalance Problem of Paralleled Single-Phase Grid-connected Unipolar-PWM Inverters with Common Dc Bus

Dong Li, *Student Member, IEEE*, and Carl Ngai Man Ho, *Senior Member, IEEE*
RIGA Lab, University of Manitoba
75 Chancellors Circle
Winnipeg, MB, R3T 5V6, Canada
Carl.ho@umanitoba.ca

***Abstract* -- Unipolar-PWM (UP-PWM) inverter takes advantages of high power efficiency and small output chokes which is widely used in industry. However UP-PWM inverters cannot be used in parallel operation due to a current unbalance problem. This paper studies the current unbalance problem of paralleled UP-PWM inverters with common dc bus and ac bus. Firstly, the problem of unbalanced inductor current is defined and analyzed. Secondly, a technique to eliminate unbalanced currents is proposed. The proposed current balancing technique only requires one more current sensor in an inverter module rather than changing converter topology or modulation method, which makes it possible to apply unipolar-PWM inverters in parallel-operation while keeping the advantages of unipolar switching. The proposed current balancing method is verified by both simulation and hardware experiment. Experimental verification is performed on two 1kW, 400V input, and 120V/60Hz output prototypes, which shows a good agreement to the analytical study.**

***Index Terms*-- Unipolar PWM, Parallel operation, Circulating current, Unbalanced current**

I. INTRODUCTION

Photovoltaic (PV) generation plays an important role in renewable energy and the future smart grids. Voltage Source Inverter (VSI) is an interface of injecting solar power into public ac grid [2]. With the growing demands for PV generation, the requirement of larger capacity and higher flexibility on solar inverter becomes more and more significant. Conventional single-operated solar inverter has a lot of restrictions in terms of scalability, reliability and flexibility and will face the problem of light load operating and higher loss due to using of high current power semiconductors or bulky passive components [3]. Parallel-operated inverters can reduce the stress of high current by distributing power into multiple modules. Thus, parallel-operated modular converters are preferred in many situations [4]-[5].

Fig. 1 shows two typical configurations of distributed PV generation system [6]. In both dc-module type and multistring type, power generated from PV panels firstly converted by dc-dc converters with maximum power point tracking (MPPT) controller to a common dc bus, and then go through a dc-ac stage to the public grid. A centralized inverter was commonly used in this dc-ac stage [7]. However, a centralized inverter lacks scalability, reliability and flexibility for grid-connected application. Hence, modularized architecture will be preferred for the dc-ac stage in many cases.

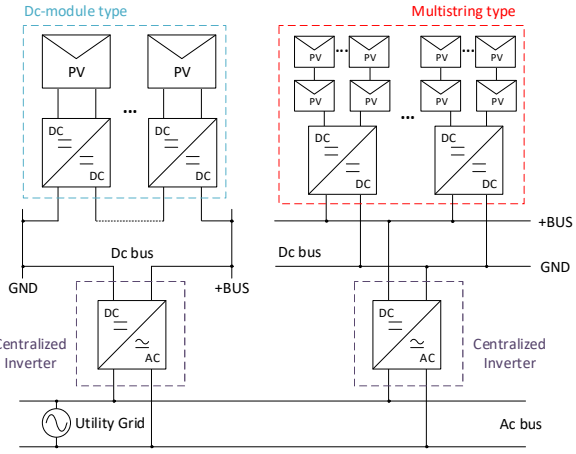


Fig. 1 Typical distributed PV generation systems.

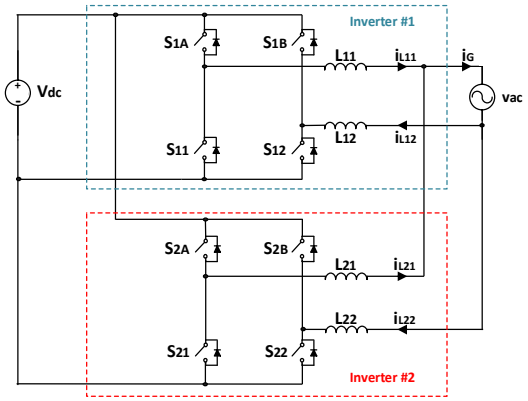


Fig. 2 Parallel-operated inverters with common dc bus and ac bus.

Fig. 2 shows the connection that two inverter modules working in parallel with common dc and ac buses. Using a number of parallel-operated inverter modules takes advantages rather than using a single centralized inverter:

1) Redundancy can be improved by the N+1 configuration realized by multi-module parallel operation, which can increase the system reliability [8]-[9].

2) System control can be more flexible. Power sharing strategy can be made based on parallel operation, to avoid

This is an updated version of conference paper [1]. This new version includes further mathematical analysis and updated experimental results.

inverter light-load operating. Each module can operate at its optimized power rating, which can improve system performance [10]-[13].

3) System can be more scalable. System capacity can be increased by simply adding more inverter modules without removing existing inverters [14].

4) Modularized inverters meet the requirement of mass production, which will significantly reduce cost of design and production.

However, there are some problems when inverters operate in parallel mode, of which the most significant one is unbalanced current. In order to analyze and understand the issues and characteristics of paralleling inverters, researchers investigated several cases of parallel-operated grid-tied inverters with different topologies and modulation strategies [15]-[16]. Among the cases, bipolar PWM (BP-PWM) inverter, Unipolar Double Frequency PWM (UDF-PWM) inverter [17], and H5 inverter [18] are free of unbalance current problem in parallel operation; full-bridge inverter with Unipolar Pulse Width Modulation (UP-PWM) faces a current unbalance problem in parallel operation. A UP-PWM inverter has only 2 high-frequency (HF) switches and only 1 of the HF switches is switching at one moment, which is less than other modulation methods mentioned above, where the details are given in table I. The switching combination of UP-PWM inverter could provide a lower switching loss and lower semiconductor cost [19]. However, the unbalance current problem in parallel operation makes the advantages of UP-PWM inverters cannot be maintained in the parallel-operating mode. Furthermore, there is no study giving any detailed explanation on the causes of generating unbalanced currents or providing any solution to balance the currents without changing topology or modulation method. It makes that UP-PWM inverter has not been widely used for paralleling to scale up the rated power. The proposed method enables parallel operating of UP-PWM inverters with simply adding one more current sensor, and the advantage of low switching loss and low semiconductor cost can be kept.

In order to standardize inverter modules, which are capable of scaling up the handling power by paralleling, this paper proposes a method to achieve the following features in UP-PWM inverters,

1) The inverter modules are unipolar switching either in single-module or multi-module operating mode. It provides the advantages of small output choke size and semiconductor losses [20]-[21].

2) Grid current can be evenly shared by the inverter modules.

In this paper, firstly, the problem of unbalanced inductor currents in parallel-operated UP-PWM inverters is defined and analyzed by system equivalent circuits and control loop analysis. The idea of Switched-Controlled (SC) and Non-Switch-Controlled (NSC) inductor, which is resulted by the nature of unipolar switching, was proposed to explain the current unbalance problem. Then a new concept of proposed dual current sensor technique to solve the inductor currents balancing issue is introduced. Two Digital Signal Processor (DSP) controlled, 1kW, 400V input, and 110V/60Hz output inverter modules have been implemented and evaluated in parallel connection. Proposed method is verified by experimental test. The result shows a good agreement to analytical study.

TABLE I
NUMBERS OF SEMICONDUCTORS USED FOR FULL BRIDGE INVERTERS WITH DIFFERENT PWM METHODS OR TOPOLOGIES

	No. of Switches		No. of HF Switches under operating	No. of Switches in the Main Current Path
	HF	LF		
UP-PWM	2	2	1	2
BP-PWM	4	0	4	2
UDF-PWM	4	0	2	2
H5	3	2	2	3

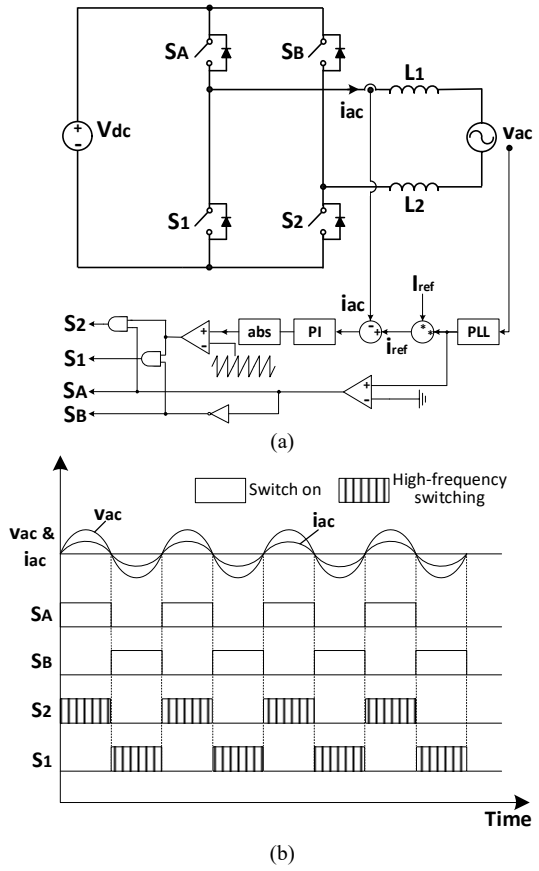


Fig. 3 Typical full bridge inverter with UP-PWM: (a) topology and control, and (b) switching pattern.

II. ANALYSIS OF UNBALANCED INDUCTOR CURRENT

In this section, the cause of unbalanced inductor current problem in conventional parallel-operated UP-PWM inverters is identified and analyzed.

TABLE II
PARAMETERS OF SIMULATED INVERTER MODULES

Parameter	Value	Parameter	Value
$V_{ac\text{-}rms}$	120 V	V_{DC}	380 V
I_{ref1}	5 A	f_{sw}	20 kHz
L_{11}, L_{12}, L_{21}, L_{22}	2 mH	Sawtooth Signal Phase Difference	π
k_p	0.07	k_i	350

Fig. 3 (a) shows a typical full bridge grid-connected VSI with two split-filter inductors and its controller block diagram with UP-PWM switching scheme. Fig. 3 (b) shows a typical unipolar PWM switching pattern for the full bridge VSI. S_A and S_B are line frequency (e.g. 60 Hz) switches and S_1 and S_2 are high frequency (e.g. 20 kHz) switches. This combination of semiconductors gives a better switching performance by using MOSFETs and fast diodes [22]. It is widely used in industry, especially solar inverters [23]. The control algorithm can be easily realized by an analog or digital controller.

Fig. 2 shows the connection that two inverters operate in parallel with common dc bus and ac bus. Ideally, each inverter should be able to work individually or in parallel, so each of them has an independent controller as Fig. 3 (a) shows.

If parameters of the two UP-PWM inverters are identical, equal current sharing among the paralleled inverters should be possible. However, in a real application, the inductor current will become unbalanced. The cause of this unbalanced current issue is studied in this section, which is found out to be a misalignment of the current reference or sensor gain.

A simulation model was built considering differences in PWM carrier signals and current reference signals. Each inverter module is same as shown in Fig. 3. The connection is shown in Fig. 2. Current sensors are set to sense currents on i_{L11} and i_{L21}. Simulation parameters are shown in TABLE II. Two carrier sawtooth signals are set to be unsynchronized, in the simulation case, which have a phase difference of half cycle π. Parameter K_{ref} is used to represent the difference between two reference signals,

$$i_{ref2} = K_{ref} \cdot i_{ref1} \quad (1)$$

Fig. 4 shows the simulation results that K_{ref} varies from 1 to 0.994. It can be seen in Fig. 4 (a) that when $i_{ref1} = i_{ref2}$, though the current ripples are not symmetrical and varying due to the unsynchronized sawtooth signals, two inverters can equally share power, and inductor currents are balanced. In Fig. 4 (b), (c) and (d), though the difference of two reference signals are very small that less than 1 percent, inductor currents i_{L12} and i_{L22} become seriously distorted and unbalanced. And while the reference difference getting larger, the currents become more unbalanced. At the same time, grid current i_G and inductor currents i_{L11}, i_{L21} are still sinusoidal and following references. The unbalanced currents on L_{12} and L_{22} could already damage devices and have distorted the power sharing purpose of inverters parallel-operating.

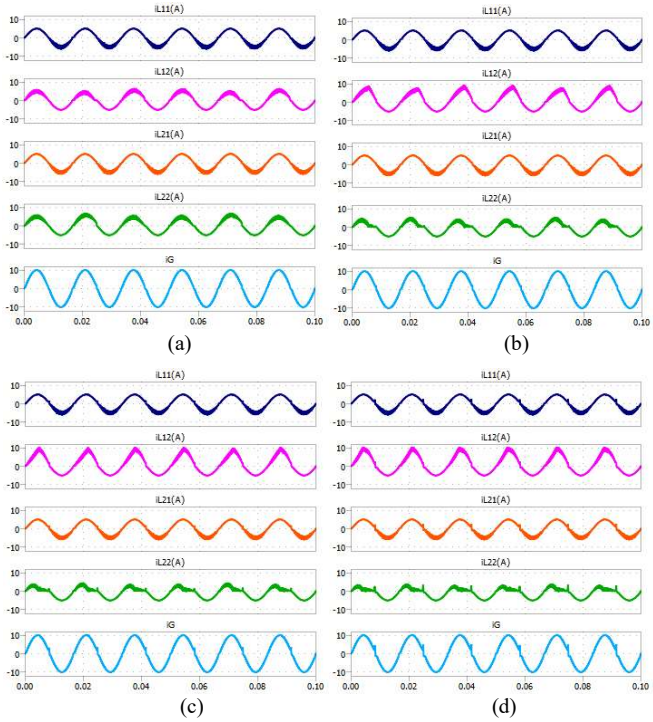


Fig. 4 Simulation results of two conventional UP-PWM inverters work in parallel: (a) K_{ref} =1, (b) K_{ref} =0.998, (c) K_{ref} =0.996, (d) K_{ref} =0.994.

Noticing that unbalanced current only happens in half cycle of operation. Based on Fig. 2 and the switching pattern in Fig. 3 (b), equivalent circuits with controllers can be obtained when v_{ac} is in positive cycle and negative cycle, respectively, as shown in Fig. 5 (a) and (b). Fig. 6 shows the corresponding control block diagrams. T_1 and T_2 are the open-loop transfer functions of the two inverters.

The position of current sensors is physically fixed to sense currents on L_{11} and L_{21}, which makes the parallel operated system in positive and negative cycles different. In Fig. 5 (a), feedback signals are from i_{L11} and i_{L21} on the upper branches, while the PWM signals go to S_{12} and S_{22} on the lower branches which are connected to L_{12} and L_{22}, as indicated in red dashed line blocks. It can be seen from the simulation results that current unbalance only happens in this half cycle. In Fig. 5 (b), active switches S_{11}, S_{21} and feedback signals i_{L11}, i_{L21} are both on the lower branches as shown in blue dashed line blocks, in which case it is free of current unbalance problem.

Each UP-PWM inverter has two split inductors and only one high-frequency switch at a moment. Hence, the inductors can be separated into two operating conditions, Switching-Controlled (SC) and Non-Switching-Controlled (NSC). For the SC status, inductors are directly connected to high-frequency switches, so the inductor currents are directly influenced by switching actions, like L_{12} and L_{22} in Fig. 5 (a) and L_{11} and L_{21} in Fig. 5 (b). For the NSC status, inductors are connected to a closed switch and are parallel with other NSC inductor. They share the grid current simply depending on branch impedance, like L_{11} and L_{21} in Fig. 5 (a) and L_{12} and L_{22} in Fig. 5 (b). Table III shows how the inductors act in two half

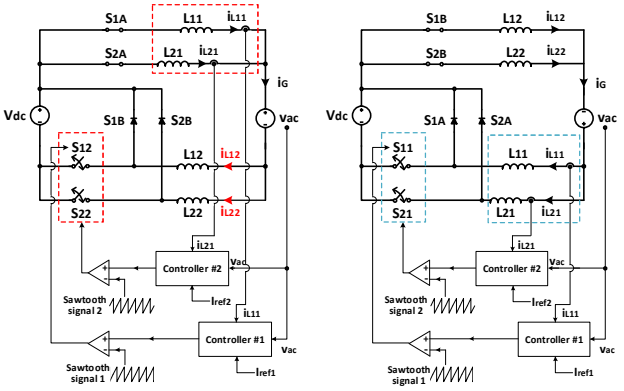


Fig. 5 Parallel operating equivalent circuits,
v_{ac} is in (a) positive half cycle, (b) negative half cycle.

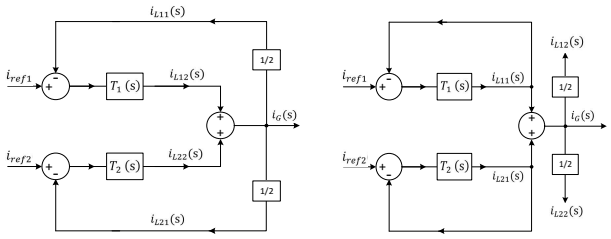


Fig. 6 Parallel operating control block diagrams,
v_{ac} is in (a) positive half cycle, (b) negative half cycle.

TABLE III
OPERATING STATUS OF INDUCTORS

	HF switches	L_{11}	L_{12}	L_{21}	L_{22}
$v_{ac} > 0$	S_{12}, S_{22}	NSC	SC	NSC	SC
$v_{ac} < 0$	S_{11}, S_{21}	SC	NSC	SC	NSC

cycles. Only when the feedback signals are from NSC inductor currents, unbalanced inductor currents will appear.

According to simulation results in Fig. 4, unbalanced inductor currents only occur in the positive half cycle of v_{ac}, of which the equivalent circuit is shown in Fig. 5 (a). In this half cycle, S_{12} and S_{22} are working at high frequency, which means i_{L12} and i_{L2} are SC inductor currents. However, the current sensors are fixed to measure i_{L11} and i_{L21} which are NSC inductor currents. The control block diagram for this half cycle is shown in Fig. 6 (a). Two control loops are interacting with each other through the common ac bus. Meanwhile in the other half cycle, as shown in Fig. 6 (b), the two control loops are still independent from each other which is free of unbalanced current problem.

Based on the control block diagram shown in Fig. 6 (a), i_G can be expressed as,

$$i_G = (i_{ref1} - i_{L11})T_1 + (i_{ref2} - i_{L21})T_2 \tag{2}$$

Assume all branches are identical, i_{L11} and i_{L21} will always equally share i_G,

$$i_{L11} = i_{L21} = \frac{i_G}{2} \tag{3}$$

By putting (3) into (2), i_G can be written as,

$$i_G = \frac{i_{ref1}T_1 + i_{ref2}T_2}{1 + \frac{1}{2}T_1 + \frac{1}{2}T_2} \tag{4}$$

T_1 and T_2 have almost same frequency responses and their gains are much larger than 1,

$$T_1 \approx T_2 \text{ and } |T_1| \approx |T_2| \gg 1 \tag{5}$$

Based on (4) and (5), we can have the expression of i_G at low frequency,

$$i_G \approx i_{ref1} + i_{ref2} \tag{6}$$

Hence, grid current i_G can well follow the references, and if $i_{ref1} \approx i_{ref2}$, NSC inductor currents i_{L11}, i_{L21} could also follow each reference based on (3).

From Fig. 6 (a), we could also have,

$$i_{L12} = (i_{ref1} - i_{L11})T_1 = \left(i_{ref1} - \frac{i_G}{2}\right)T_1 \tag{7}$$

By putting (1) and (4) into (7),

$$i_{L12} = \left(\frac{2i_{ref1} + i_{ref1}T_2 - K_{\text{ref}}i_{ref1}T_2}{2 + T_1 + T_2}\right)T_1 \tag{8}$$

Simplify (8),

$$\frac{i_{L12}}{i_{ref1}} = \frac{2T_1 + (1 - K_{\text{ref}})T_1T_2}{2 + T_1 + T_2} \tag{9}$$

Similarly, for inverter #2, it also can be derived that,

$$\frac{i_{L22}}{i_{ref2}} = \frac{2T_2 + (1 - \frac{1}{K_{ref}})T_1T_2}{2 + T_1 + T_2} \tag{10}$$

Putting (5) into consideration, (9) and (10) can be rewritten as,

$$\frac{i_{L12}}{i_{ref1}} = 1 + (1 - K_{\text{ref}})T_1 \tag{11}$$

$$\frac{i_{L22}}{i_{ref2}} = 1 + (1 - \frac{1}{K_{ref}})T_2 \tag{12}$$

Apparently, if K_{ref} is ideal that equal to one, values of equations (11) and (12) will both be one, which means inductor currents i_{L12} and i_{L22} can follow the references i_{ref1} and i_{ref2} respectively. However, even if K_{ref} is just slightly different from 1, values of equation (11) and (12) will deviate from one significantly, because gain of T_1 and T_2 is designed to be large enough to obtain smaller steady state error. It means the slight difference of current reference or sensing gain will be amplified. As a result, inductor currents become unbalanced between SC inductor currents i_{L12} and i_{L22}, as the simulation results shown in Fig. 4. Moreover, equations (11) and (12) also agree the simulation results that the more K_{ref} is far from 1, the more distorted and unbalanced the currents are.

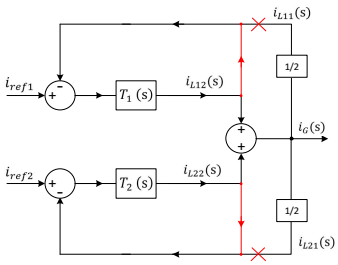
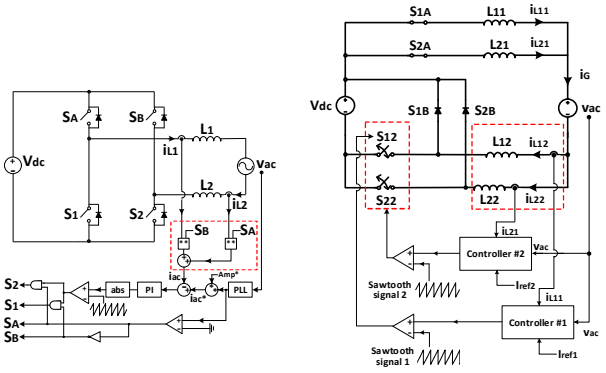


Fig. 7 Modification to avoid unbalanced inductor currents, $v_{ac} > 0$.



(a) (b)

Fig. 8 Proposed method to balance inductor currents in parallel-operation: (a) proposed method, and (b) its parallel operating equivalent circuit when v_{ac} is in the positive cycle.

When v_{ac} is in the negative half cycle, the feedback signals i_{L11} and $i_{L21}$are SC inductor currents. The equivalent circuit and control diagram are shown in Fig. 5 (b) and Fig. 6 (b) respectively. It can be seen from Fig. 6 (b), i_{L11} and i_{L21} are controlled by two independent control loops, that satisfy,

$$i_{L1} = \frac{T_1 i_{ref1}}{1+T_1} \tag{13}$$

$$i_{L2} = \frac{T_2 i_{re}}{1+T_2} \tag{14}$$

While considering assumption (5),

$$i_{L11} \approx i_{ref1} \tag{15}$$

$$i_{L21} \approx i_{ref2} \tag{16}$$

And i_{L12} and i_{L22} will equally share i_G,

$$i_{L12} = i_{L22} = \frac{i_{ref1}+i_{ref2}}{2} \tag{17}$$

Therefore, all four inductor currents can follow the reference in the negative half cycle of v_{ac} which agrees simulation results in Fig. 4.

Based on the analysis above, the difference of current references of parallel-operated inverters, which is represented by (1), is the major reason of unbalanced inductor currents happening. Although individual digital controllers have the same digital reference values, eventually the references can hardly be the same such as in unit feedback equivalent diagrams Fig. 6, due to the error of sampling circuit, analog-digital conversion and environmental noises. Therefore, K_{ref} in (1) cannot reach one practically.

III. Proposed Dual Current Sensor Method

While the misalignment of current reference or sensor gain cannot be removed practically, there are other approaches may solve the current unbalance problem.

Based on analysis in Section II, the current unbalance problem is caused by the control structure shown in Fig. 6 (a) that the feedback signals are from NSC inductor currents when in the positive half cycle of v_{ac}. When v_{ac} is in the negative half cycle, the control structure as shown in Fig. 6 (b) is free of unbalance current problem. To mitigate the unbalanced currents, the control block diagram should be modified in the positive half cycle of v_{ac} to change the feedback signal to SC inductor currents. Then in both half cycles, the control structure could be kept as same as in Fig. 6 (b).

Hence, when the high frequency switches are S_{12} and S_{22}, feedback signals should be i_{L12} and i_{L22} rather than i_{L11} and i_{L21}. Fig. 7 shows the proposed modification to the control diagram in this half cycle. The proposed technique is to simply add one more current sensor on each inverter module to measure currents on both inductors, then current feedback signal is inter-changed accordingly between two measured current signals in positive and negative half cycles.

The proposed dual current sensor technique is highlighted with a red dash block in the control block diagram in Fig. 8 (a). Two current sensors are used in each inverter to measure currents on both two split inductors. When S_A is turned on, S_2 is working at high frequency, SC inductor current i_{L2} will be taken as the feedback signal. When S_B is turned on, S_1 is working at high frequency, SC inductor is changed to L_1, and i_{L1} will be taken as the feedback signal. By drawing parallel-operating equivalent circuits, when v_{ac} is in negative cycle, inverters operate the same as the equivalent circuit in Fig. 5 (b). When v_{ac} is in positive cycle, feedback signals change to i_{L12} and i_{L22}, and equivalent circuit changes to Fig. 8 (b). Therefore, the parallel-operated inverters can work symmetrically in positive and negative half cycle, and inductor currents will be well balanced all the time.

With the proposed method, in negative half cycle of v_{ac}, four inductor currents will keep following equations (15) – (17). In positive half cycle of v_{ac}, the four inductor currents now follow,

$$i_{L12} \approx i_{ref1} \tag{18}$$

$$i_{L22} \approx i_{ref2} \tag{19}$$

$$i_{L11} = i_{L21} = \frac{i_{ref1}+i_{ref}}{2} \tag{20}$$

Hence, while $i_{ref1} \approx i_{ref2}$, all inductor currents will be balanced all the time. It also can be seen that, if i_{ref1} and i_{ref2} are different, inductor currents will become unsymmetrical in positive and negative half cycles. When the inductor is SC,

inductor current will follow one of the reference current, which is represented by (15) - (16) and (18) - (19). When the inductor is NSC, it follows average of two current references, which is represented by (17) and (20). At the same time the total output current always follows $i_{ref1} + i_{ref2}$.

With added current sensor, the control structure of parallel inverter system can always be kept as independent control loops. Every inverter can well regulate its output current as a sinusoidal waveform. Though the added sensor also contains sensing error, it will not affect the controller function.

IV. Experimental Verification

An experimental testbed has been implemented with two 1kW, 380V input, 120V output grid-connected full bridge inverter prototypes, where the 380V is a typical dc link voltage for dc microgrid or solar farm applications [24]. The specification is shown in TABLE IV. Each inverter module is controlled by a TI F28377s DSP individually. The connection diagram and a photo of test setup are shown in Fig. 9 (a) and (b), respectively. The resistor load is used to absorb excess power go through the isolation transformer as a consideration of experiment safety. The current sensor used is hall effect current transducers LEM LAH 25-NP, which have an accuracy of $\pm 0.3\%$. This accuracy could promise a minimized harmonic issue may be caused by the switching feedback signals.

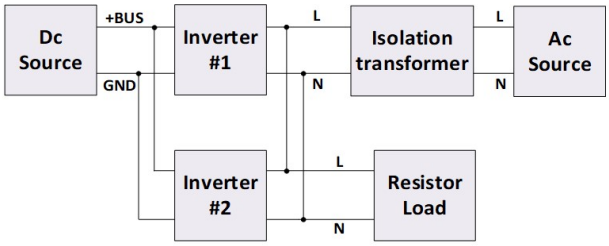
Fig. 10 shows the experimental waveforms that two inverter modules work in parallel using conventional control scheme. Though the total grid current i_G is stable and sinusoidal, the inductor currents are already unbalanced and distorted. The unbalanced currents only appear when v_{ac} is in positive half cycle, and one inductor current is almost doubled while the other one is zero. This shows a good agreement to the analytical study in section II. According to equations (11) and (12), how the two inverters share the unbalanced currents is depending on the value of K_{ref}. In the simulation study, K_{ref} is set to a fixed value, so the unbalanced currents are periodic as shown in Fig. 4. However, in a real experiment, the sensing circuit parameters may vary due to temperature, and the performance of phase-lock-loop (who give the sinusoidal shape to the current reference), even noises could affect the value of K_{ref}. The K_{ref} fluctuating around 1.0 gives the result as shown Fig. 10.

Fig. 11 shows experimental results that two UP-PWM inverter modules work in parallel using the proposed dual current sensor method. It can be seen that the inductor currents in two inverter modules are well balanced under different load conditions. Measured by power analyzer, at rating of 700w each, the gird current THD is 1.72% and harmonic of each order can fulfill power quality standard. Thus, with proposed method, full bridge UP-PWM inverters can be applied in parallel-operation.

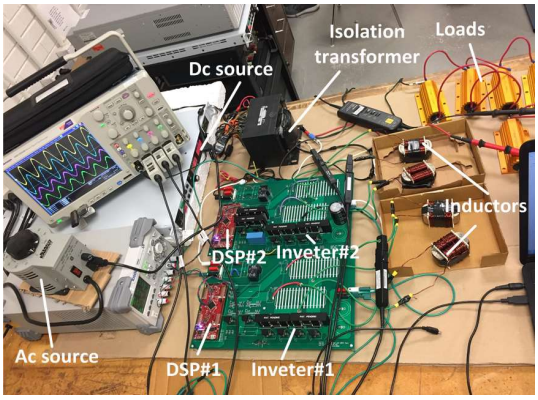
It also can be seen in Fig. 11 that current ripples of inductor currents are different in their positive and negative half cycles.

TABLE IV
SPECIFICATIONS OF EXPERIMENTAL TESTBED

Parameter	Value	Parameter	Value
$V_{ac\text{-}rms}$	120 V	V_{DC}	380 V
Po	2 kW (1 kW each)	f_{sw}	20 kHz
L_{11}, L_{12}, L_{21}, L_{22}	2 mH	k_p	0.07
		k_p	350



(a)



(b)

Fig. 9 Experimental setup, (a) connection diagram, and (b) testing platform.

When the inductor is SC, as mentioned in Section II, it appears a larger ripple, which is the actual switching ripple. In the other half cycle, when the inductor is NSC, it shows current ripple as half of grid current. The grid current ripple is smaller due to the interleaving effect when there is a phase shift between the PWM signals of two inverters. Thus, the NSC inductor current shows a smaller ripple. Fig. 12 shows the experimental waveforms of inductor current ripples, where i_{L12} and i_{L22} are SC inductor currents and i_{L11} is one of NSC inductor currents. The different current ripples in positive and negative cycles only appear on the inductor current, instead of grid current, which is harmless to the grid. And for the grid current, it always shows the interleaved current with smaller ripple in both positive and negative cycles.

From equations (15) – (20), we can see that while SC inductor currents can strictly follow their own current references, the NSC inductor will just simply share the total current. It means, if the paralleled inverters are at different ratings, the NSC inductor currents cannot be guaranteed to work at its rated power. The experimental result that two UP-

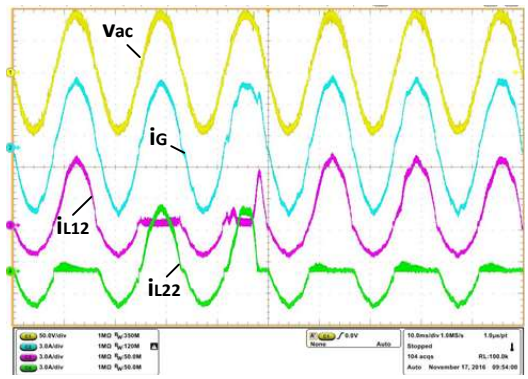
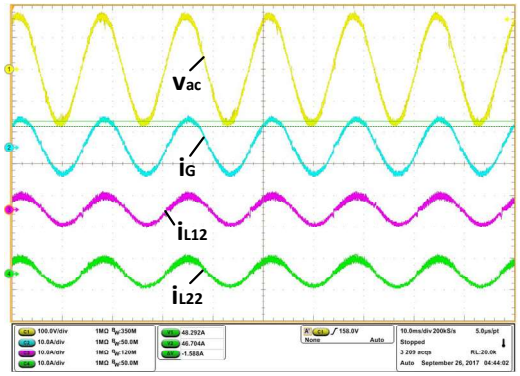
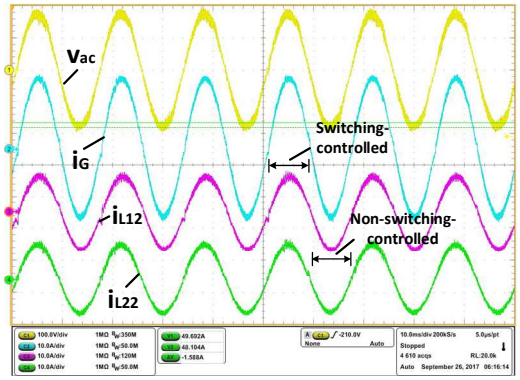


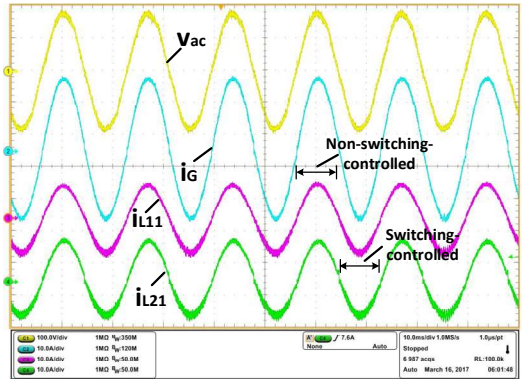
Fig. 10 Experimental waveforms of two inverters working in parallel using conventional scheme.



(a)



(b)



(c)

Fig. 11 Experimental waveforms of two inverters working in parallel with proposed dual current sensor method: (a) rated at 400W each, (b) 700W each with showing i_{L12} and i_{L22}, (c) 1000W each with showing i_{L11} and i_{L21}.

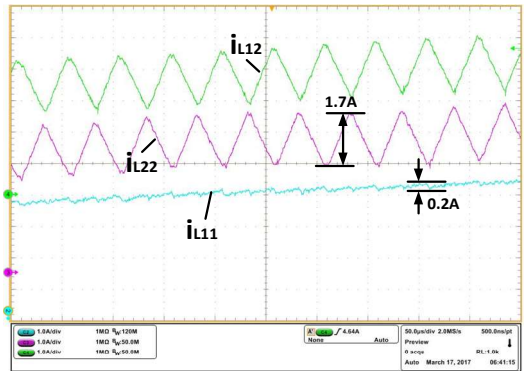


Fig. 12 Experimental waveforms of inductor current ripples.

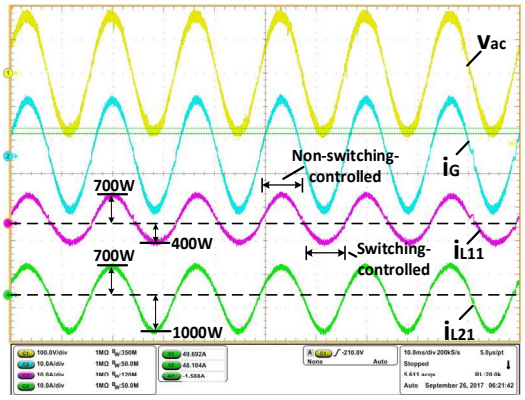


Fig. 13 Experimental waveforms that two inverters with different ratings operate in parallel with proposed method, inverter#1 is given a 400W reference and inverter#2 is given a 1000W reference.

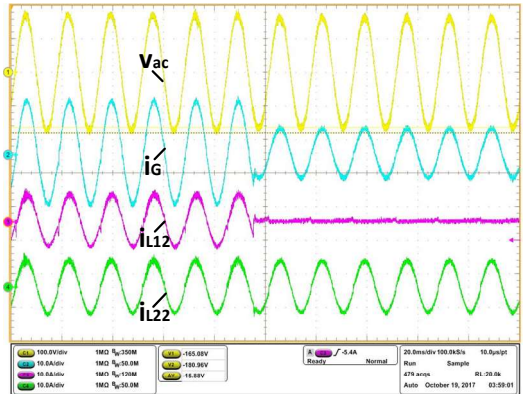


Fig. 14 Experimental waveforms that one of the parallel-operated inverters is in outage.

PWM inverters operating in parallel with different power rating is shown in Fig. 13. Inverter #1 is set to operate at 400W while inverter #2 is set to 1000W. It can be seen that when the inductor current is SC, it follows its own reference, when the inductor current is NSC, it equally shares the grid current with the other NSC inductor current. This shows one limitation of UP-PWM inverter in parallel operation that the inverters must be in same rating, otherwise the inverters with lower rating will be over current. It is still suitable for modular inverter applications, since the modules are identical to each other, as

a requirement of mass production.

Fig. 14 shows the experimental result that one of the parallel-operated inverters is out of service. At a preset moment, inverter #1 is disconnected (all four switches are turned off). It can be seen that, after one inverter being turned off, the other inverter can still work steadily, even at transient.

V. CONCLUSION

The paper studied the parallel-operation of grid-connected UP-PWM inverters with common dc bus. The problem of unbalanced inductor currents in parallel-operated UP-PWM inverters was studied by equivalent circuit and control loop analysis. The idea of Switched-Controlled (SC) and Non-Switch-Controlled (NSC) inductor, which is resulted by the nature of unipolar switching, was proposed to explain the current unbalance problem. Based on the analysis, the dual current sensor technique was established to solve the unbalanced inductor current problem. The concept is to add one more current sensor to measure both of two split inductor currents in each inverter, and select feedback signal alternately in different switching modes. By keeping the feedback signal from SC inductor current, the current unbalance problem can be solved. Analytically and experimentally verifications was demonstrated to verify the found solution and analysis. The study in this paper proves that, by simply adding a current sensor to each inverter module, it is possible to apply UP-PWM inverters in parallel-operation while keeping the advantages of high efficiency and small output chokes without changing topology or modulation method.

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