A Delay-Tolerable Master-Slave Current-Sharing Control Scheme for Parallel-Operated Interfacing Inverters with Low-Bandwidth Communication

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***Abstract* -- Parallel-operated inverters with common dc and ac bus can be used as interface for dc systems connecting to an ac network. High cost and complicated wiring of communication are main drawbacks of communication-based current-sharing methods for parallel system. Many new communication tools, e.g. Power Line Communication (PLC), Bluetooth and Zigbee modules, are cheap and require no extra wire connection, but have low communication bandwidth and low data rate, which result a large communication delay and zero-order-hold period that could cause stability issues if used to transmit control signals. This paper presents a method to mitigate the instability issue caused by communication effects, in parallel gird-tied inverter system with master-slave current-sharing control. Firstly, the master-slave current-sharing control scheme is introduced. Then, the influence of communication delay and zero-order-hold on the system is analyzed. And design criteria to reduce the influence of low-bandwidth communication (LBCom) is studied and determined. New approaches, by designing current reference low-pass-filter and voltage feed-forward loop in slave modules, are introduced. Performance of proposed control structure and design criteria are experimentally verified. With the proposed method, LBCom tools can be applied to systems with master-slave control architecture, while keeping the robustness and transient performance, with improved modularity and operation flexibility.**

***Index Terms*-- Master-Slave control, Parallel inverter, Low-bandwidth communication, Delay effects, Time delay**

I. NOMENCLATURE

α	System overall open-loop gain
β	Ratio of voltage controller integral gain over proportional gain
C	Dc link capacitance
err	Dc link voltage error
f_{sw}	Switching frequency
$I_{\mathrm{G,rms}}$	RMS value of total current injected into the grid
I_{fw}	Output of slave feedforward controller
I_{refn}	The current magnitude reference for n$^{\mathrm{th}}$ inverter
i_{n}	Output current of n$^{\mathrm{th}}$ inverter
$I_{\mathrm{n,rms}}$	RMS value of output current of n$^{\mathrm{th}}$ inverter
K	Linearized feedforward gain
K_{fw}	Feedforward coefficient
k_{p}	Proportional gain of voltage PI controller
k_{i}	Integral gain of voltage PI controller
L_{nm}	m$^{\mathrm{th}}$ inductance of n$^{\mathrm{th}}$ inverter
P_{input}	Input power
t_{lpf}	Current reference low pass filter time constant
Δt_1	Communication transmission delay
Δt_2	Zero-order-hold sample interval
V_{dc}	Dc link voltage
ΔV_{dc}	Amplitude of dc link voltage ripple
$V_{\mathrm{dc,ref}}$	Reference of dc link voltage
v_G	Grid voltage
$V_{G,rms}$	RMS value of Grid voltage

II. INTRODUCTION

More and more distributed dc systems, like solar farms and dc microgrids, are connecting to the utility grid as an important way to harvest renewable energy, and will keep playing an important role in the future smart grid. Voltage source inverter (VSI) is critical to interface these distributed dc systems with utility ac grid [2]. With the growing demands of dc systems, the needs of VSI with larger capacity and higher flexibility have become significant. In most of dc applications, a large-capacity centralized interfacing inverter is commonly used as interface between dc bus and utility grid [3]. Besides regulating the output current to be sinusoidal and synchronized to the grid voltage, the interfacing inverter is also responsible of keeping dc bus voltage stable towards variation of solar power output. The single-operated centralized inverter has many restrictions in terms of flexibility, reliability and scalability, and will face the problem of light load operating and higher loss due to using of high current power semiconductors or bulky passive components, especially for systems with fluctuating power flow [4]. Using close-range parallel-operated inverters to replace a central inverter, as shown in Fig. 1, can reduce the stress of high current by distributing power into multiple modules. Thus parallel-operated inverters take more advantages in some cases that the power can be shared with multiple VSI modules with improved redundancy and flexibility [5]-[8]. Such parallel module design has been adopted by many commercial products in PV [9] and UPS applications [10].

To achieve power sharing among parallel-operated converters, droop characteristic-based control and active load sharing control technologies are commonly used [11]. While droop control taking advantages of easy implementation and high modularity [12]-[13], active load sharing control has better performance in terms of voltage regulation and power sharing, but requires communication among paralleled modules to share information of current reference or current-sharing error [15]-[17]. Master-slave architecture is one of commonly used architectures, which has respective current loop controller in each slave module and a common voltage

This is an updated version of conference paper [1]. This new version includes further analysis and updated experimental results.

controller in master module. Equal current sharing and precise voltage regulation can be achieved simultaneously. This paper is mainly focusing on master-slave control for modular design where compatibility issue is not considered. With master-slave architecture that current reference of each module is given by the master, many smart features can be enabled, e.g. dynamic power sharing [6]. With master selection techniques like automatic master [18] and democratic master [19], plug-n-play and high reliability can also be achieved on master-slave-controlled system. A disadvantage of communication-based control is that it requires interconnection of control signals that relies on high-bandwidth and precise communication, which can be costly (for communication devices, cable and hubs) and the wiring will reduce modularity and may introduce significant noises into control signals. Thus, the master-slave control is commonly be applied only in a close range [7].

With development of communication technology, new communication tools are available on the market, e.g. Power Line Communication (PLC) module, Bluetooth module and Zigbee communication module. These tools have been widely used in Internet of Things (IOT) and smart grid applications, due to their features of no extra wires, low cost, operation flexibility and distributed intelligence. At the same time, these digital communication modules are equipped with built-in checking rules which are reliable even in a high EMI environment. Furthermore, a single digital communication channel can be multiplexed to transmit several different signals, e.g. amplitude, phase or control commands. It is a trend to use such modular communication devices in the future smart grid [20]-[21]. Combining master-slave controlled parallel inverter system with these new communication technologies can omit the physical wire connection and provide a reliable communication channel resistive to environmental noise. The ad-hoc communication network also enables plug-n-play feature of converter modules. However, as a tradeoff of low-cost, these new communication tools are featured as low-bandwidth and low-rate, which limits the usage of these advanced communication tools mainly in high level coordination, e.g. manual control and data collection, instead of in the control layer. Fig. 2 (a) shows the common logic structure of a parallel inverter system [22]. Communication network C1 can be implemented with LBCom tools. However, the communication network of control layer C2 is usually based on high-bandwidth communication, e.g. analogue or fiber optic, even sometime using sensors to directly sense the output of another converter. Using two separate communication networks is neither convenient nor economic. Fig. 2 (b) shows a case of proposed parallel inverter system combining two communication networks C1 and C2 into one LBCom network (using Zigbee modules), which can lead to higher modularity and lower cost.

Apparently, the challenge is how to overcome the impact of LBCom delay. The communication delay Δt_1 and zero-order-hold (ZOH) step Δt_2 of LBCom are shown in Fig. 3. Large delay and ZOH added in the control loop can result an oscillation even collapse of a master-slave controlled system. The stability issue caused by communication delay has been a

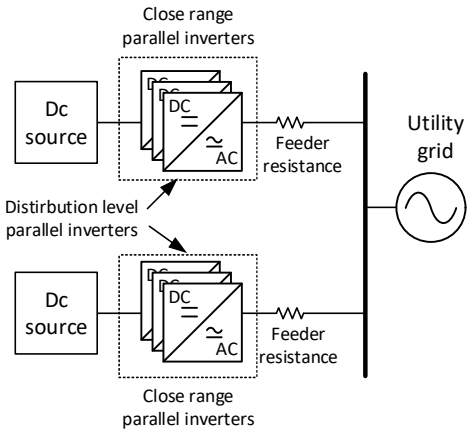


Fig. 1 Application of close-range parallel inverter system.

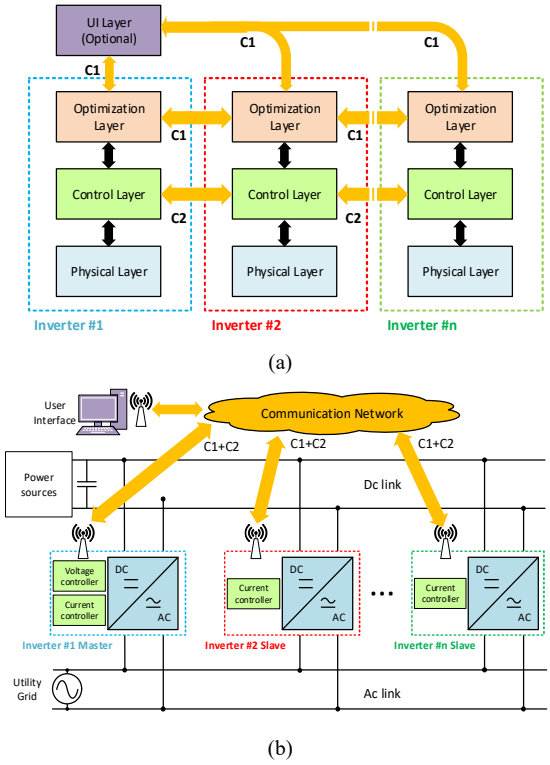


Fig. 2 (a) Typical logical structure of parallel inverter system with two sperate communication networks C1 and C2. (b) Proposed master-slave controlled parallel inverter system with one LBCom network.

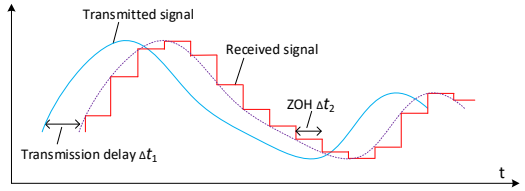


Fig. 3 Delays of low-bandwidth digital communication.

topic of research in many areas [23]-[28]. In most of the researches, only pure delay is considered. However, ZOH Δt_2 can be much larger than Δt_1 as shown in Fig. 3, which should also be taken into consideration in the stability analysis,

especially when the communication channel is multiplexed for several signals. In this paper, a model considering both pure delay and ZOH is established and Nyquist diagram which can accurately reflecting effect of both time delay and ZOH is used for stability analysis. Moreover, while previous studies mainly focusing on obtaining the delay bound, this paper provides new approaches to actively increase the system tolerable bound of communication delays.

The contribution of this paper is to propose a design method for master-slave current-sharing control of paralleled inverters to actively increase the tolerability to LBCom impacts. The proposed control scheme is to achieve the following features, 1) Cost-effective low-bandwidth communication device is adopted to transmit current reference from master module to slave modules, and system stability can stand with the impact of communication delay and ZOH, even when towards very high load dynamic changes. 2) Grid current can be evenly shared by inverter modules at steady state. At transient, the inverter modules can be decoupled to avoid oscillation and instability. 3) System is robust to varying communication delay and high EMI noises. In the paper, firstly, the master-slave current-sharing control is introduced. A transfer function model is established. Secondly, the influence of communication delay and ZOH on the parallel inverter system is analyzed. Methods to reduce the influence of LBCom are studied and compared. A slave module Low-Pass-Filter (LPF), which decouples slave modules from master module at transient, is proposed. And a slave module Feed-Forward Loop (FFL) controller that is similar to an adaptive voltage droop controller is introduced, which utilize local compensation to improve the transient performance, to provide system larger stable margin and release master's stress at transient. Performance of proposed control scheme and design criteria are demonstrated with simulation results and experimentally verified on two 800w/120V inverter modules.

III. Model of Master-Slave Controlled Inverters

A typical interfacing inverter system, such as solar farm or dc microgrid interfacing inverter commonly has two control targets, dc bus voltage and ac output current. The two control targets can be achieved by using a double-loop control structure that the outer loop regulates dc link voltage by generating current reference to the inner loop which controls output current [29]. In a input-parallel output-parallel inverter system (with first-order L filter), as shown in Fig. 4, the inputs of inverters are connected to a common dc bus; outputs are gathered together and then get connected to a common grid feeder branch. For this parallel inverter system, a master-slave architecture can be applied to implement the double-loop control. The voltage controller is located in the master inverter module, usually is implemented by a PI controller with low control bandwidth. It monitors the error of dc link voltage and generate current amplitude reference accordingly to all inverter modules. All inverter modules have an independent Phase-Locked Loop (PLL) and current controller. Thus their output currents can be regulated sinusoidal and synchronized to the grid voltage. The current controller is usually

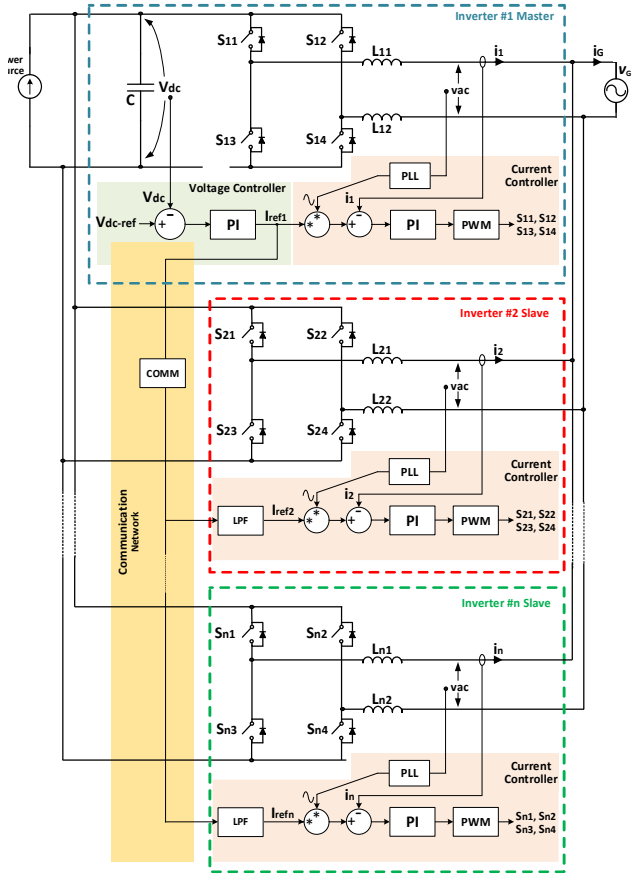


Fig. 4 Overview of a typical input-parallel output-parallel inverter system with master-slave control architecture.

implemented by PI or hysteresis controller with fast dynamic response [2]. In this paper, simple stationary frame PI controller is used for inner current loop. The controller for each converter is independent (without any PWM synchronization), hence each module can work as a standalone device or in parallel with other devices.

In the master-slave architecture, output of voltage controller is given to all modules. Thus, at steady state, modules can equally share the power. The output of voltage controller, which is the current reference, is given to slave modules through a communication network with a significant delay and Zero-Order Hold (ZOH) when LBCom is used. At the same time, the current reference transmission inside the master module bypasses communication and has almost no delay. Hence the actual current references received by inverter modules are not synchronized. The unsynchronized current references will significantly affect the performance of voltage loop, for example, dc link voltage oscillation even collapse. The proposed control method could reduce the influence of LBCom, by redesigning slave module LPF and adding an FFL.

Considering the case that consists of one master module and one slave module, the control diagrams are shown in Fig. 5, of which (a) is the ideal system neglecting communication delay effect; (b) shows the system considering communication impact; (c) shows the proposed system with voltage FFL in slave module. The blocks in blue dash box are processed in

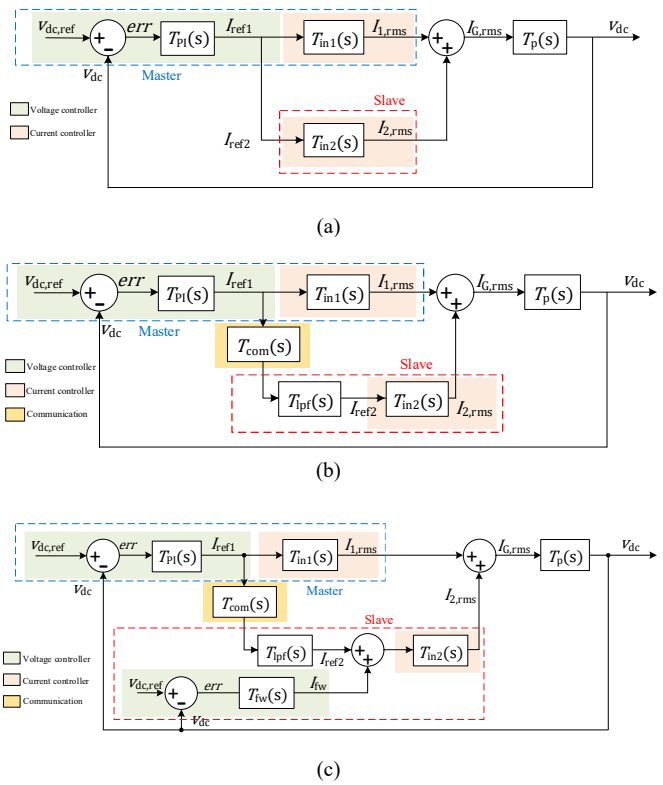


Fig. 5 Control diagram of one master module and one slave module operating in parallel, (a) without communication impact, (b) with communication impact, (c) with voltage feed-forward loop in slave module.

master module and the blocks in red dash box are processed in slave module.

The master voltage controller is usually implemented by a PI controller, which can be represented as (1), where k_p is proportional gain and k_i is integral gain. The design of k_p and k_i mainly takes consideration of making the voltage loop crossover frequency to be ten times smaller than the double-line frequency to avoid 2nd-order harmonic [30].

$$T_{PI}(s) = -\frac{k_p s + k_i}{s} \tag{1}$$

Due to the power stage transfer function as given in equation (3) having a negative sign, the voltage controller also needs to have a negative sign to make the system a negative feedback system.

T_{in1} and T_{in2} are transfer functions of current loop of master and slave modules, respectively. The dynamic response of inner current loop is much faster than outer voltage loop, so the transfer functions of current loop can be considered as a constant value for study on the outer loop. To get the Root Mean Square (RMS) value of output current,

$$T_{in1}(s) = T_{in2}(s) = \frac{1}{\sqrt{2}} \tag{2}$$

The transfer function of power stage can be derived as (3),

$$T_p(s) = \frac{\widetilde{v_{dc}}}{\widetilde{i_{G,}rms}} = -\frac{V_{G,RMS}}{V_{dc}Cs} \tag{3}$$

where the parameters are indicated as in Fig. 4.

The communication stage consists of a time delay and a ZOH is as given in (4), where Δt_1 and Δt_2 are defined in Fig. 3.

$$T_{com}(s) = T_{delay}(s) \times T_{ZOH}(s) = e^{-\Delta t_1 s} \times \frac{1-e^{-\Delta t_2 s}}{\Delta t_2 s} \tag{4}$$

A first-order LPF is used for the LPF stage as shown in (5). t_{lpf} is filter time constant, when $t_{lpf} = 0$, the LPF is bypassed.

$$T_{lpf}(s) = \frac{1}{t_{lpf}s+1} \tag{5}$$

The FFL can be considered as an I-V based voltage droop controller,

$$T_{fw}(s) = \frac{\widetilde{i_{fw}}(S)}{\widetilde{err}(S)} = -K \tag{6}$$

For an ideal system without considering communication effect as in Fig. 5 (a), the overall open-loop transfer function of the system is,

$$T_{ol,i}(s) = T_{PI}T_p(T_{in1} + T_{in2}) = \frac{\sqrt{2}(V_{G,RMS}k_p s + V_{G,RMS}k_i)}{V_{dc}Cs^2} \tag{7}$$

For a system considering effect of LBCom as in Fig. 5 (b), the overall open-loop transfer function is,

$$T_{ol}(s) = T_{PI}T_p\left(T_{in1} + T_{com}T_{lpf}T_{in2}\right)$$

$$= \frac{V_{G,RMS}k_p s + V_{G,RMS}k_i}{\sqrt{2}V_{dc}Cs^2} \times \left(1 + \frac{e^{-\Delta t_1 s} - e^{-(\Delta t_1 + \Delta t_2)s}}{t_{lpf}\Delta t_2 s^2 + \Delta t_2 s}\right) \tag{8}$$

For the system has both LPF and FFL as shown in Fig. 5 (c), the overall open-loop transfer function is,

$$T_{ol}(s) = T_p\left(T_{PI}T_{in1} + T_{PI}T_{com}T_{lpf}T_{in2} + T_{fw}T_{in2}\right)$$

$$= \frac{V_{G,RMS}}{\sqrt{2}V_{dc}Cs}\left[\frac{k_p s + k_i}{s} \times \left(1 + \frac{e^{-\Delta t_1 s} - e^{-(\Delta t_1 + \Delta t_2)s}}{t_{lpf}\Delta t_2 s^2 + \Delta t_2 s}\right) - K\right] \tag{9}$$

These derived transfer functions can be used to determine the stability of the systems.

IV. Parameter Design to Reduce the Effect of LBCom

In this section, the stabilities of several cases of master-slave controlled parallel inverter systems are analyzed using Nyquist diagram. From (7) to (9), for all the systems, the number of poles on the right complex plane is zero. According to Nyquist stability criterion, the Nyquist contour should not include critical point (-1, j0) to guarantee stability.

Table I System Specifications

Parameters	Value	Parameters	Value
$V_{dc,ref}$	300 V	Δt_1	15 ms
C	1.5 mF	Δt_2	34 ms
$V_{G,RMS}$	120 V	k_p	0.008
P_{input}	1.5 kW	k_i	1.25

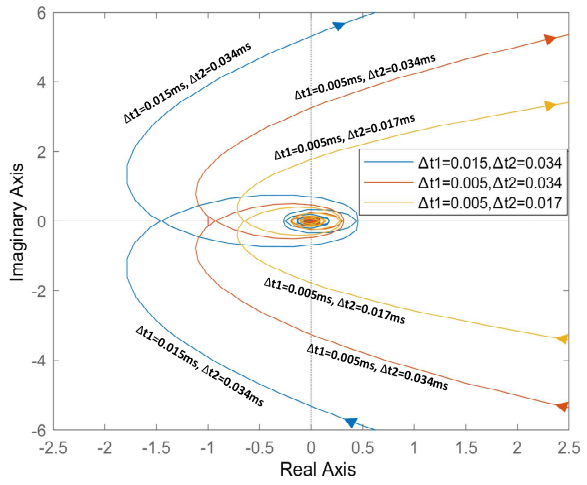


Fig. 6 Nyquist diagrams of system open-loop transfer function with communication effect and no LPF.

A. *Communication effect on system stability*

For a typical system with parameters as shown in TABLE I, for an ideal system neglecting LBCom impact, based on (7), the system is apparently closed-loop stable.

However, for the system considering communication impact, as modeled in (8), while LPF is bypassed, the Nyquist diagram is shown in Fig. 6. Due to the exponential terms from communication impact, Nyquist contour will rotate around origin. The contour has infinite intersection points with real axis. Therefore, only when all intersection points are on right side of critical point (-1, j0) can the system be closed-loop stable. In Fig. 6, with large communication delay and ZOH, an intersection point moves to the left of (-1, j0), thus the system becomes closed-loop unstable, due to the influence of communication. Thus, an originally stable system can become instable when communication effect is involved. It is important to properly design the control system to mitigate communication influence.

Fig. 6 also shows the Nyquist contours with different communication delays and ZOH steps. It can be seen that, larger delay or ZOH step will make the left intersection point further to left, which will lead the system less likely become stable.

B. *Voltage loop controller design*

System transfer function (8) can be rewritten as,

$$T_{ol}(s) = \alpha \times \left(\frac{s+\beta}{s^2}\right) \times \left(1 + \frac{e^{-\Delta t_1 s} - e^{-(\Delta t_1 + \Delta t_2)s} s}{t_{lpf}\Delta t_2 s^2 + \Delta t_2 s}\right) \quad (10)$$

where

$$\alpha = \frac{V_{G,RMS} k_p}{\sqrt{2} V_{dc} C} \quad (11)$$

and

$$\beta = \frac{k_i}{k_p} \quad (12)$$

While communication delay Δt_1 and ZOH step Δt_2 are predetermined values, which are considered fixed. Thus, according to (10), the parameters can be designed are α, β and t_{lpf}. α, β are related to PI parameters and t_{lpf} is LPF time constant. Parameter α represents system open-loop gain. By reducing α, the whole Nyquist contour will scale down to the origin, which means all intersection points on real axis will move closer to the origin. When α is small enough that all intersection points are on right side of critical point (-1, j0), the system becomes stable.

Fig. 7 shows the Nyquist diagram with different gain α. The original system described by TABLE I, of which the open loop gain $\alpha = 1.5$, is unstable as indicated by blue line in Fig. 7. When the loop gain decreases, the system becomes more stable. When $\alpha = 1.0$, the system is close to the critical stable point. And when α further decreased to 0.5, the system becomes stable. Hence, by reducing system open-loop gain, the system can be stable even delay and ZOH are involved. However, the reduction of open-loop gain will weaken overall system's ability of transient response.

In (10), $V_{G,RMS}$ and V_{dc} are fixed, and C is commonly designed to meet the requirement of dc link voltage ripple. While β is kept as a constant, α can be changed by simultaneously scaling down k_p and k_i, or changing the sensor gain if sensor gain is considered.

Besides reducing open-loop gain α, reducing β by keeping k_p the same and reducing k_i could also slow down the system response to avoid oscillation between parallel-operated inverters, as shown in Fig. 8. Reducing β has very similar effect as reducing α, which will also reduce controller's bandwidth. Hence, in the following paper, we mainly use α as indicator of bandwidth of voltage controller, while β being kept constant.

Thus, by properly designing voltage controller, system can be kept stable towards communication effects. It requires to reduce control bandwidth of voltage controller to avoid potential oscillation among parallel-operated inverters, which will sacrifice dynamic performance of voltage regulation e.g. settling time and overshoot.

C. *Low-pass filter design*

Modifying α and β which are basically modifying parameters of voltage controller, will influence the performance of overall voltage loop. Thus, mitigating communication impact by only designing α and β will inevitably slow down the voltage regulation performance. One of proposed solutions is to modify slave module controllers. As shown in the control block diagram Fig. 5 (b), an LPF is added to each slave module. In the proposed method, the master module can keep the same control performance as a single-operated inverter and slave modules should have lower control bandwidth towards voltage change thus the modules are decoupled and the oscillation can be avoided.

The current reference received by slave modules are piecewise-constant signals due to ZOH. The slave module controller is commonly equipped with an LPF with relatively high cut-off frequency to smooth the received current reference signal. By simply redesigning the LPF to reduce the

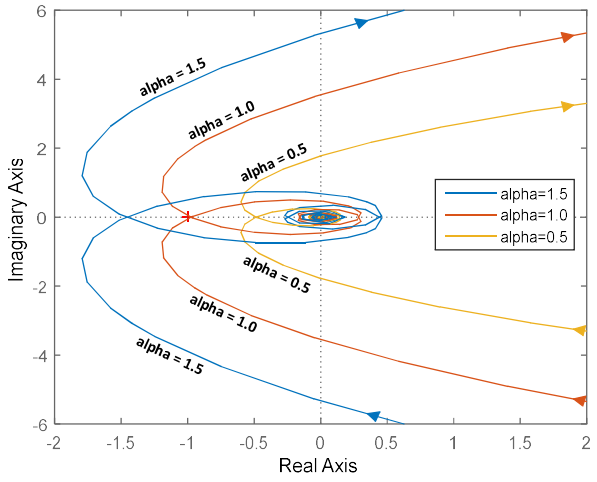


Fig. 7 Nyquist diagram of system open-loop transfer function with communication effect with different α.

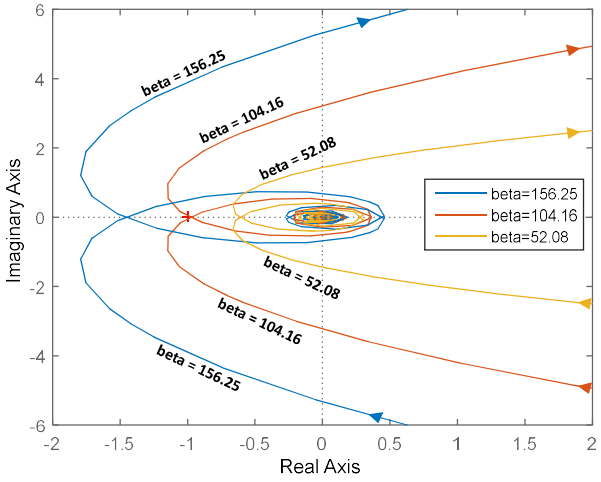


Fig. 8 Nyquist diagram of system open-loop transfer function with communication effect with different β.

cut-off frequency, impact of wireless digital communication can be mitigated.

The received current reference signal at slave module go through the LPF firstly, then be taken by current controller. When the LPF is properly designed, slave modules can only get the low frequency signal in the current reference, which is enough for the modules to achieve power sharing purpose at steady state. At the same time, the relatively high frequency signals, which could cause oscillation or instability, are filtered. Thus, master module and slave modules contribute to dc link voltage in different bandwidths. In the proposed structure, power exchanges during transient, which requires high control bandwidth, will be mainly taken care by the master module. Power exchanges at steady state will be shared among all slave modules and master module.

Therefore, with proposed structure, for voltage regulation, the master module keeps the same ability of transient response as a single-operated inverter. At steady state, power will be evenly shared among all modules. By properly designing LPF, communication impact can be mitigated while keeping voltage

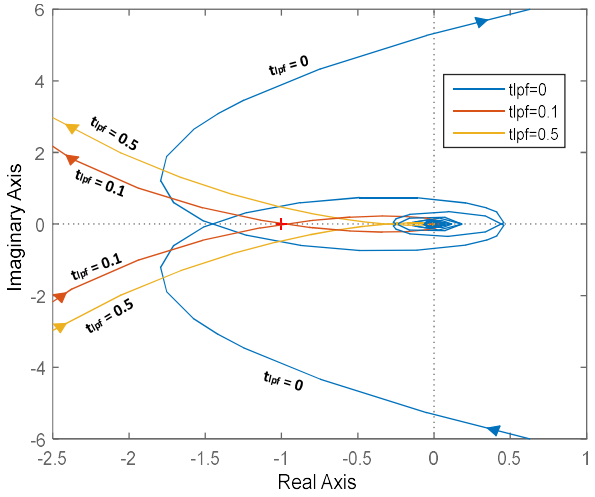


Fig. 9 Nyquist diagram of system open-loop transfer function with communication effect with different t_{lpf} in slave module.

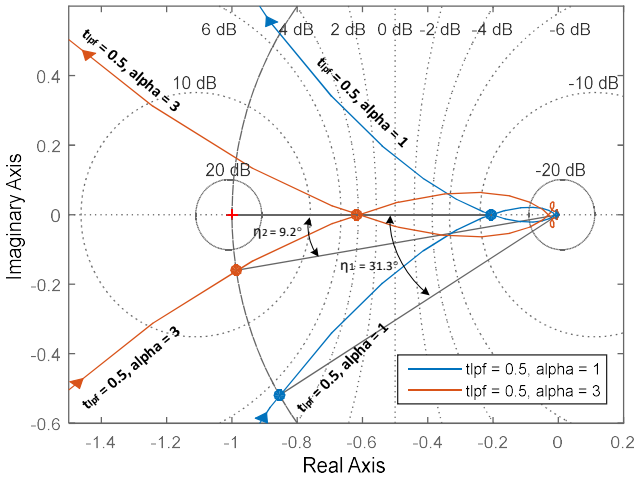


Fig. 10 Nyquist diagram of system open-loop transfer function with delay effect with different α when LPF in slave module is functioning.

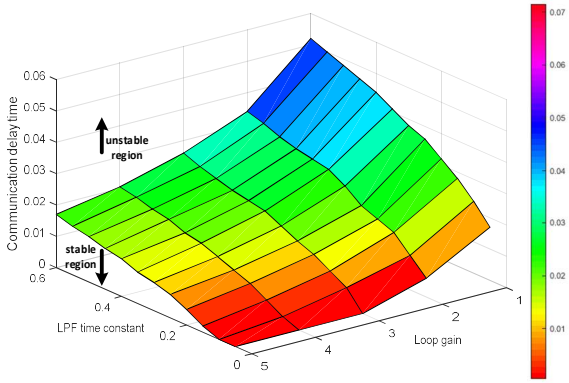


Fig. 11 Bound for the system operating in stable region, β is fixed to 156.25, Δt_2 is fixed to 0.034s.

regulation with a relatively fast-dynamic response.

As shown in (5), a simple first-order LPF is used in the study. To smoothing piecewise-constant signal, an LPF with relatively high cut-off frequency is adequate. For example,

when the ZOH sample interval Δt_2 = 0.034ms, a t_{lpf} = 0.05s is enough to smooth the piecewise-constant signal. However, to mitigating communication impact, a lower LPF cut-off frequency is required.

Fig. 9 shows the Nyquist diagram of system open-loop transfer function (8) with different LPF time constants t_{lpf}. While increasing t_{lpf}, which means lowering the LPF crossover frequency, Nyquist diagram intersections with real axis get closer to the origin. When t_{lpf} = 0.1s, the system is near to the critical point of being stable. When t_{lpf} = 0.5s, the system is stable with margin.

According to Fig. 9, an LPF with larger time constant t_{lpf} in slave module makes the system more stable and robust. A t_{lpf} tending to infinity means the slave modules will keep a constant current output as their initial settings which are independent from voltage controller. At this point, only master module is involved in voltage control. Thus, the system is as stable and robust as a single operated inverter. However, this has distorted the current sharing purpose of parallel operation. An LPF with cut-off frequency that 5-10 times smaller than the voltage loop natural frequency ω_n is rational.

Furthermore, with LPF in slave module, there is more space for PI controller design. As shown in Fig. 7, when LPF is missing, system can only be stable when open-loop gain α is less than 1.0. In

Fig. 10, with LPF t_{lpf}= 0.5s, the system becomes stable even for α = 3.0, with enough gain margin. Increased open-loop gain with slave module LPF can provide a better transient performance while keeping the system stable.

Assuming β and Δt_2 are fixed, a bound of system operating in stable region, which is decided by loop gain α, LPF time constant t_{lpf}, and communication delay time Δt_1, can be obtained. The surface in Fig. 11 shows the bound. The region above the surface indicates system being unstable. The region below the surface indicates system being stable. It can be seen that, when LPF is absent or the time constant is too small, the system can only tolerate a very short communication delay, at a prerequisite of low loop gain. When LPF is added, the system can tolerate longer communication delay even with a larger loop gain.

However, though the LPF can make systems with communication effect theoretically stable and has enough gain margin as shown in

Fig. 10, the phase margins which are $\eta_1 = 31.3^\circ$ and $\eta_2 = 9.2^\circ$ still cannot meet the engineering requirement which is $40^\circ \sim 50^\circ$ [31]. Furthermore, as LPF is introduced to slave modules, the master could provide much more power than the slave modules at transient. While the power that master module can provide is limited, considering this current saturation characteristic, at transient the system may have a large voltage sag or swell even a stability issue.

D. Feed-forward loop design

As mentioned above, by solely adding LPF in slave modules, the phase margin of system is insufficient, and a high-rating master module may be required. Like neighboring information is used to compensate steady state error in droop-

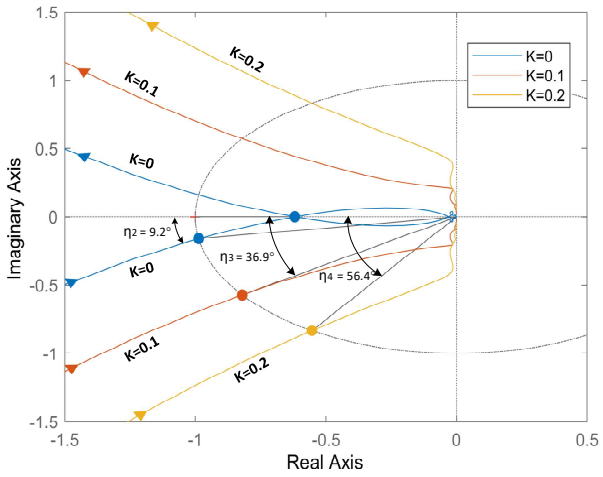


Fig. 12 Nyquist diagram of system open-loop transfer function with both LPF and FFL in slave module, while t_{lpf} = 0.5 s and α = 3.

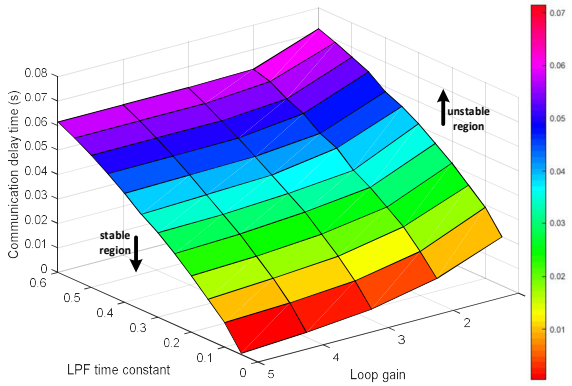


Fig. 13 Bound for the system stable region while FFL is involved, β is fixed to 156.25, Δt_2 is fixed to 0.034s and K is fixed to 0.0005.

controlled system, local compensation can be used to improve transient performance in master-slave-controlled system. A voltage feed-forward controller is added to each slave module.

Fig. 5 (c) shows the control diagram that feed-forward loop is added to slave module. To obtain the characteristic that has high feed-forward gain at large voltage error but low gain at small voltage error, any power function can be used for the feed-forward controller. Here the feed-forward controller is selected as a cube function with a gain -K_{fw},

$$I_{fw}(t) = -K_{fw} err(t)^3 \tag{13}$$

The linearized transfer function of the feed-forward controller, as an update of (6), is,

$$T_{fw}(s) = -K = -3K_{fw} ERR^2 \tag{14}$$

It can be seen from (13) and (14), at steady state, $ERR = 0$, feed-forward loop has no effect to the system, which means the slave module will follow the same current reference as master module. At large transient, the slave module will contribute to compensate dc link voltage error at a high gain due to the square term of ERR, which could significantly reduce the stress of master module at transient. The controller

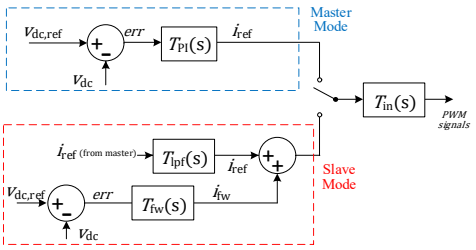


Fig. 14 Controller diagram with multi-master control ability.

is actually an adaptive feed-forward voltage droop controller, of which the gain K is self-adjusted according to ERR value.

Fig. 12 shows Nyquist diagrams based on (9) with different feed-forward parameters. It can be seen with feed-forward loop, both phase margin and gain margin of system can be increased. And Fig. 13 shows the delay bound while FFL is involved. Compared to Fig. 11, with both LPF and FFL in slave module, the tolerable delay time is increased significantly, especially when loop gain is high. Thus, with properly designed LPF and FFL, the system can be tolerable with large time delays while keeping a large stable margin and high loop gain. With a large tolerable margin of communication delay, even the delay varies, the system can still be kept in the stable region and a high loop gain can provide a better transient performance.

In Fig. 12, the phase margin increases along with increasing FFL gain. However, if the gain is over designed, the robustness of system will be reduced, and the steady state performance may be influenced. Especially, due to the steady state double line frequency ripple on dc link, a large 2nd-order harmonic can be generated if FFL is overdesigned.

To avoid FFL affecting steady state performance, the parameter selection should consider the steady state double line frequency ripple on dc link [30], which is expressed as,

$$\Delta V_{dc} = \frac{P}{4\pi f C V_{dc}} \tag{15}$$

Where P is total output power of the parallel-operated system, f is line frequency which is 60Hz in the studied system.

Assume at steady state the magnitude of 2nd-order harmonic of output current should be less than I_{2nd},

$$K_{fw}\Delta V_{dc}{}^3 < I_{2nd} \tag{16}$$

Combine (16) and (17),

$$K_{fw} < \frac{64\pi^3 f^3 C^3 V_{dc}^3 I_{2nd}}{P^3} \tag{17}$$

Thus, K_{fw} should be designed satisfying (17) to fulfill requirement of 2nd-order harmonic.

E. Master outage

In conventional master-slave control, loss of master will cause failure of whole system. With proposed slave controller, the system can still run when the master converter is down. The FFL in slave module can still form a closed voltage control loop, which is similar to an I-V droop controller, with basic power sharing and voltage regulation performance.

Furthermore, the proposed controller can also be applied to a multi-master system. All modules can be equipped with both master and slave controller, as shown in Fig. 13. Each module can be switched between master mode control and slave mode control. With proper master-selecting mechanism [18]-[19], one master will be active, and when the master module is down, one slave module will shift to master mode to send current reference to other modules.

V. Simulation and Experiment Verifications

A. Simulation Verification

The proposed scheme is simulated using PLECS. Two full-bridge VSI modules with unipolar-PWM are used in verification [32]. Simulation parameters are provided in TABLE I and II.

Fig. 15 (a) shows the simulation results of parallel inverter system with conventional master-slave control, of which the control diagram is shown in Fig. 5 (b). While communication impact being involved, when $\alpha = 1$, the system is close to the critical stable point, according to Nyquist diagram in Fig. 7. Simulation waveforms in Fig. 15 (a) show a good agreement to it, that dc link voltage and two current references for the two modules are badly oscillating.

For simulation in Fig. 15 (b) and (c), slave module LPF with $t_{lpf} = 0.5$ s is added. The oscillating system in Fig. 15 (a) become stable even with increased loop gain $\alpha = 3$, which approves Nyquist diagram in Fig. 10.

TABLE II Extra System Parameters

Parameters	Value	Parameters	Value
Baud rate	9600 bps	L_{11}, L_{12}, L_{21}, L_{22}	2 mH
P_{rate}	800 W each	f_{sw}	20 kHz

Fig. 15 (d) shows simulation results that slave module is equipped with both LPF and FFL. With properly designed FFL, at transient, though both module's outputs still have an overshoot, the oscillation is damped quickly and the power distribution among the modules are better balanced. The dc link voltage transient performance is also improved significantly.

Fig. 16 (a) and (b) shows simulation results of two parallel-operated inverters using V-I and I-V droop control respectively [14]. Secondary voltage regulation based on LBCom is adopted in the simulation, hence for both case, the dc link voltage has no steady state error. For V-I droop control, as shown in Fig. 16 (a), the settling time is longer and overshoot is larger towards transient, compared to proposed master-slave control. For I-V droop control, as shown in Fig. 16 (b), the voltage regulation is very fast. However, the output current is badly distorted by second-order harmonics, which does not occur in V-I droop control or master-slave control. And for both V-I and I-V droop control, the power sharing become unbalanced when a voltage sensing error exists (in this case, 1% voltage sensing error results a 3A current-sharing error). Master-slave control, having only one voltage controller in master module, will not have this current-sharing issue caused by voltage sensing error.

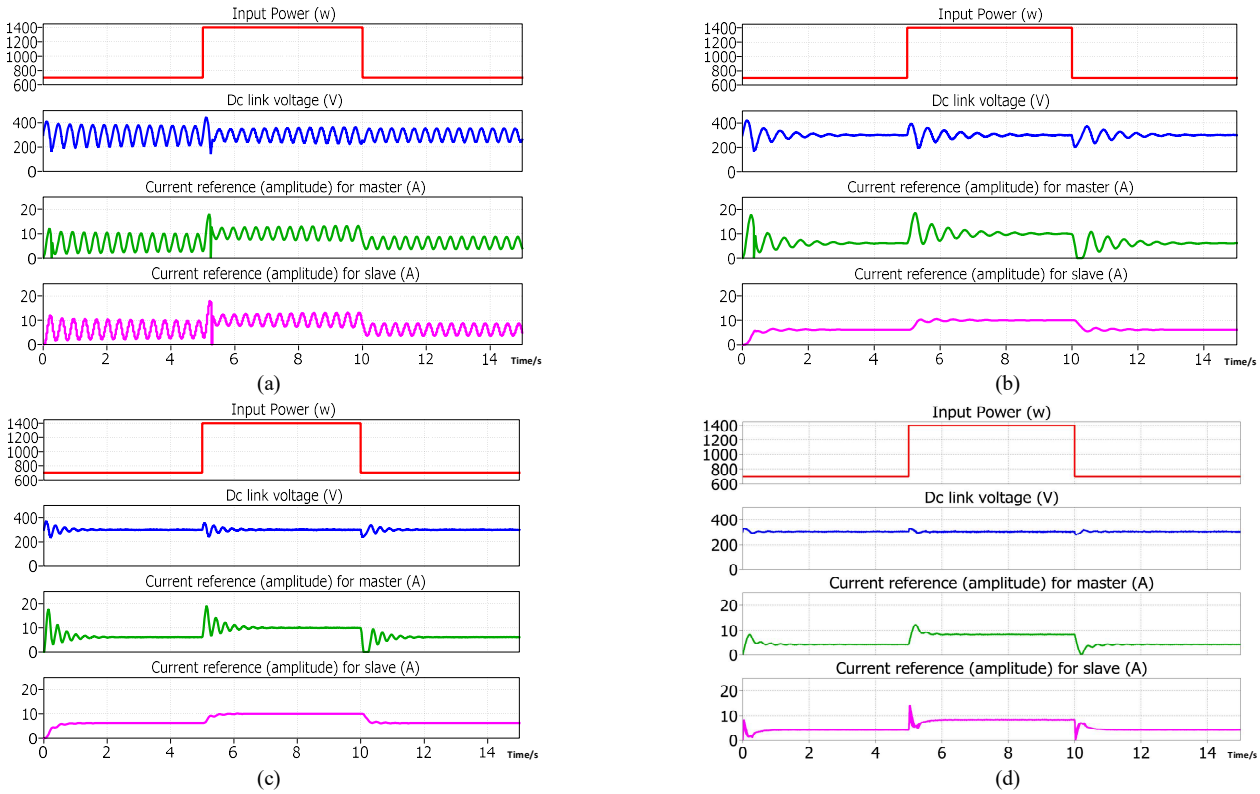


Fig. 15 Simulation results of two inverters operating in parallel with time delay $\Delta t_1 = 15$ ms, $\Delta t_2 = 34$ ms, (a) conventional master-slave control with no LPF and FFL in slave module and $\alpha = 1$, (b) modified master-slave control with LPF and no FFL in slave module, $\alpha = 1$, $t_{lpf} = 0.5$ s, (c) modified master-slave control with LPF and no FFL in slave module, $\alpha = 3$, $t_{lpf} = 0.5$ s, (d) modified master-slave control with both LPF and FFL in slave module, $\alpha = 1$, $t_{lpf} = 0.5$ s, $K_{fw} = 5e^{-4}$.

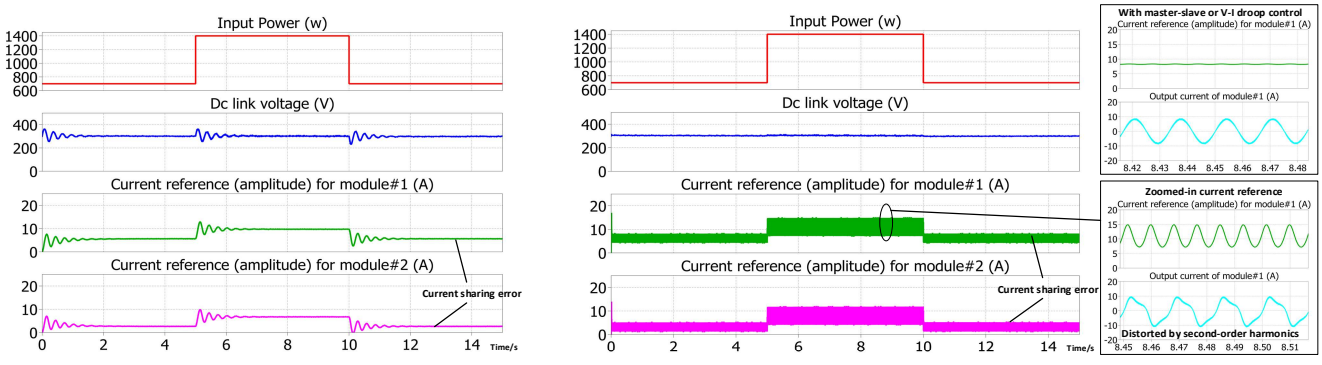
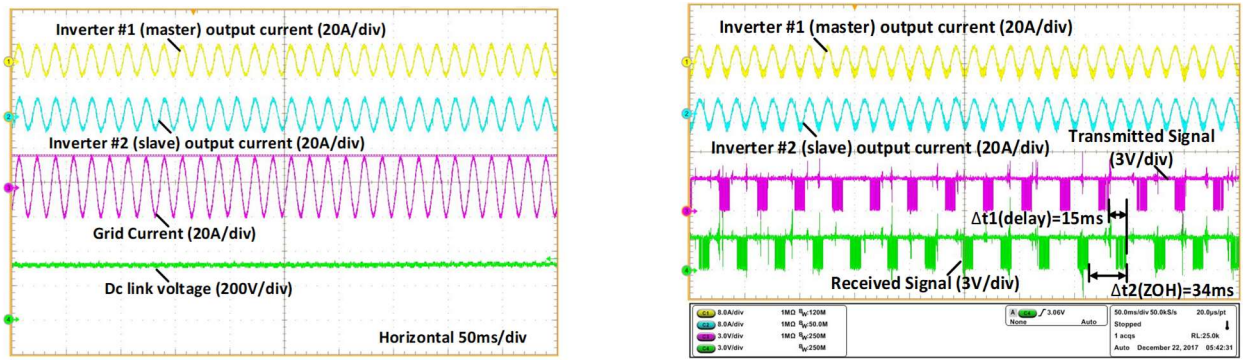


Fig. 16 Simulation results of two inverters operating in parallel using droop control with secondary voltage regulation, both droop coefficients are set to 1Ohm, and 1% voltage sensing error is considered, (a) V-I droop control, (b) I-V droop control.

B. *Experimental Verification*

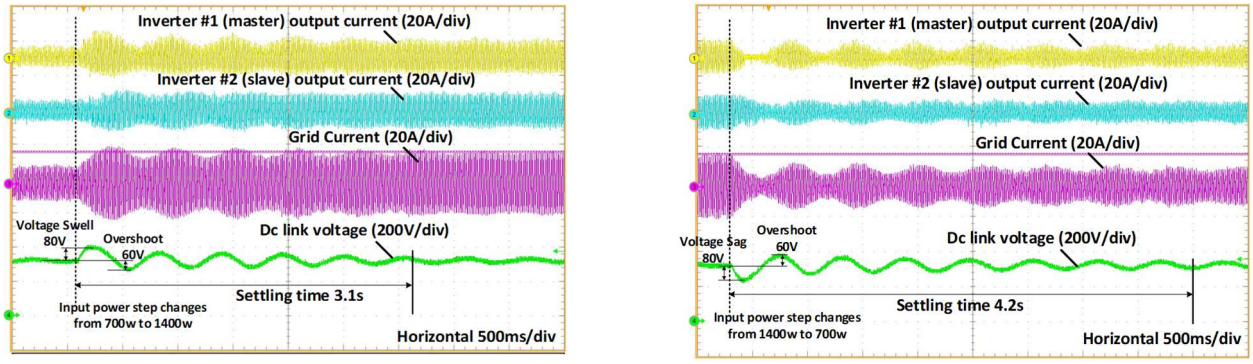
An experimental testbed has been implemented with two grid-connected full bridge inverter modules. Each inverter module is controlled by a TI F28377s DSP individually. Communication is based on DIGI Xbee 802.15.4 wireless communication module, which is based on Zigbee protocol, a wireless mesh network standard. Experiment specifications are as shown in Table I and II. Xbee modules are connected to DSPs using UART communication. The master module will periodically broadcast the current reference i_{ref} to all slave modules, of which the time interval will be the ZOH time interval. Checking mechanisms has been built into the communication protocol to guarantee the correctness of wireless digital communication, even in a high-EMI noise environment.

Fig. 17 (a) shows the experimental waveforms of system steady state performance with proposed master-slave control design. It can be seen that, the dc link voltage is well following the reference voltage, 300 V, and grid current is stable and sinusoidal which is equally shared by two inverter modules. Fig. 17 (b) shows the measured communication signals at steady state. Transmission delay Δt_1 and ZOH Δt_2 are



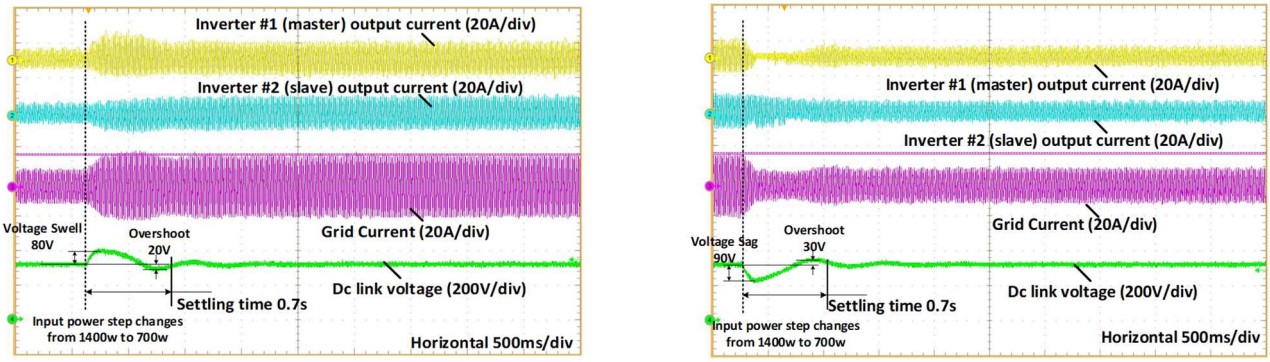
(a) (b)

Fig. 17 Experimental waveforms of steady state performance at 1400W total output power, (a) showing dc link voltage, (b) showing communication signals.



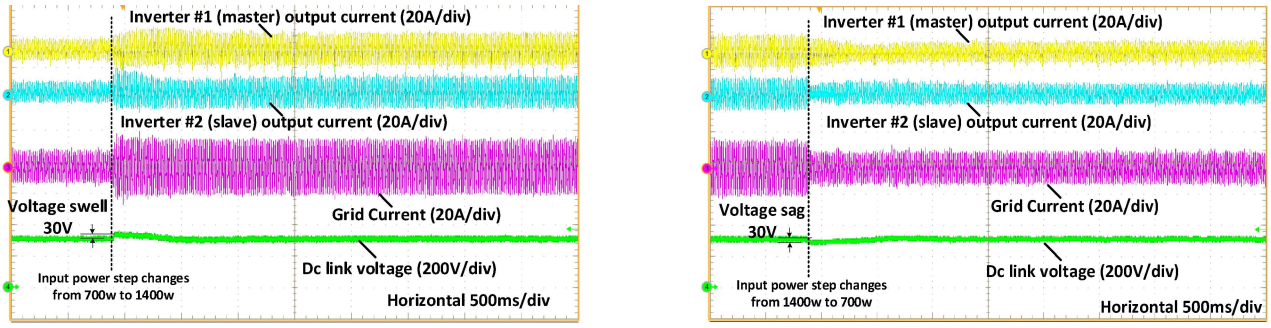
(a) (b)

Fig. 18 Experimental waveforms of transient with LPF in slave module, and t_{lpf} = 0.5 s, α = 1, input power step changes (a) from 700W to 1400W, (bfrom 1400W to 700W.



(a) (b)

Fig. 19 Experimental waveforms of transient with LPF in slave module, and t_{lpf} = 0.5 s, α = 3, input power step changes (a) from 700W to 1400W, (b) from 1400W to 700W.



(a) (b)

Fig. 20 Experimental waveforms of transient with LPF and FFL in slave module, and t_{lpf} = 0.5 s, α = 3, K_{fw}=0.0005, input power step changes (a) from 700W to 1400W, (b) from 1400W to 700W.

shown in the figure. At the same time, the influence of EMI noise on the communication signals can be observed, which is inevitable in power electronic applications. With checking mechanism built in the LBCom modules, the communication is not interrupted. Fig. 18 shows the transient performances of system when t_{lpf} is 0.5 and loop gain α is 1.0. Fig. 18 (a) and (b) shows the experimental results of input power step up and step-down changes respectively. Though the system is stable, the transient performance is poor. The overshoot is large and settling time is long. In Fig. 19, while t_{lpf} is kept at 0.5, loop gain α is increased to 3. It can be seen that the transient performance is improved with increased loop gain. The voltage overshot and settling time both get smaller, but the voltage sag and swell at transient are still large.

In Fig. 20, both LPF and FFL are added in slave module with parameters t_{lpf} = 0.5 s, α = 3, $K_{fw} = 5e^{-4}$. It can be seen that the transient performance is improved significantly with FFL involved. The voltage sag or swell at transient is reduced to less than 30V (10%). And the output power variation of master module is reduced.

The experiment results verified the validity of master-slave control for parallel-operated inverters using LBCom with proposed design method. It also shows good agreement to the study of parameter selection, that with a proper current reference LPF and FFL in slave module, the system shows good tolerability to LBCom effect while keeping a good transient performance.

VI. Conclusion

The paper proposed a robust master-slave control scheme for parallel-operated interfacing inverters, which is tolerable to Low-Bandwidth Communication (LBCom) effects. The effect of communication delay and zero-order-hold (ZOH) on the system is studied. New approaches that design current reference low-pass-filter (LPF) and add voltage feed-forward loop (FFL) to slave modules are proposed, which can compensate the impact of LBCom to achieve a stable and robust operation while keeping a good transient performance.

Experiment results show good agreements to the analytical study. Conclusions are as following,

1) low-bandwidth low-rate communication tools can be used in master-slave current-sharing control of parallel-operated inverters, with proper controller design.

2) By only adjusting voltage loop controller parameters, system can be stable towards impact of time delay and ZOH, but at a sacrifice of loop gain, which may lead to a bad transient performance. And the margin of tolerable delay time is narrow.

3) By designing current reference LPF to slave modules. The effect of LBCom can be mitigated while having an improved transient performance. However, the phase margin is not enough, and it may require higher rating for master module.

4) By having both LPF and FFL in slave modules. The parallel-operated inverter system with LBCom can have enough phase and gain margins to guarantee a stable and robust operation. At the same time, FFL gives slave modules faster transient response. Balanced power distribution among the modules can be achieved at both transient and steady state.

With the proposed method to increase system's tolerability to communication impact, modern communication tools, like PLC, Bluetooth and Zigbee, which are low-cost and flexible but limited by low-bandwidth, can be applied to master-salve control of parallel interfacing inverter system while keeping good steady state and transient performances, which is conducive to make the inverter cost-effective, intelligent and modular. The method can also be expanded to other parallel converter systems.

References

[1] D. Li, and C. Ho, "Master-Slave Control of Parallel-Operated Interfacing Inverters Based on Digital Wireless Communication", in *Proc. IEEE ECCE18*, Sept. 2018.

[2] C. Ho , V. Cheung and H. Chung, "Constant-frequency hysteresis current control of grid-connected VSI without bandwidth control", *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2484 – 2495, Nov. 2009.

[3] S. B. Kjaer, J. K. Pedersen and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292-1306, Sept.-Oct. 2005.

[4] U. S. Selamogullari, D. A. Torrey and S. Salon, "A Systems Approach for a Stand-Alone Residential Fuel Cell Power Inverter Design," *IEEE Trans. Energy Conver.*, vol. 25, no. 3, pp. 741-749, Sept. 2010.

[5] L. Zhang *et al.*, "Parallel Operation of Modular Single-Phase Transformerless Grid-Tied PV Inverters With Common DC Bus and AC Bus," *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 3, no. 4, pp. 858-869, Dec. 2015.

[6] J. H. Teng, S. H. Liao, W. H. Huang and C. C. Chiang, "Smart Control Strategy for Conversion Efficiency Enhancement of Parallel Inverters at Light Loads," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7586-7596, Dec. 2016.

[7] X. Yu, A. M. Khambadkone, H. Wang and S. T. S. Terence, "Control of Parallel-Connected Power Converters for Low-Voltage Microgrid—Part I: A Hybrid Control Architecture," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 2962-2970, Dec. 2010.

[8] K. Sun, X. Wang, Y. W. Li, F. Nejabatkhah, Y. Mei and X. Lu, "Parallel Operation of Bidirectional Interfacing Converters in a Hybrid AC/DC Microgrid Under Unbalanced Grid Voltage Conditions," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1872-1884, March 2017.

[9] "*ABB central inverters PVS800-57B – 1645 to 1732 kW*, " ABB PVS800 datasheet, Mar, 2018.

[10] "*Parallel UPS configurations*, " EATON white paper, Jan, 2009.

[11] H. Han, X. Hou, J. Yang, J. Wu, M. Su and J. M. Guerrero, "Review of Power Sharing Control Strategies for Islanding Operation of AC Microgrids," *IEEE Trans. Smart Grid*, vol. 7, no. 1, pp. 200-215, Jan. 2016.

[12] H. Chiang, K. Jen and G. You, "Improved droop control method with precise current sharing and voltage regulation," *IET Power Electronics*, vol. 9, no. 4, pp. 789-800, 30 3 2016.

[13] S. Xu, J. Wang and J. Xu, "A Current Decoupling Parallel Control Strategy of Single-Phase Inverter With Voltage and Current Dual Closed-Loop Feedback," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1306-1313, April 2013.

[14] H. Wang, M. Han, R. Han, J. M. Guerrero and J. C. Vasquez, "A Decentralized Current-Sharing Controller Endows Fast Transient Response to Parallel DC–DC Converters," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4362-4372, May 2018.

[15] S. Moayedi and A. Davoudi, "Distributed cooperative load sharing in parallel DC-DC converters," in *Proc. IEEE APEC2014*, 2014, pp. 2907-2912.

[16] X. Sun, L.-K. Wong, Y.-S. Lee and D. Xu, "Design and analysis of an optimal controller for parallel multi-inverter systems," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 53, no. 1, pp. 56-61, Jan. 2006.

[17] Z. Zhang, Z. Zhang, S. Xie and C. Yang, "A control strategy for paralleled bi-directional DC-DC converters used in energy storage systems," in *Proc. IEEE ECCE2016*, 2016, pp. 1-6.

[18] M. Le Bolloch, M. Cousineai, T. Meynard, "New masterless modular current-sharing technique for dc/dc parallel converters", *Proc. Power Electronics and Motion Control Conf.*, pp. 73-80, September 2010.

[19] M.M. Jovanovic, D.E. Crow, F.Y. Lieu, "A novel low-cost implementation of 'democratic' load-current sharing of paralleled converter modules", *IEEE Trans. Power Electron.*, vol. 11, no. 4, pp. 604-611, 1996.

[20] M. A. Setiawan, F. Shahnia, S. Rajakaruna and A. Ghosh, "ZigBee-Based Communication System for Data Transfer Within Future Microgrids," *IEEE Trans. Smart Grid*, vol. 6, no. 5, pp. 2343-2355, Sept. 2015.

[21] H. Choi and J. Jung, "Enhanced Power Line Communication Strategy for DC Microgrids Using Switching Frequency Modulation of Power Converters," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4140-4144, June 2017.

[22] A. Werth et al., "Peer-to-Peer Control System for DC Microgrids," *IEEE Trans. Smart Grid*, vol. 9, no. 4, pp. 3667-3675, July 2018.

[23] S. K. Mazumder, M. Tahir and K. Acharya, "Master–Slave Current-Sharing Control of a Parallel DC–DC Converter System Over an RF Communication Interface," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 59-66, Jan. 2008.

[24] E. A. A. Coelho *et al*., "Small-Signal Analysis of the Microgrid Secondary Control Considering a Communication Time Delay," *IEEE Trans. Ind. Electron.*, vol. 63, no. 10, pp. 6257-6269, Oct. 2016.

[25] A. Alfergani and A. Khalil, "Modeling and control of master-slave microgrid with communication delay," in *Proc. IREC*, 2017, pp. 1-6.

[26] X. Lu, J. M. Guerrero, K. Sun and J. C. Vasquez, "An Improved Droop Control Method for DC Microgrids Based on Low Bandwidth Communication With DC Bus Voltage Restoration and Enhanced Current Sharing Accuracy," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1800-1812, April 2014.

[27] J. Lai, H. Zhou, X. Lu, X. Yu and W. Hu, "Droop-Based Distributed Cooperative Control for Microgrids With Time-Varying Delays," *IEEE Trans. Smart Grid*, vol. 7, no. 4, pp. 1775-1789, July 2016.

[28] M. A. Setiawan, A. Abu-Siada and F. Shahnia, "A New Technique for Simultaneous Load Current Sharing and Voltage Regulation in DC Microgrids," *IEEE Trans. Ind. Informat.*, vol. 14, no. 4, pp. 1403-1414, April 2018.

[29] B. Yang, W. Li, Y. Zhao and X. He, "Design and Analysis of a Grid-Connected Photovoltaic Power System, " *IEEE Trans. Power Electron*, vol. 25, no. 4, pp. 992-1000, April 2010.

[30] F. Xiao, L. Dong and X. Liao, "A single-phase grid-connected PV inverter with improved grid-connected current," *2015 CCDC*, Qingdao, 2015, pp. 4083-4088.

[31] K. Ogata, Modern Control Engineering. 2010, p. 462.

[32] D. Li, C. Ho and K. K. M. Siu, "A Method for Solving Current Unbalance Problem of Paralleled Single-Phase Grid-connected Unipolar-PWM Inverters with Common DC Bus," in *IEEE Trans. Ind. Appl.,* early access.