

Stability Analysis of Power Hardware in the Loop (PHIL) Architecture with Solar Inverter

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Abstract— Power Hardware in the Loop (PHIL) simulations have been rapidly growing in recent times due to the flexibility it offers in conducting various system-level studies as well as individual device evaluation. Evaluating a power converter have been one of the major applications of PHIL at recent times in the industry. Following this trend, this paper proposes a way to evaluate a PV micro inverter in PHIL arrangement. The mathematical background to quantify the stability criteria for a PHIL network is presented along with theoretical and experimental verifications. The methodology in this work is based on the model of interface devices and accurate delay model to analyze the stability of a PHIL system employing Routh-Hurwitz's formulation. An extensive analysis on stability along with compensator design to enhance the stability limit of a PHIL system is presented. The work flow developed is applied to evaluate a 250 W PV micro inverter which showed a stable performance with more than 97% efficiency during steady state and transients.

Index Terms— Nyquist Plot, Padé Approx., PHIL, PV Inverter, Real Time Simulations, Routh-Hurwitz Criteria

I. INTRODUCTION

The technology of Power Hardware in the Loop (PHIL) is gaining interest in recent years in industries as well as in academic research settings. The PHIL arrangement offers a variety of advantages in terms of flexibility, space requirement and time. This semi-physical simulation setup can emulate an actual-like environment to evaluate real power apparatuses. This type of testing platform provides a great degree of freedom while evaluating renewable-sourced Power Electronic (PE) converters. One of the applications is, testing a Photovoltaic (PV) inverter connected to the grid under changing environmental conditions and performing various other grid interaction studies [1], [2]. This is just one application and PHIL platforms have been widely adopted to evaluate systems with real energy sources and energy storage elements to study the interactions between them [3].

PHIL may be described as a system consisting of a real-time software model, in a real time simulator like RTDS, interacting with a physical system through an interface device for exchange of power between them. The interface basically

consists of amplifier, Analog Input (AI) card, Analog Output (AO) card and sensor. This interface, therefore, naturally consists of an unavoidable delay from the fiber cables, I/O cards, sensors, conditioning circuits, filters and amplifiers. From the standpoint of system performance, the interface plays a significant role in a stable and accurate PHIL operation. Moreover, the stability problems of PHIL have been intriguing to many researchers and the challenge remains to completely demystify the stability issues.

The stability problem of PHIL simulations is discussed extensively in literatures [4] and [5]. There have been many other studies that focus on accuracy and stability improvement of Hardware in the Loop (HIL) simulations [6]-[8]. However, PHIL being an emerging technology, research focused on generalizing the stability theory has been minimal and more investigation in this area is needed before the techniques with HIL can directly be employed. Similarly, the methods proposed by [4]-[6] for stability analysis and accuracy improvements in PHIL are mostly case specific and provide the basis for analysis for a particular interfacing method. Another important factor in PHIL implementation is choosing the proper Interface Algorithms (IA), as implementation with different IAs poses a unique challenge of stability and accuracy. The performance evaluation of various IAs is analyzed and well documented in [4], [7], [9]-[14]. Among these studies made for stability analysis, it is common to define the stability criteria in terms of the impedance ratio of the simulation and hardware [4]-[5], [12]-[13]. Therefore, an estimate of output impedance is required to carry out these stability studies. As the measurement of actual impedance of the system under study is not always accurately obtained, this will have a significant impact on stability studies. Additionally, it is essential that other parameters that impact the PHIL be analyzed in detail to understand the stability issues. As illustrated in [7], the open loop transfer function of the PHIL can be one of the ways to analyze the system to understand the measure of the stability and parametric effects on stability.

This paper extends the existing studies in PHIL and develops a mathematical framework for quantifying the stability criteria. Further, a comprehensive analysis of the stability problem including verification of theory and mathematical analysis through experiments have been presented in extensive lengths. In addition, this work proposes a methodical approach to work with stable PHIL. The mathematical equations are developed considering a standard resistor divider network in PHIL arrangement and further extended to incorporate a grid connected PE inverter. The

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challenges with PHIL implementation along with methods to stabilize the loop have been discussed in great details in this work. The current filtering technique has been made to its full utilization with the design of compensation block that eliminates any delays and inaccuracies associated with the filter. With the design of proper filter and compensation blocks, a stable working PHIL is demonstrated experimentally for a resistor divider network as well as for a grid connected PV inverter.

II. SYSTEM MODELLING AND ANALYSIS

A. Power Hardware in the Loop (PHIL) Architecture

A general test setup of a PHIL arrangement with an Ideal Transformer Interface Algorithm (ITA) for a resistor divider circuit is shown in Fig. 1. ITA is a well-established method to perform PHIL studies due its simplicity in implementation [7], [14]. This has been clearly demonstrated in [4], [5], [7].

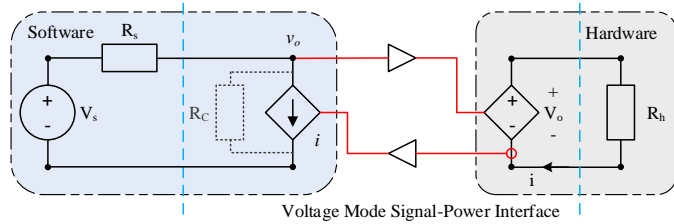


Fig. 1. Ideal Transformer Interface Algorithm.

The ITA setup for a resistor divider consists of an impedance sourced through a voltage-source inside a simulation environment (SE) followed by an interface that connects it to the Device Under Test (DUT). The interface includes a Digital to Analog Converter (DAC) card, a linear amplifier, current sensor and Analog to Digital Converter (ADC) card. The voltage from SE is fed out by DAC card in signal level which is then amplified to corresponding power level voltage. The current from the hardware is sensed and fed-back into SE through ADC card.

An additional resistor R_C has been integrated with the controlled current source and the interface is modified accordingly, Fig. 1. This resistor is needed for the entirety of the interface modelling as the actual PHIL system includes this parallel resistor, and it is vital that is incorporated in the system model to understand its effect on system performance. This paper considers this current source resistor and accordingly presents the mathematical basis for analysis. The implementation diagram for a modified ITA used in this paper is shown in Fig. 1. There are other interface algorithms like Partial Circuit Duplication (PCD) and Damping Impedance Method (DIM) having higher stability margins for PHIL applications [9]. However, these algorithms are relatively complicated to implement. Literatures like [4], [7]-[14] have clearly demonstrated the flexibility of ITA, and therefore ITA is chosen in this work for forming the analysis and experiments.

B. Interface Modelling

Each interface devices for PHIL in ITA can be modelled with their respective transfer function and delays [1], [4]-[17].

Since the interface bridges the SE with the real system, delay within the digital computation and time for ADC and DAC is of utmost importance in determining system performance. Additionally, the amplifier and sensor response cannot be overlooked if the overall system stability is to be studied. Taking these considerations, the system in Fig. 1 can be represented in terms of control block consisting of transfer functions of each component. Fig. 2 shows the control block equivalent of system in Fig. 1 with important components and nodes labelled.

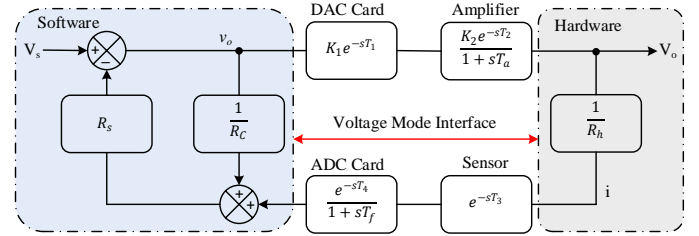


Fig. 2. Control Block Diagram representing the Interface.

The open loop transfer function of the system with resistor divider can be derived using the control block in Fig. 2 and is given by (1).

$$G_{OL}(s) = \frac{V_o(s)}{V_s(s)} = \frac{R_s}{R_C} + G(s) \cdot H(s) \cdot \frac{R_s}{R_h} \quad (1)$$

Where, R_s , R_C and R_h are the software, current source and hardware resistances respectively and, $G(s)$ and $H(s)$ are the transfer functions of forward path and feedback path respectively. $G(s)$ contains the transfer function for AO card and amplifier. Similarly, $H(s)$ contains the transfer function for AI card and sensor delay. Expression for $G(s)$ and $H(s)$ is given by (2) and (3) respectively.

$$G(s) = K_1 \cdot K_2 \cdot \frac{e^{-s(T_1+T_2)}}{1+sT_a} \quad (2)$$

$$H(s) = \frac{e^{-s(T_3+T_4)}}{1+sT_f} \quad (3)$$

Where, K_1 is the software gain, K_2 is the amplifier gain, T_1 and T_4 are the time-step delay, T_2 is amplifier response time, T_3 is the sensor delay, T_a is the cut-off of amplifier and T_f the anti-aliasing filter cut-off of AI card.

The open loop transfer function of the system can be used to analyze the effect of current source resistance on the accuracy. It is also important to note that, delay exponentials in (2) and (3) are not always easy to deal using a standard bode-based frequency response approach. To overcome this problem, the subsequent section presents the approximation of delay using polynomial along with its accuracy quantified.

C. Approximate Delay Model

There are different graphical and mathematical tools to analyze delays. However, the challenge remains for representing the system with delays using transfer function by suitable rational function. Considering this, Taylor series and Padé approximation (PA) are widely accepted as the mathematical tool to approximate pure delays by their respective numerator and denominator polynomials. This allows the use of classical control techniques to analyze the

system. The approximation is moreover governed by the accuracy of the model.

A comparison between Taylor and PA model for delays have been presented in [18]. Taylor approximations for delays have several disadvantages in terms of physical realizability, unstable zeros and unstable for higher order polynomials [18]. Conversely PA offers a considerable flexibility in terms of the degree of polynomials in numerator and denominator and are accurate if the order of numerator is less than that of denominator [18]. Further, an improved accuracy for Padé approximation is proposed in [19] when the order of numerator is one less than the denominator. To validate this, a comparison is made in this paper based on the measure of Integral Square Error (ISE) of PA for equal numerator and denominator order, and PA with one less order in numerator than denominator. A comparison of step responses of Third-Order-Denominator-Third-Order-Numerator (TDTN) PA and Third-Order-Denominator-Second-Order-Numerator (TDSN) PA with its pure delay counterpart is shown in Fig. 3(a). Similarly, Fig. 3(b) presents the step response comparison of second order system with pure delay with TDTN PA and TDSN PA. In Fig. 3, a TDTN, TDSN and a pure delay system is denoted as *Padé₃₃*, *Padé₂₃* and *Pure* respectively. In both the cases ISE for TDSN is lower than TDTN. This is due to the fact that TDTN system experiences a negative jump at the start, otherwise is fairly accurate.

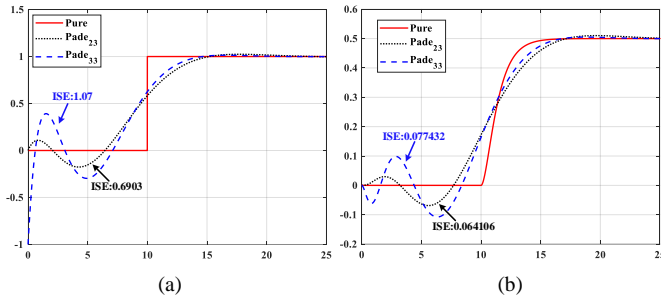


Fig. 3. Step Response of Padé Approx for (a) Pure delay & (b) Second order with Pure delay.

Based on the observation from Fig. 3, delays can be modelled with PA having one less order in numerator than denominator. For the case of this paper, a TDSN PA represented by (4) is considered for the analysis, as there is relatively low improvement in the accuracy by going higher orders.

$$PA_{23}(e^{-sT_d}) \approx \frac{60 - 24 \cdot sT_d + 3 \cdot (sT_d)^2}{60 + 36 \cdot sT_d + 9 \cdot (sT_d)^2 + (sT_d)^3} \quad (4)$$

After approximating the exponential delay function by polynomials, the accuracy of interface with respect to current source resistance can be estimated using (1), (2), (3) and (4) for the system parameters presented in Table I. The parameter T_d represents the lumped delay of the overall loop in Fig. 2.

TABLE I
INTERFACE PARAMETERS

| K_1 | K_2 | T_d | T_a | T_f |
|-------|-------|-------------|-------------|---------------|
| 1/20 | 20 | 100 μ s | 0.4 μ s | 15.75 μ s |

For the purpose of accuracy evaluation, frequency response of (1) when $R_C \rightarrow \infty$ is compared with finite values of R_C .

This is done to achieve an ideal like characteristic as setting value of R_C much higher than R_S would result in the term R_S/R_C to be negligible and (1) would yield to an ideal current source model. Additionally, this approach allows to choose the value of R_C based on R_S . To be able to compute the accuracy of this approach, ISE is used to quantify and judge the accuracy limit for varying values of R_S dependent R_C .

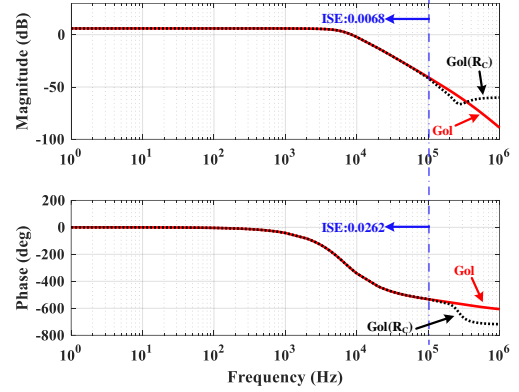


Fig. 4. Accuracy Evaluation of Interface with Current Source Resistor.

The frequency response presented in Fig. 4 compares a plot of $G_{ol}(R_C)$ when $R_C = 1000 \cdot R_S$ with $R_C \rightarrow \infty$. The ISE of the frequency response of the plot for finite R_C is recorded to check the accuracy until a frequency range of 100 kHz. For the purpose of this study, it is a reasonable frequency range to estimate the accuracy considering the fact that cut-off frequency of anti-aliasing filter in AI card is limited to 84.2 kHz. The effect of current source resistor can basically be neglected for the choice of current source resistor, $R_C = 1000 \cdot R_S$, for the frequency range of interest. To further show the variation in accuracy with changing R_C , ISE for various values of R_C is recorded and presented in Table II. One important conclusion that can be drawn from Table II is, the value of R_C lower than 100 times R_S results in a very high error and therefore should be avoided while choosing values higher than 1000 times is merely the accuracy requirement of the user.

TABLE II
ISE COMPARISONS FOR VARIOUS VALUES OF R_C

| Value of R_C | Accuracy Index | |
|------------------------|-----------------|-------------|
| | ISE (Magnitude) | ISE (Phase) |
| $R_C = R_S$ | 31.872 | 715.3529 |
| $R_C = 10 \cdot R_S$ | 4.1016 | 572.098 |
| $R_C = 100 \cdot R_S$ | 1.7087 | 34.8617 |
| $R_C = 1000 \cdot R_S$ | 0.0068 | 0.0262 |
| $R_C = 1000 \cdot R_S$ | 6.3599e-5 | 2.3862e-4 |

III. DEVELOPMENT OF STABILITY EQUATIONS

Rightly choosing the interface method for PHIL does not entirely guarantee the stability of the system. The interface consists of an unavoidable delay from the fiber cables, I/O cards, sensors, conditioning circuits, filters and the amplifiers. In detail investigation of this interface delay along with other parameters in the interface is therefore required if the stability of the system is to be understood. To study the stability of PHIL with resistor divider network, interface device models described in Section II-B and Section II-C serves a basis for further mathematical formulation. Considering the selection of

current source resistor so as to have a minimal effect in accuracy within the frequency range of interest, (1) can be represented as;

$$G_{OL}(s) = G(s) \cdot H(s) \cdot \frac{R_s}{R_h} \quad (5)$$

Once the open loop transfer function of the system in Fig. 2 is known, stability can be easily studied by treating it as a standard control block. Equation (6) describing the characteristics equation can therefore be used to quantify the stability.

$$1 + G_{OL}(s) = 0 \quad (6)$$

$$(1 + sT_a) \cdot (1 + sT_f) + K_1 \cdot K_2 \cdot e^{-sT_d} \cdot \frac{R_s}{R_h} = 0 \quad (7)$$

Substituting (4) in (7) and considering parameters described in Table I, K_1 and K_2 would cancel out each other and the overall equation would resolve to a 5th order polynomial of the form (8).

$$\mathcal{F}(s) = a \cdot s^5 + b \cdot s^4 + c \cdot s^3 + d \cdot s^2 + e \cdot s + f = 0 \quad (8)$$

Where,

$$a = T_a \cdot T_d^3 \cdot T_f$$

$$b = (T_a + T_f) \cdot T_d^3 + 9 \cdot T_a \cdot T_f \cdot T_d^2$$

$$c = (9 \cdot T_a + 9 \cdot T_f + T_d) \cdot T_d^2 + 36 \cdot T_a \cdot T_d \cdot T_f$$

$$d = 36 \cdot (T_a + T_f) \cdot T_d + 3 \cdot \left(3 + \frac{R_s}{R_h}\right) \cdot T_d^2 + 60 \cdot T_a \cdot T_f$$

$$e = 60 \cdot (T_a + T_f) + 12 \cdot \left(3 - 2 \cdot \frac{R_s}{R_h}\right) \cdot T_d$$

$$f = 60 \cdot \left(1 + \frac{R_s}{h}\right)$$

With the polynomial characteristic's equation, the stability analysis can be made using Routh-Hurwitz (R-H) criteria. This enables to quantify the stability issue in terms of interface devices, time delay and system under test. The R-H criteria suggests the system to be stable if there are no sign changes in the R-H table. Each sign change in R-H table corresponds to a right half plane pole signifying an unstable system.

A. Necessary but Not Sufficient Condition

From the characteristic equation described by (8), it is evident that system would be unstable if following two conditions are met;

- If there is any missing term in the characteristics equation
 - o Equation (8) shows all the coefficients finite, hence not unstable
- If there is any sign change in the coefficients
 - o All the coefficients are positive except for e , which might end up being negative with changing ratio of R_s/R_h . This needs to be ensured positive before investigating stability.

Therefore, necessary condition for stability is governed by the positive value of coefficient e which yields.

$$\frac{R_s}{R_h} < \frac{60 \cdot (T_a + T_f) + 36 \cdot T_d}{24 \cdot T_d} \quad (9)$$

Equation (9) describes the necessary condition for stability in terms of amplifier bandwidth and interface delays but most importantly the boundary of instability for a chosen software-hardware resistor. To have the quantitative measure of stability, R-H criteria serves the sufficient condition.

B. Formulation of Stability Criteria

If, in characteristics equation, there are no missing terms and all the coefficient have the same sign does not guarantee the stable system. For stability, R-H table is constructed, and any sign change in the first column is looked for. The first column of R-H table for (8) is tabulated in Table III. With the criteria from Table III, the stability of the system under test can be ensured beforehand.

| For $a > 0$ | $X =$ $bc - ad > 0$ | $Y =$ $be - af > 0$ | $Z =$ $(dX - bY)Y - X^2f > 0$ | f |
|----------------|------------------------|------------------------|----------------------------------|-----|
|----------------|------------------------|------------------------|----------------------------------|-----|

$$\left. \begin{aligned} b &= T_f \cdot T_d^3 \\ c &= T_d^2 \cdot (9 \cdot T_f + T_d) \\ d &= 36 \cdot T_f \cdot T_d + 3 \cdot \left(3 + \frac{R_s}{h}\right) \cdot T_d^2 \\ e &= 60 \cdot T_f + 12 \cdot \left(3 - 2 \cdot \frac{R_s}{R_h}\right) \cdot T_d \end{aligned} \right\} \quad (10)$$

Considering the system in Table I, for a linear amplifier, T_a is much smaller than T_f and T_d , and therefore would have a minimal contribution in coefficient b, c, d and e . With this modification, the updated coefficients of (8) may be rewritten and expressed as in (10).

The stability criteria in Table III can be analyzed with updated coefficients to observe the effect of time delay to determine the stable range of R_s/R_h . But first, (9) can be revisited with above assumptions and can be revised as;

$$\frac{R_s}{R_h} < \frac{5 \cdot T_f + 3 \cdot T_d}{2 \cdot T_d} \quad (11)$$

The criteria stated in Table III along with updated coefficients form the mathematical basis to analyze the stability. By subsequently plugging (10) in criteria of Table III, stability equations can be simplified to analyze the effects of interface parameters in stability. With this, the following inequalities can be tested to find the stability boundary.

Ineq.1: Cond.1: $X > 0$; $X = bc - ad$

$$\text{Cond. 1} \rightarrow \frac{T_d + 9T_f}{3T_d} - \frac{3(T_d + 4T_f)}{T_d} > \frac{R_s}{R_h} \quad (12)$$

Ineq.2: Cond.2: $Y > 0$; $Y = be - af$

$$\text{Cond. 2} \rightarrow \frac{5T_f + 3T_d}{2T_d} > \frac{R_s}{R_h} \quad (13)$$

Ineq.3: Cond.3: $Z > 0$; $Z = (dX - bY)Y - X^2f$

Cond.3 \rightarrow Graphical determination

C. Investigating Stability

The analytical equations governing the stability is a set of three multivariate inequalities given by *Cond.1*, *Cond.2* and *Cond.3*. These multivariate inequalities would yield infinite number of solutions without imposing any constraints in the variables. Hence it becomes computationally cumbersome to determine the solution analytically. Rather a better approach

would be to compare each condition graphically to determine the operating boundary for a specified constraint in variables. The methodology of sequence follows as; first, an operating range of T_d is chosen for a given T_f , and with varying T_a the Left-Hand Side (LHS) of the inequality (12) is determined and compared with the ratio R_s/R_h to confirm the criteria described by *Cond.1*. After identifying the operating region governed by *Cond.1*, LHS of inequality (13) is checked for *Cond.2* in similar manner followed by which inequality in *Cond.3* is also evaluated. To be able to properly understand the effect of each parameters describing stability criteria, each condition is individually represented in a graphical plane showing their operating boundary.

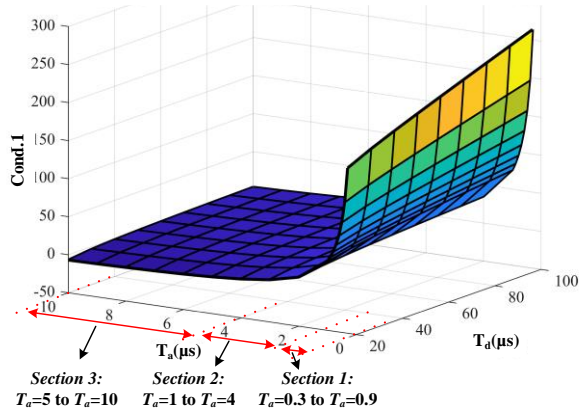


Fig. 5. Graphical representation of *Cond.1* for varying T_d and T_a .

The plot of *Cond.1* is generated for a T_f specified in Table I by varying T_d and T_a . The 3-dimensional variation of LHS of inequality in (12) is shown in Fig. 5. This serves as a graphical tool to choose the ratio R_s/R_h such that it is always less than the value of *Cond.1* (Z -axis) in Fig. 5 so as to satisfy the inequality (12). Basically, the plot in Fig. 5 sets a boundary above which the system would be unstable for a defined range of parameters. This sets a tone for going forward and evaluating remaining two conditions to be able to judge the stable operating region.

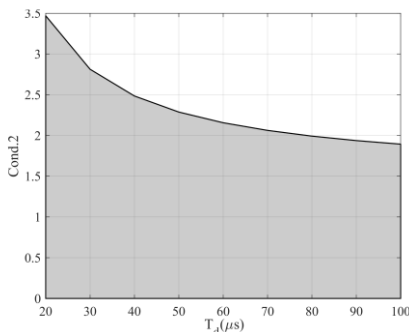


Fig. 6. Area under the plot showing region satisfying *Cond.2*.

The inequality in *Cond.2* can be represented graphically in a manner similar to *Cond.1* for a given T_f . This leads the LHS of inequality in (13) dependent only on the delay time T_d . A plot of the LHS of (13) for varying T_d is shown in Fig. 6 for a T_f specified in Table I. The shaded region in the plot shows the region under which the ratio R_s/R_h must remain in order to

satisfy the stability inequality stated by *Cond.2*. With *Cond.1* and *Cond.2* both satisfied to find the operating boundary of resistances ratio, it is further necessary to proceed with examining *Cond.3* to completely show the stable operating boundary of the system under study.

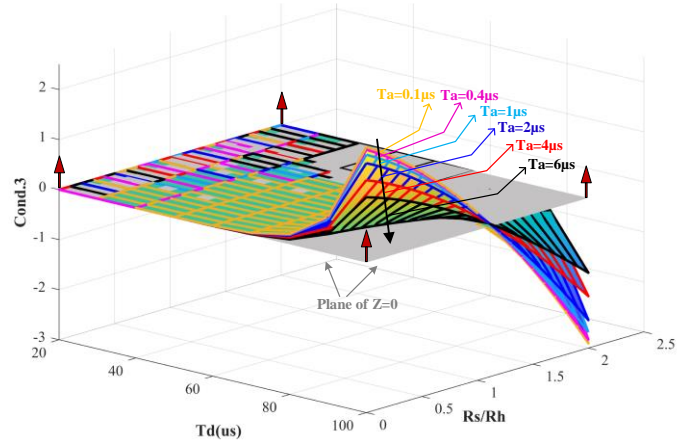


Fig. 7. Plot showing the plane of stable operating region for varying T_d and resistance ratio.

The inequality stated to check *Cond.3*, unlike other two conditions, is a high order polynomial; at least a square of sixth order on initial examination resulting due to the term X^2 . Further simplification to independently collect the ratio R_s/R_h becomes intensive and instead the expression Z can be directly evaluated as it is, for the specified range of parameters and stability check can be made with respect to the positive value of Z . To evaluate the inequality relating *Cond.3*, a series of operating conditions for varying T_d for a given T_a and T_f is chosen. Consequently, for a chosen range of resistance ratio bounded by *Cond.1* and *Cond.2* the variation in Z value is studied. The plot of Z against varying T_d and R_s/R_h ratio is shown in Fig. 7 and the resultant plot is compared with $Z=0$ plane to check for the inequality governing *Cond.3*. Once all three conditions for a given operating point is satisfied, the system under test should ensure stable operation.

IV. VERIFICATION OF STABILITY CRITERIA

There are variety of tools widely employed to design a control system as well as to examine its stability. Among these tools, the graphical methods like Bode and Nyquist plot are preferred to evaluate the controller of a practical system as these methods can be directly applied to experimentally obtained frequency response of a practical hardware. Additionally, for a non-minimum phase system like the system consisting of delays and right half plane zeros, the usual controller design approach with bode using gain and phase margins becomes insufficient as these systems introduce extra phase lag for the same attenuation. However, Nyquist plot overcomes this shortcoming and comes in handy to completely evaluate the performance parameters of a non-minimum phase system as well. Therefore, this paper uses Nyquist plot to make initial verification of the stability criteria derived in Section III. Further, additional experimental results to support this verification is presented considering a resistor divider network as well as a grid connected PV inverter.

A. A Resistor Divider Network

A system of resistor divider network with two combinations of R_s and R_h is chosen to verify the stability test. Nyquist plot is used to test stability graphically for $R_s > R_h$ and $R_s = R_h$, and is shown in Fig. 8. The plot is based on the open loop transfer function in (5) and the rest of parameters are chosen from Table I. The system with $R_s > R_h$ shows an unstable characteristic as compared with $R_s = R_h$ which shows a stable characteristic. With this method it is difficult to quantify the stability margins and therefore we settle for absolute stability for verifications.

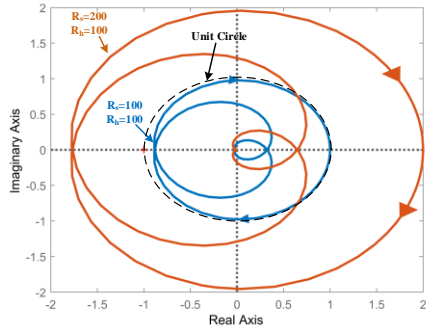


Fig. 8. Nyquist stability test for a system of resistor divider.

To put the stability equations derived in Section III to test, similar parameters to that of Nyquist plot is required. Each condition is checked methodically in the graphs Fig. 5 through Fig. 7. With the parameter from Table I, Cond.1 lies in Section 1 of the plot with corresponding value approximated to 200 (196.6 being the actual value). From (12) it is obvious that the ratio R_s/R_h must be lower than this value to ensure stability. However, Cond.2 overrides Cond.1 by setting $R_s/R_h < 1.894$ (obtained from Fig.6). Moreover, to completely guarantee stability, Cond.3 needs to be satisfied as well. From Fig. 7, for specified parameters, $R_s/R_h < 1.1$ guarantees the stability. Similar observations are seen from Fig. 8 when $R_s/R_h = 1$ and $R_s/R_h = 2$.

B. A Grid Connected PV Inverter

The stability investigation methodology developed in this paper is further used to evaluate the stability of a grid connected PV inverter in PHIL configuration. To be able to directly apply the criteria developed in Section III, the output impedance of a PV inverter needs to be estimated. For this, an impedance analyzer is configured which measures the response in inverter current as the grid voltage changes. With these two measurements of grid voltage and inverter current the output impedance of the inverter can be determined experimentally.

The impedance characteristic of an inverter can be examined to determine the output impedance at the frequency of interest, in this case being the line frequency. The experimental result obtained from the impedance analyzer is presented in Fig. 9 which records the impedance of 124.4 Ω at 60 Hz with a phase of 1.7 deg. Once the output impedance of the PV inverter is known, similar analysis to that for the resistor divider case can be made to predict the stable operating conditions for a micro inverter connected to the grid.

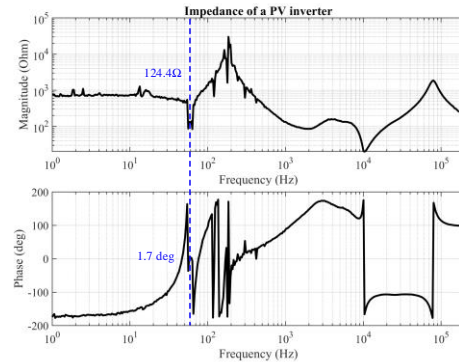


Fig. 9 Experimental determination of output impedance of an inverter.

V. EXPERIMENTAL EVALUATION WITH PHIL

The major challenge while implementing the PHIL, be it a simple network with resistors or with interconnected switching regulators, is to make the loop stable. Therefore, it is important to understand the performance of a PHIL with a network of resistor divider first.

A. PHIL with a Resistor Divider

The PHIL implementation equivalent of a resistor divider network is shown in Fig. 10. Resistances R_s and R_h form the voltage divider with the source voltage V_s in the software environment. The power amplifier is required to reflect the voltage drop across the hardware resistor. The combination of current sensor (current feedback) and voltage amplifier completes the PHIL arrangement with ITA interface.

The implementation of a resistor divider network with PHIL in RTDS requires a digital low pass filter to eliminate the noise associated with analog to digital conversion. However, this comes at an expense of additional lag to the already present time step lag into the fed current signal. At the same time, it is also evident that a low pass filter would increase the stability margin due to the presence of a left half plane pole. Therefore, to take full advantage of the integrated current filter, a compensator can be designed such that any lag associated with the filter can be compensated. Fig. 11 shows the bode plot of a low pass filter with crossover at 1kHz and the required characteristics of the compensator superimposed along with the response of their combinations.

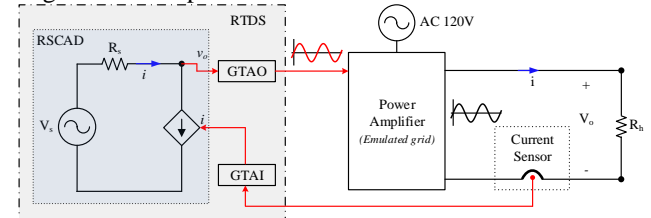


Fig. 10 PHIL Implementation with resistor divider network.

From Fig. 11 the advantage of employing a compensator can be clearly understood. At low frequency the gain of the filter-compensator combination is low such that it helps eliminate any unwanted DC gain in the loop and at the same time it preserves the low pass nature at frequency above 1kHz. Another advantage of such compensator is, it can be designed to improve the phase lag due to low pass filter at a frequency of interest. With this knowledge the compensator and filter transfer functions can be expressed as;

$$G_{LPF} = \frac{1}{1+sT_{lpf}} \quad (14)$$

$$G_{Comp} = \frac{sT_{comp}}{1+sT_{comp}} \quad (15)$$

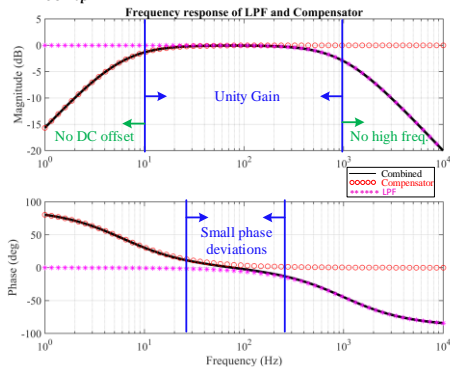


Fig. 11 Compensator design to eliminate the delay due to filter.

Employing the compensator and filter given by (14) and (15) in RTDS to the PHIL implementation for $R_s = R_h = 100\Omega$, a stable operation of resistor divider network is obtained as predicted by the stability criteria. The experimental result for stable operation of resistor divider network is shown in Fig. 12. The result presented in Fig. 12(a) is the measurement made at the physical hardware and Fig. 12(b) shows the respective voltage and current measurements inside the software environment.

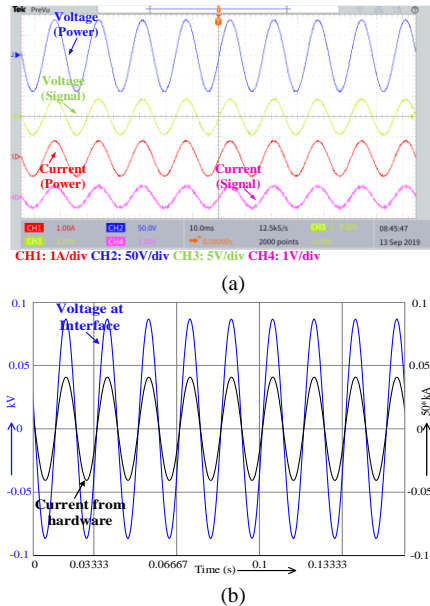


Fig. 12 Resistor divider measurement ($R_s/R_h=1$) at (a) hardware (b) software.

With only the filter present the current in Fig. 12(b) would have a small DC offset as well as a lagging phase with respect to the voltage. To prove the operation of the compensator as described in Fig. 11, an experiment is run and the measurements of voltage at interface as well as currents with and without the compensator are made. From the result presented in Fig. 13, it is clearly seen that the current without the compensator has a phase lag with respect to the voltage while the compensator employed current and voltage are in phase with an insignificant error. This error can be quantified using the reactive power measurements at both hardware and

software end. This is because for a system with resistors, ideally, there should be zero reactive power exchange. Due to the phase shift between voltages and currents as a result of PHIL delays, a reactive power exchange may be seen which can be measured to estimate the errors. For a compensator employed system with $R_s = R_h = 100\Omega$, a Yokogawa power analyzer is used to measure the reactive power physically and also reactive power measurement is made at the software end. The combined hardware and software reactive power measurements directly correspond to the error in PHIL. The measurement showed a total error of 2.243% out of which hardware and software error is recorded at 0.214% and 2.028% respectively. With this, it is valid to say that the errors will be much larger for system without the compensator.

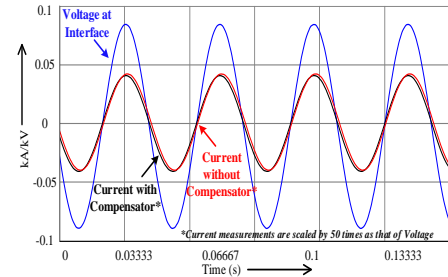


Fig. 13 Comparison showing with and without employing the compensator.

Further to examine the stability margin, the ratio R_s/R_h is increased until the oscillation in the system is seen. This should be enough to give idea about the operation boundary. As analyzed in Section IV-A, the system should show unstable operation when the ratio R_s/R_h increases beyond 1.1. Various experiments were performed by changing the software resistance. The system showed stable operation until $R_s/R_h < 1.48$ which is higher than the theoretical prediction. This is expected due to the fact that theoretical analysis considers the stability margin for a system without additional pole from low pass filter. However, it still gives a fair estimate of the stability operation which can be employed during system specification before performing the PHIL evaluation. The experimental result showing the operation of a resistor divider network when resistances ratio changes from 1.45 to 1.49 is presented in Fig. 14. The oscillation recorded shows the system operating in a margin of instability and hence no further increment in source resistance was made.

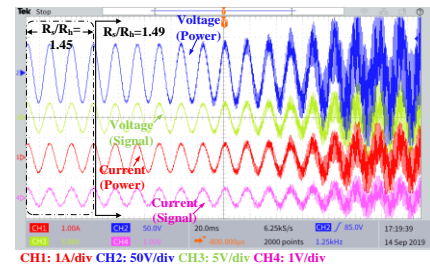


Fig. 14 Measurements for varying R_s/R_h .

B. PHIL with a Grid Connected PV Inverter

Once the system of PHIL with resistor divider is analyzed and implemented, it can be directly extended to evaluate a grid connected PV inverter. The schematic for a grid connected PV

decrease in grid voltage causes the inverter to boost up more current, while remaining within its limit, to maintain the power supplied. It is to be noted that, the system remains stable even during grid transients. Therefore, it can be verified that, the stability analysis in Section III provides enough information to work with a stable PHIL. These observations are crucial in understanding the performance of PV inverter connected to the grid.

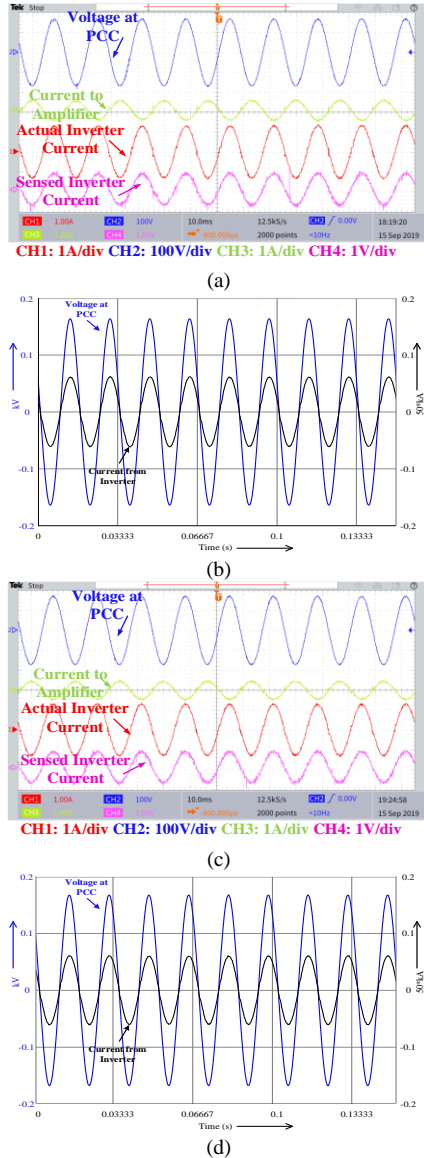


Fig. 17 Steady state results of PV inverter with (a) Strong grid-hardware measurements (b) Strong grid-software measurements (c) Weak grid-hardware measurements and (d) Weak grid-software measurements.

3) Accuracy Estimation

The accuracy of a PHIL system with PV inverter can be estimated in a way similar to that described in Section-V-A. Since the PV inverter under study does not support reactive power exchange, any reactive power seen at the PCC of hardware end and software end corresponds to the error due to PHIL. These measurements are taken at different loading conditions of the power amplifier and are tabulated below in Table V.

TABLE V
ERROR MEASUREMENT

| Amplifier Loading | Error % | | |
|-------------------|----------|----------|-------|
| | Hardware | Software | Total |
| ~No-Load | 2.902 | 0.658 | 3.56 |
| ~Half-Load | 2.621 | 0.394 | 3.015 |

In Table V, the error measurements at hardware does not take into considerations the error in the Phase Locked Loop (PLL). This could be the possible reason for higher error at the hardware end compared to the software. Basically, it can be said that use of compensator aids in stability with a reasonable accuracy margin.

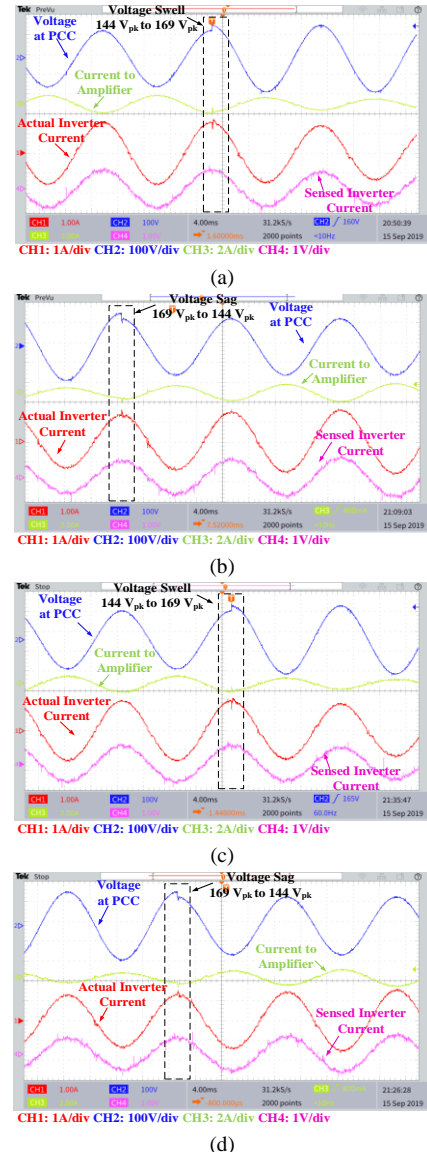


Fig. 18 Transient performance of PV inverter with PHIL under (a) SG-voltage swell (b) SG-voltage sag (c) WG-voltage swell (d) WG-voltage sag.

VI. DISCUSSION ON FUTURE APPLICATIONS

The methodology described in this paper to perform PHIL experiments with PV micro inverter can be easily extended to perform similar type of other PHIL experiments with hardware consisting of renewable sources. The reason being,

the stability criteria developed in this paper is based on impedance and therefore as long as the hardware impedance is known, the analysis methodology can be employed to guarantee a stable PHIL. Considering this, instead of modelling PV by a negative resistance as in [23], [24] and state space averaging to model inverter, this paper directly uses an impedance measured from the network analyzer to perform the stability analysis. The experiments performed are in good standing to validate the proposed method. Further advantages of such approach could be an evaluation of a converter connected to a renewable source with unknown topology and controller with PHIL, in other words, the DUT could be a black box.

VII. CONCLUSION

This paper presented a mathematical framework for considering stability analysis of PHIL. The expression considers all the parameters in the interface to predict the stability and therefore may serve as a tool in determining the proper interface devices beforehand. Besides, the effect of adding a current filter along with compensation design technique to eliminate the effect of filter delays has been extensively analyzed. The quantitative stability analysis has been proposed in this paper considering a resistor divider network. This analysis has been further extended to experimentally evaluate a grid connected PV inverter with PHIL. The PV inverter with PHIL configuration showed a stable and accurate operation at steady state and during various grid transients. The experimental results of PHIL system showed a good agreement with the theoretical predictions.

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