A Fast-Dynamic Control Scheme for a Power-Electronics-Based PV Emulator

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***Abstract*— The dynamic performance of a photovoltaic (PV) emulator is critical for testing applications with fast maximum power point tracking (MPPT) algorithms. In this paper, a power-electronics-based PV emulator (PVE) is proposed to achieve fast-dynamic response as well as to emulate accurately in all regions of the current-voltage (I-V) characteristic curve. The control scheme of proposed PVE consists of an instantaneous output impedance matching (IOIM) controller based on load resistance feedback to generate the voltage reference signal and an inner boundary control (BC) scheme to regulate the converter at a given reference within a short period of time. The IOIM controller overcomes the drawback of conventional PVEs that suffer from oscillating reference signal in a certain region of the I-V characteristic curve. Moreover, use of load resistance feedback in the reference generation algorithm allows to decouple the reference signal generator from the inner control loop. The BC scheme adapts a corrected second-order switching surface to achieve a faster response time and robust operation with switching converter loads. Detailed small signal model of the PVE is derived to design the IOIM control loop and to ensure a stable and fast convergent emulation in the entire I-V characteristic curve. Experimental results of a 130 W (V_{MPP}=35.2V, I_{MPP}=3.69A) prototype are presented with both resistive loads and a MPPT converter to verify its performance under fast varying irradiance and load conditions.**

***Index Terms*— Solar PV emulator, PV simulator, boundary control with corrected second-order switching surface.**

I. Introduction

In recent years, solar photovoltaic (PV) energy has proven to be one of the main renewable energy contributors, mainly due to technological advancements, lower manufacturing cost and its impact against climate change [2]. Integration of solar power into the power grid leads to investigate issues related to solar PV inverters, power quality, harmonic current generation and propagation, islanding of distributed sources and many more [3]. Thus, systems involving the interconnected operation of solar PV arrays need to be analyzed and tested prior to their installation to achieve high energy efficiency and reliable power supply. One way of accomplishing these tests is by installing a prototype system and carrying out field tests.

This work was supported in part by a grant from the Natural Sciences and Engineering Research Council of Canada (NSERC) Discovery Grants program, Canada (Sponsor ID: RGPIN-2016-05952). Part of the work described in this paper has been presented in the ECCE 2017 [1].

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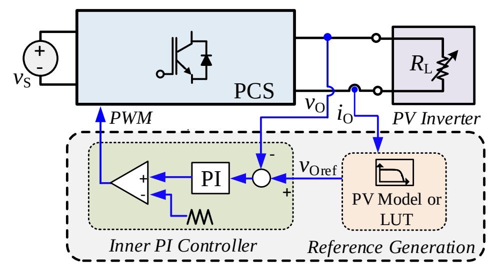


Fig. 1 Typical PVE configuration with direct referencing method.

Field testing using real PV arrays is expensive, bulky and time consuming. Moreover, output current-voltage (I-V) characteristics of a PV cell depends on environmental conditions like, solar irradiation level and atmospheric temperature. Hence, it is not feasible to maintain a controllable testing environment [4]. To overcome these problems, PV emulators are used in test setups and now it has become an essential device among power and energy researchers as a tool to evaluate different contingency test scenarios, especially aviation and space applications.

A PV emulator (PVE) is a controlled power source that mimics I-V characteristics of a real PV array at a given irradiance and temperature. External load characteristics determines the operating point on the I-V characteristic curve. The power source of the PVE, commonly known as the power conversion stage (PCS) is either a linear power amplifier [5],[6] or a switched mode power supply (SMPS) [7]-[11]. The PVE with a linear power stage scheme offers an exceptional dynamic performance which is well-suited for PV source emulators [6]. However, PVE with linear power stage is limited to low power applications. In contrary, SMPSs are preferred over linear power stage schemes for relatively higher power applications in terms of its advantages in low cost, high efficiency and high-power density. Even though SMPSs have been extensively used in the literature for PVEs, their performance are not promising in terms of response time and limited bandwidth compared to linear power stage schemes [4]-[6]. A typical topology of SMPS type PVE is buck converter. Dynamic performance of buck type converters is determined by LC filter values, control loop and the voltage conversion ratio [12]. These parameters should be correctly engineered in SMPS design to mimic similar dynamic characteristics of a real PV module. Dynamic characteristics of a real PV module is mainly governed by the RC filter formed by the load resistance and inherent source capacitance which represents the diffusion effect of PV cells [13]. Nonetheless, real PV modules exhibit fast dynamic response and have proven to reach the steady-state within few microseconds to tens of microseconds after a transient [11]. Hence, PVE demands for fast transient performance as a nonlinear source emulator.

Fig. 1 shows the system configuration of a switched-mode PVE with direct reference method. The controller of the PVE consists of an inner control loop that determines the switching signal of the SMPS and an outer loop that measures the load side current and/or voltage and generate the reference signal for inner loop controller. The outer loop reference generation algorithm affects the accuracy and the response time of the PVE the most and its ability to emulate the entire I-V curve. The most common outer loop algorithm is known as the direct referencing method (DRM) which measures the load side voltage and feed into a PV model to calculate a current reference directly [14]. The same logic has been implemented by measuring load side current and generating voltage reference for the inner loop.

The problem with DRM is that it creates an oscillatory reference signal in one region of operation (i.e. in constant voltage region (CVR) with current-mode control and constant current region (CCR) with voltage-mode control) as feedback signal always has an ac ripple [15]. As shown in Fig. 2, I-V characteristic curve can be divided into two regions namely CCR and CVR. In CCR, small change in current would escalate a large change in voltage. Similarly, in CVR, small change in voltage would escalate a large change in current. Thus, operation of PVE in both CCR and CVR is challenging with DRM. The dual mode control methods [15], [16] are employed to resolve oscillatory reference signal by using two separate direct referencing blocks and accordingly choosing the control mode considering operating regions in I-V curve; CCR or CVR. However, this increases the complexity of the controller and it requires an additional control algorithm to improve performance in the vicinity of maximum power point (MPP) [15]. Alternatively, the impact of oscillatory reference signal can be minimized by designing the inner control loop (*i.e.* proportional-integral (PI) controller) with a lower control bandwidth. This eliminates the effect of high frequency oscillations but at the expense of dynamic performance of the PVE. Therefore, linear controller with lower bandwidth has been generally used over fast-dynamic non-linear control methods. High bandwidth control schemes are employed in [11], [17] to improve the dynamic response. However, its performance on oscillatory operating region has not been investigated thoroughly.

Further, with DRM, reference generation loop is coupled with inner control loop design. In other words, response time of reference signal is limited by the inner loop bandwidth. Since low bandwidth inner controllers are typically used to overcome the oscillatory reference signal, this will further impact the overall system response of PVE. Resistance comparison methods [8], [18] are considered to decouple the outer reference generation loop from the PCS and inner loop stages and to suppress reference oscillatory problem. This method uses the load resistance as the feedback signal to determine the operating point reference. The load information is determined instantaneously by measuring output current and voltage. Any change in load would immediately be reflected to the reference generation block and would not loop through PCS and inner loop. In this way, reference generation block will be decoupled

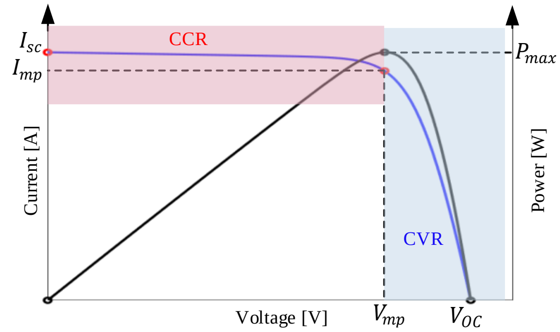


Fig. 2 The I-V and P-V characteristics of PV module.

from the rest of the system. However, in [8], [18] reference signal is converged to an operating point through an iterative method by comparing the measured load resistance and reference load resistance. Problem with this approach is the number of iterations that takes to reach steady-state is high which lead to the slow transient response of PVE. References [19], [20] have taken steps to develop current-resistance PV model to generate the current reference directly based on measured resistance.

This paper seeks to develop a fast-convergent reference generation algorithm (RGA) using load resistance feedback to make it independent from inner control loop design and for achieving a stable reference signal over entire I-V curve. Additionally, this paper is focused on utilizing a wide bandwidth inner control loop to improve dynamic response of the PVE for keeping its usefulness in testing real applications such as MPP tracking (MPPT) converters which have a convergence speed of tens of milliseconds [11]. The proposed PVE includes a synchronous DC-DC buck converter as the power conversion stage with a non-linear boundary control (BC) scheme to regulate its output voltage and instantaneous output impedance matching (IOIM) controller to generate a stable voltage reference. In contrast to DRM, IOIM controller generates a stable voltage reference throughout the I-V curve. Further, it has the advantage over resistance comparison method in terms of convergent speed and its bandwidth is mainly dependent on the integral gain as well as the operating point in I-V curve. Inner voltage-mode (VM) control loop is implemented using a BC with corrected second-order switching surface (σ_{cor}^2) [21] to achieve ultra-fast response and robust operation. Proposed PVE is investigated theoretically and experimentally under steady-state operation and different transient conditions including load step change and irradiance level changes with linear loads as well as with a MPPT micro inverter. The paper presents a detailed small signal model of the PVE to prove that reference generation loop is independent from PCS and inner control loop. A 130 W, 60 V input DC-DC synchronous buck converter prototype was implemented to verify the control scheme.

II. System Description and Control Strategy

The structure of the proposed PVE is shown in Fig. 3. The PCS is formed by a synchronous DC-DC buck converter that operates in VM control. Proposed controller consists of instantaneous output impedance matching (IOIM) controller as the reference generation block and inner control loop to regulate capacitor voltage at given voltage reference (v_{Oref}). Firstly, output current (i_O) and voltage (v_C) are sensed and fed into the IOIM controller to obtain the load information (R_L) instantaneously. In IOIM, current correspond to both PV model and load resistance are matched through integral controller action while generating the v_{Oref}. The conventional V-to-I look up table (LUT) is used to implement the PV model. Boundary control with corrected second-order switching surface (σ_{cor}^2) is employed as the inner controller which determines switching instants for S_1 and S_2 in PCS.

A. Novel IOIM controller for reference generation

The output characteristics of a PV module depend on load condition and its operating point must satisfy both load and I-V characteristics. From a mathematical point of view, the operating point can be identified by solving the non-linear I-V characteristic equation (1) of a single-diode PV model, and the load characteristic equation given by (2).

$$I = I_{ph} - I_{on}\left[exp\left(\frac{V+R_s I}{aV_t}\right) - 1\right] - \left(\frac{V+R_s I}{R_p}\right), \tag{1}$$

$$I = \frac{V}{R_L}, \tag{2}$$

where I_{ph} is photo current generated by the incidence of irradiation on a solar cell, I_{on} is reverse saturation current, a is diode ideality constant, R_s represents structural resistance in a PV cell, R_p represents the leakage effect of a solar cell semiconductor material, $V_t = kT/q$ is thermal voltage of a PV cell in which k is the Boltzmann constant and q is the magnitude of an electron charge [22]. Due to the implicit non-linear characteristics of (1), solving both equations numerically would slow down the reference generation process.

In IOIM, control approach is taken to solve these two equations and extract v_{Oref} for a measured load resistance. As shown in Fig. 4, currents correspond to the load line (i_R) and PV model (i_{Oref}) are compared to determine impedance matching voltage through integral controller. The i_R is obtained by multiplying v_{Oref} and $1/R_L$. PV model is implemented using an V-to-I LUT that used to generate i_{Oref} for a given v_{Oref} feedback signal. The LUT approach is chosen over an approximate explicit I-V equation [23] for its easy implementation and to minimize the computational burden on microcontroller. Fig. 4 shows the trajectory of i_R and i_{Oref} when the load changes from R_{L1} to R_{L2}. The controller moves both i_R and i_{Oref} towards the new operating point until the steady-state error is zero. The IOIM controller guarantees a stable reference signal irrespective of the operating region and bandwidth of the reference generation can be adjusted mainly through the integral gain (k_i).

B. Inner Control Loop Design

A stable voltage reference is determined by IOIM within a short period of time, a fast-dynamic controller is required to regulate v_C at the reference value. In [21], σ_{cor}^2 is presented for buck converters connected to capacitive loads. The load of the PVE is a non-linear switching converter and typically has a large

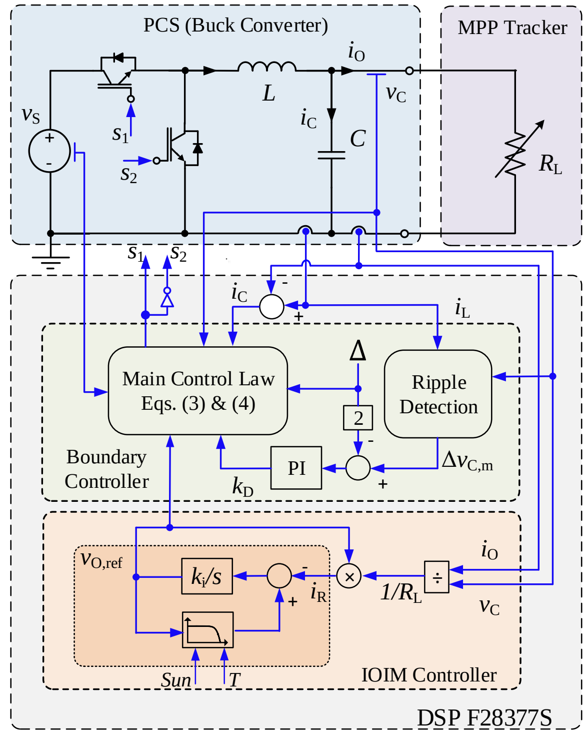


Fig. 3 Architecture of the PVE with the proposed control scheme.

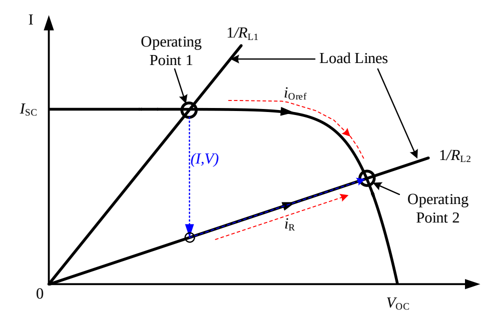


Fig. 4 Trajectory of control parameter under a load step up on I-V plane.

input capacitor (C_L) to filter the high frequency switching components. Hence, σ_{cor}^2 method is chosen as the inner loop controller for achieving faster response time and robust operation with non-linear switching loads. The corrected switching surface accounts for the existence of unknown load capacitor and outer voltage ripple feedback loop is introduced to determine corresponding switching criteria gain factor that adjusts the overall gain while maintaining the output voltage ripple at a specified voltage band (2Δ). In BC, switching surface is defined as a boundary condition in the state-plane that decides the state of the switches of the converter [24], [25]. The switching criteria for buck converter is given as below,

Switch ON Criteria (S_1=1 and S_2=0)

$$v_C \le v_{C,min} + k_1[1 + k_D]i_C^{\,2} \qquad \& \qquad i_C < 0, \tag{3}$$

Switch OFF Criteria (S_1=0 and S_2=1)

$$v_C \ge v_{C,max} - k_2[1 + k_D]i_C^{\,2} \qquad \& \qquad i_C > 0, \tag{4}$$

where $v_{C,min} = v_{Oref} - \Delta$, $v_{C,max} = v_{Oref} + \Delta$, $k_D = C_L/C$,

$k_1 = \frac{L}{2C}\frac{1}{v_S - v_{Oref}}$, $k_2 = \frac{L}{2C}\frac{1}{v_{Oref}}$ and Δ is the voltage band reference. Detailed derivation of (3) and (4) is given in [21]. The σ_{cor}^2 requires instantaneous values of v_S, v_C, i_C, Δ and k_D to determine the switching actions. The value of k_D is determined by an outer feedback loop as shown in Fig. 3. The error amplifier generates the required k_D value based on the voltage ripple error which is calculated by taking the difference between specified peak-to-peak voltage band (2Δ) and peak-to-peak ripple of v_C ($\Delta v_{C,m}$). The detailed design procedure for outer feedback loop is presented in [21]. The ripple magnitude of v_C is measured by using i_L and v_C. The control law derived is valid for converter operating in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) [25]. Hence, PVE can operate in open circuit voltage output. However, PVE wouldn't be able to operate in short circuit current output as this is a voltage output converter. The minimum output voltage will be decided by considering the minimum duty ratio that can be implemented and the peak-to-peak voltage ripple.

C. Power stage design considerations

The filter inductor (L) is designed to allow a maximum peak-to-peak current ripple (Δi_{Lmax}) while maintaining a desired switching frequency range for given specifications of the PVE. The switching frequency (f_S) of the boundary-controlled buck converter is given by,

$$f_S = HK\Delta^{-0.5}(1 + k_D)^{-0.5}, \quad (5)$$

where $H = \frac{v_{ref}(v_S - v_{Oref})}{L v_S}$, $K = \frac{\sqrt{k_1 k_2}}{\sqrt{2dk_1} + \sqrt{2(1-d)k_2}}$ and d is the duty ratio. A detailed derivation of (5) is given in [21], [26]. The f_s is varying and it will be dependent on LC filter values, voltage conversion ratio, Δ and load capacitance. Based on the steady-state characteristics of the buck converter, peak-to-peak current ripple is given by,

$$\Delta i_L = v_S d(1-d)/(L f_S). \quad (6)$$

The variation of both f_s and Δi_L with L can be determined from (5) and (6). The range of C_L and v_C are key specifications in selecting the inductor value that would maintain desired current ripple and f_S range. The upper bound condition for f_S is determined when C_L is minimum and d=0.5 while lower bound of f_S is determined when C_L is maximum and $d(1-d)$ is minimum. The ripple current will be at maximum at the lower boundary condition of f_S and vice versa. Fig. 5 shows the variation of both f_S and Δi_L with L at upper and lower bound conditions for given Δ and C. It provides a guideline to determine the inductor value for a specified ripple current and desired f_S range.

The output capacitance is typically selected by considering the effect of output voltage ripple, inductor current ripple and transient load response capability of the capacitor under an extreme transient from maximum load to no load. This yields,

$$C_{min} = \Delta i_{Lmax}/[8 f_s.(2\Delta)], \quad (7)$$

$$C_{min} = L * I_{L,peak}/(V_{OS}^2 - v_O^2), \quad (8)$$

where $I_{L,peak}$ is the maximum peak current, V_{OS} is the output

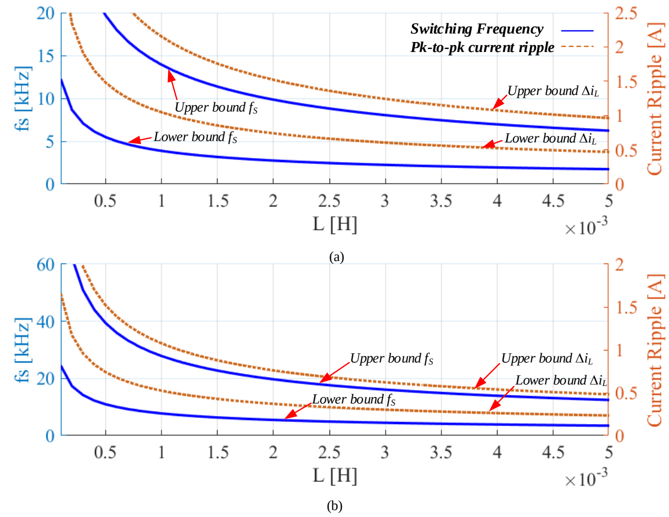


Fig. 5 Variation of f_S and Δi_L with L for upper bound condition for f_S (C_L=0, d= 0.5) and lower bound condition for f_S (C_L=30μF, d= 0.16) (a) Δ =1 V (b) Δ= 0.25 V.

voltage overshoot at maximum load. Both (7) and (8) are taken into consideration for selecting the capacitance.

III. System Modelling and Analysis

The aim of this section is to derive the small signal model of proposed PVE to show that the reference generation block is decoupled from PCS and inner control loop. The analysis is done considering a resistive load at the output. First, the small signal relationships based on load resistance and voltage reference will be developed by considering the load resistance (r_L) as an input variable to the system. The following formulas, in Laplace domain, can be derived by applying Ohms law for the proposed PVE shown in Fig. 3.

$$v_C(s) = r_L(s) i_O(s), \quad (9)$$

$$v_{Oref}(s) = r_L(s) i_R(s). \quad (10)$$

By introducing small signal perturbations in (9)-(10), the relationship among small signal terms of v_C (Δv_C), i_O (Δi_O), r_L (Δr_L) and v_{Oref} (Δv_{Oref}) are derived as,

$$\Delta r_L(s) = \frac{1}{I_O}\Delta v_C(s) - \frac{R_L}{I_O}\Delta i_O(s), \quad (11)$$

$$\Delta i_R(s) = \frac{1}{R_L}\Delta v_{Oref}(s) - \frac{I_R}{R_L}\Delta i_O(s). \quad (12)$$

where R_L, I_O, I_R are the DC terms of r_L, i_O, i_R respectively. To determine the transfer function (TF) between Δi_{Oref} and Δv_{Oref}, the linearized model of PV is required. The linear model of PV is described by the line tangent to the I-V characteristic curve at the linearization point (V_{pv}, I_{pv}) [27], i.e.,

$$\Delta i_{Oref} = (I_{pv} - g_{pv} V_{pv}) + g_{pv}\Delta v_{Oref}, \quad (13)$$

where g_{pv} is the derivative of the I-V curve at the operating point. It is obtained by differentiating (1) at any operating point on the I-V characteristic curve and given by (14).

$$g_{pv}(V_{pv}, I_{pv}) = \frac{\Delta i_{Oref}(s)}{\Delta v_{Oref}(s)} = -\frac{\frac{I_O}{aV_t} exp\left(\frac{V_{pv}+R_S I_{pv}}{aV_t}\right) - \frac{1}{R_{sh}}}{1 + \frac{I_O R_S}{aV_t} exp\left(\frac{V_{pv}+R_S I_{pv}}{aV_t}\right) + \frac{R_S}{R_{sh}}}. \quad (14)$$

The PV module parameters required for (14) are determined by using an iterative method presented in [22]. This allows to extract parameters based on manufacturer's datasheet. The key parameters of PV module (BP365, 65 W) under standard test conditions (STC) is tabulated in Table I. The TF between Δi_R and Δv_{Oref} can be derived by utilizing the PV model in (13) to IOIM control architecture shown in Fig. 3, which yields,

$$\Delta v_{Oref}(s) = G_{IOIM}(s)\Delta i_R(s), \tag{15}$$

where $G_{IOIM}(s) = \frac{-k_i/s}{1-(k_i/s)g_{pv}}$.

TABLE I
PARAMAMETERS OF THE BP365 PV MODULE AT 25 ^{0}C, 1000 W/m^2

Parameter		Value
Maximum power	P_{max}	65 W
Short circuit current	I_{SC}	3.99 A
Open circuit voltage	V_{OC}	22.1 V
Voltage at P_{max},	V_{MPP}	17.6 V
Current at P_{max}	I_{MPP}	3.69 A
Temperature Coefficient of V_{OC}	K_V	-(80±10) mV/ºC
Temperature Coefficient of I_{SC}	K_I	(0.065±0.015)% / ºC
Number of cells in series,	N_S	36
Reverse saturation current of the diode	I_{on}	7.41984e^{-10} A
Equivalent series resistance	R_S	0.444
Equivalent parallel resistance	R_P	*204.02*
Diode ideality constant	a	*1.067635*

The closed-loop (CL) TF of the inner BC loop can be approximated as a first-order low pass filter with a cross-over frequency of switching frequency [28], and it is given by,

$$G_{inner}(s) = \frac{\Delta v_C(s)}{\Delta v_{Oref}(s)} = \frac{1}{1+\tau s}, \tag{16}$$

where $\tau = 1/2\pi f_S$. The control block diagrams of PVE including the reference generation loop and boundary controlled PCS can be derived with small signal relationships that are given by (11),(12),(15),(16) and is shown in Fig. 6 (a). From Fig. 6 (a), the loop gain of IOIM loop is given by,

$$G_{OL_{IOIM}}(s) = \frac{\Delta v_{Oref}(s)}{\Delta r_L(s)} = \frac{-G_{IOIM}(s)}{R_L}. \tag{17}$$

The closed-loop TF of the reference generation loop ($G_{CL\_IOIM}(s)$) is given by,

$$G_{CL_{IOIM}}(s) = -\frac{I_{pv}}{R_L}\frac{G_{IOIM}(s)}{1-\frac{G_{IOIM}(s)}{R_L}}. \tag{18}$$

From (17) and (18), it is evident that reference generation loop is independent from $G_{inner}(s)$. To validate the small signal model of reference generation loop, frequency response of $G_{CL\_IOIM}(s)$ is compared with AC sweep results from PLECS^{TM} simulation. In Fig. 7, closed-loop frequency response of developed mathematical model is compared with AC sweep results from PLECS^{TM} for three different operating points to validate the model in entire regions of I-V curve including; CCR, CVR and MPP. Results in Fig. 7 exhibit a close match, thus, validates the small signal model derived for the reference generation loop. The bandwidth of IOIM control loop should be designed lower than bandwidth of BC loop to filter out switching frequency ripple component from the instantaneous impedance measurement. Hence, maximum bandwidth of the IOIM should be chosen to be lower than the lowest f_S of the PVE. Further, for a given k_i, the bandwidth of IOIM control loop will vary according to the value of g_{pv} which is dependent on the operating point in IV curve. As shown in Fig. 7, the closed-loop bandwidth of IOIM controller will be highest in CVR. Hence, integral gain is designed by taking that PVE operates at a point in CVR. Fig. 8 shows step response of the IOIM control loop for different k_i under above mentioned operating points. Moreover, Table II provides the closed-loop bandwidth of IOIM controller for different k_i values.

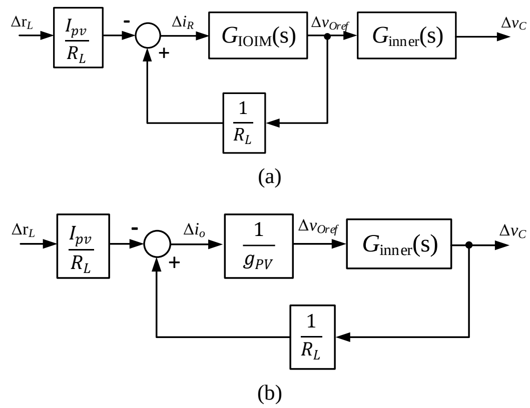


Fig. 6 Control block diagram of PVE (a) the proposed, and (b) with DRM.

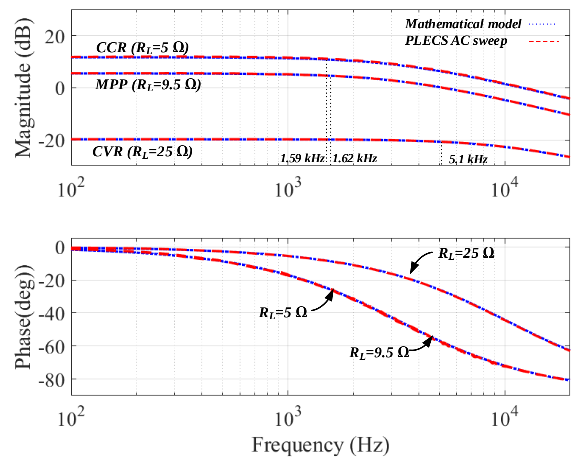


Fig. 7 Closed-loop Bode Plot of IOIM control loop with k_i =50000.

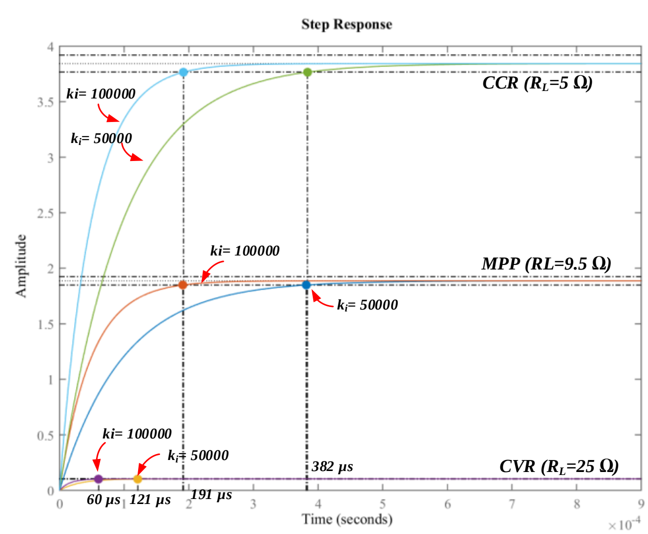


Fig. 8 Step response of IOIM control loop with k_i=50000 and k_i=100000.

To highlight the advantage of IOIM control compared to DRM, the control system block diagram of the DRM-based VM PVE presented in Fig. 1, is derived similarly by considering the r_L as an input variable to the system and shown in Fig. 6 (b). The open-loop TF of the reference generation loop is given by,

$$G_{OL_{DRT}}(s) = \frac{\Delta v_{Oref}(s)}{\Delta r_L(s)} = \frac{-G_{inner}(s)}{g_{pv}R_L}. \quad (19)$$

From (19), it is clearly seen that reference generation loop is coupled with the closed loop transfer function of the inner control loop (G_{inner}).

TABLE II
DYNAMIC CHARACTERISTIC OF IOIM CONTROL LOOP

k_i	Closed-loop Bandwidth		
	@CVR	@MPP	@CCR
10,000	1.03 kHz	0.331kHz	0.326 kHz
20,000	2.07 kHz	0.651 kHz	0.645 kHz
50,000	5.11 kHz	1.62 kHz	1.59 kHz
100,000	10.20 kHz	3.28 kHz	3.23 kHz
	Settling time		
	@CVR	@MPP	@CCR
10,000	606 μs	1.91 ms	1.92 ms
20,000	303 μs	954 μs	959 μs
50,000	121 μs	382 μs	384 μs
100,000	60 μs	191 μs	192 μs

IV. SIMULATION RESULTS

Simulation results of the proposed PVE with a high performance MPPT converter are provided in this section and compared with a conventional PVE (i.e. a buck converter with an inner PI controller plus an I-to-V LUT as the RGA) to exalt the performance of the proposed method. The inverted buck topology is chosen to realize the MPPT converter, which represents a common choice for the front-end dc-dc stage in PV applications. The control scheme consists of a *dp/dv* tracking scheme as the MPPT algorithm and a PI controller to regulate the input voltage of the MPPT converter. The cascaded system configuration is shown in Fig. 9, and parameters used in the simulation are listed in Table III. The control bandwidth of the conventional PVE is designed with 370 Hz to achieve shorter settling time, while avoiding the oscillatory reference issue. Simulation results of a PV array, the proposed PVE and the conventional PVE measured under a step change in irradiance are shown in Fig. 10. Fig. 10 (a) shows the input power, input voltage and input current of the MPPT converter when its inner PI controller bandwidth is set to 4.25 Hz (k_{P2}=0.0065, k_{I2}= 0.5). It is shown that MPPT converter is able to track the MPP accurately with all three PV emulation methods. However, the system with conventional PVE becomes unstable when bandwidth of the inner PI loop of the MPPT converter is increased to 1.96 kHz (k_{P2}=0.039, k_{I2}= 3) as shown in Fig. 10 (b), while, under proposed method, the MPPT converter is still able to track the MPP. In this way, the comparison highlights how the proposed PVE emulator enables to evaluate faster MPPT algorithms compared to the traditional PVE.

TABLE III
PARAMETER VALUES USED IN SIMULATIONS

BUCK STAGE				BOOST STAGE			
Param.	Value	Param	Value	Param	Value	Param.	Value
v_S/Δ	60 V/0.5V	$f_{S_{BC}}$	10 - 28 kHz	v_{DC}	48 V	k_{P2}	0.006
L	1 mH	$f_{S_{PI}}$	20 kHz	L_B	3.5 mH	k_{I2}	0.5
C	4.7 μF	k_{P1}, k_{I1}	5.7x10^{-4} ,38	C_L	15 μF	f_{S2}	20kHz

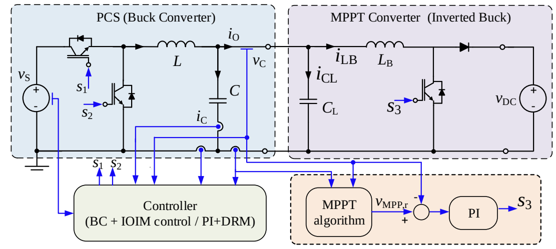
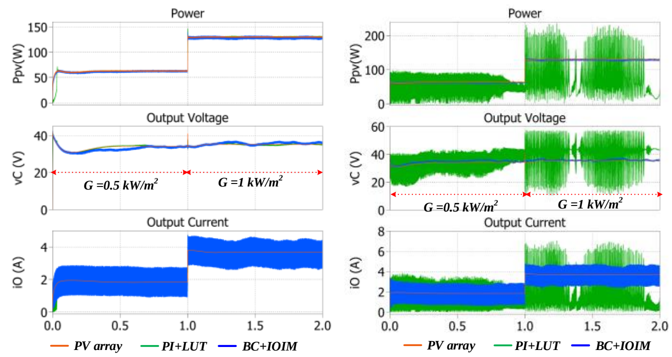


Fig. 9 The system configuration of a PVE cascaded to a VM MPPT converter.



(a) (b)

Fig. 10 Simulation comparison of PV array, proposed PVE and traditional PVE with PI+DRM for a step change in solar irradiance from 0.5 kW/m^2 to 1 kW/m^2 with a VM MPPT converter for (a) a low bandwidth PI loop (4.25 Hz) and (b) a high bandwidth PI loop (1.96 kHz).

TABLE IV
KEY PARAMETERS OF PVE PROTOTYPE

Parameter	Value	Parameter	Value
v_S	60 V	Δ	1 V
L	1 mH	C	4.7 μF
v_C	10 V – 44.2 V	i_O	0 A - 3.99 A
C_L	0 - 50 μF	f_S	3.2 kHz - 14.1 kHz

V. EXPERIMENTAL VALIDATION

A 130 W, 60 V input dc voltage, synchronous DC-DC buck converter prototype has been implemented which is based on the design block diagram in Fig. 3. The design specification of the PVE prototype is given in Table IV which is intended to emulate a PV array with two BP365 modules connected in series. Control scheme is implemented using a Texas Instruments (TI) TMS320F28377S microcontroller. BC scheme is implemented in an interrupt service routine (ISR) running at 300 kHz while outer voltage ripple feedback loop and IOIM controller are implemented in an ISR running at 50 kHz. The measured variables are i_O, i_L, i_C, v_C and v_S and all of them are sampled at 300 kHz. The k_i gain in IOIM controller is chosen as 50,000 to limit the maximum bandwidth of IOIM loop to be lower than 5.11 kHz. Further, IOIM uses a LUT to implement the BP365 PV module where the I-V pairs are stored in a 3-D array with evenly spaced voltage array for solar irradiation levels between 0 to 1 kW/m^2 in steps of 0.1 kW/m^2 and three temperature values of 0 ºC, 25 ºC and 50 ºC. The resolution of the LUT is maintained at 49 mV.

A. Dynamic Performance of Commercial Panel and PVE

The response time of a commercial PV emulator and real PV array is examined to identify their dynamic performance and compare them with the proposed PVE in modern solar power conditioning test setups. Fig. 11 (a) and Fig. 11 (b) present transient response results of a Chroma 62050H-600S solar PVE for a load step change from 25 Ω to 5 Ω, and irradiance step change between 0.5 kW/m^2 and 1 kW/m^2, respectively. In these tests, Chroma PVE is programmed to emulate two BP365 PV modules connected in series with V_{oc} = 44.2 V and I_{sc} = 3.99 A. The output voltage and current of Chroma 62050H-600S take between 15 ms – 24.5 ms to reach ± 5 % of the steady-state output value after transients. It is observed that Chroma PVE has an oscillatory output during its operation in CVR. Transient response of a real PV array is determined with a test setup that has four Siemens PowerMax SP75 PV modules which are connected in series with a resistor bank. Fig. 12 shows transient response of the SP75 array for a load step down from 50 Ω to 25 Ω. The recorded settling time is 10 µs which is expected as it has fast-dynamic characteristics [11]. It is shown that the dynamic response of commercial PVE is far from the real PV modules.

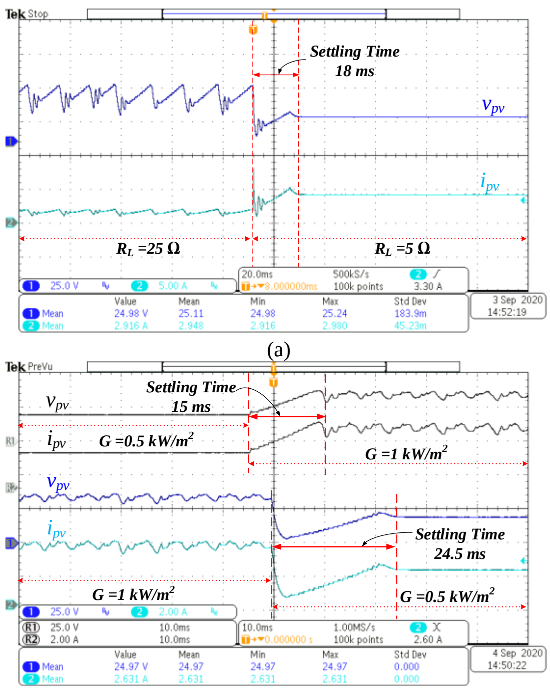


Fig. 11 Transient response of Chroma 62050H-600S PVE for (a) a load change from 25 Ω to 5 Ω at 1 kW/m^2 and for (b) a step change in irradiance between 0.5 kW/m^2 to 1 kW/m^2 at 10 Ω.

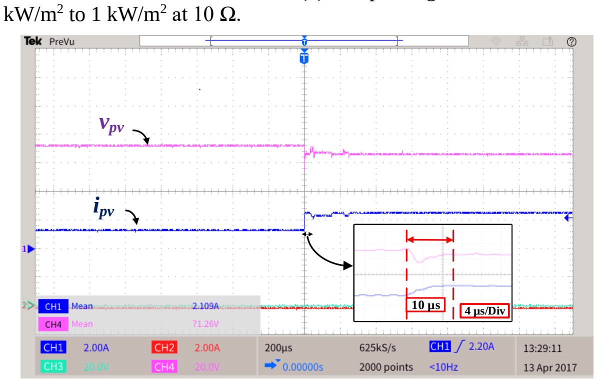


Fig. 12 Transient response of a real SP75 PV array (4x1) for a load change from 50 Ω to 25 Ω.

B. Proposed PVE - Resistive Loads Evaluations

Tests are conducted with resistive loads to evaluate accuracy and dynamic performance of the proposed PVE. With resistive loads, fast load transients can be applied, that allows to test the dynamic performance of PVE under toughest transients.

1) Steady-state performance with resistive loads

The steady-state performance of the PVE prototype is tested by operating at different resistive load levels. Fig. 13 (a) and (b) show the output waveforms (i.e. v_C, i_O) of PVE in steady-state for load condition that lies in CVR and CCR respectively. Results shows that the peak-to-peak ripple of v_C is maintained at specified voltage ripple of 2 V and stable operation of PVE is achieved in both regions of the I-V curve. Fig. 14 illustrates the steady-state operating point trajectories for different load levels on I-V plane when PVE is intended to emulate a PV array with two BP365 modules connected in series. It is tested with a maximum load of 4.75 Ω and until open circuit voltage output and results are compared with the reference I-V curve of 1 kW/m^2 and 0.5 kW/m^2. Accuracy of PVE is evaluated by taking the average value of measured v_C, i_O and compare it with PLECS PV model simulation results. Table V presents the comparison results and it shows that error percentages are within 3.5 %. Furthermore, the efficiency of the system under different loading conditions is recorded as shown in Table V. It shows that the efficiency varies between 95% - 83% which agrees with the theoretical efficiency of the converter.

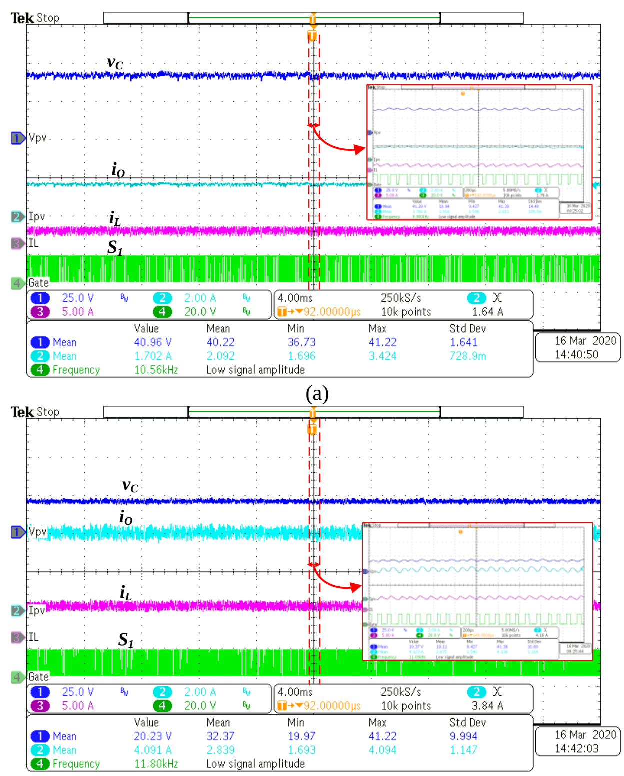


Fig. 13 Experimental results of steady-state operation with (a) 23.8 Ω (in CVR), and (b) 4.75 Ω (in CCR).

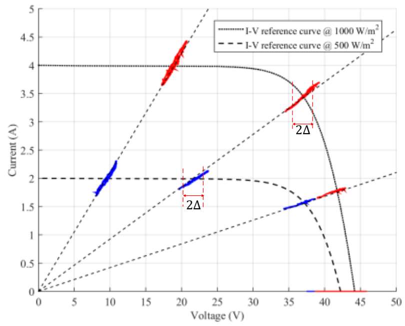


Fig. 14 Steady-state I-V trajectory with resistive loads.

TABLE V
PERFORMANCE EVAUATION OF THE PROPOSED PVE

	R_L	v_C (V)		Error %	i_O(A)		Error %	Efficiency (%)	
		PLECS	PVE		PLECS	PVE		Theo.	Meas.
1 kW/m²	23.8 Ω	41.78	41.39	0.93%	1.756	1.766	-0.6%	95.87%	94.84%
	10.8 Ω	37.09	36.89	0.54%	3.434	3.435	-0.1%	95.57%	93.40%
	4.75 Ω	18.95	19.37	-2.21%	3.988	3.988	0.0%	91.08%	87.43%
	OC	44.2	43.11	2.47%	0	-	0.00%	-	-
0.5 kW/m²	23.8 Ω	37.19	36.58	1.63%	1.562	1.547	1.0%	94.94%	94.61%
	10.8 Ω	21.53	21.78	-1.17%	1.993	1.973	1.0%	92.63%	91.72%
	4.75 Ω	9.48	9.54	-0.65%	1.995	1.994	0.0%	84.94%	83.41%
	OC	42.3	40.93	3.25%	0	-	0.0%	-	-

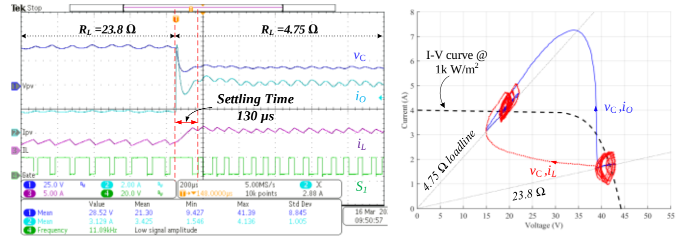
2) *Transient performance with resistive loads*

Experiments results for a load step down transient (23.8 Ω to 4.75 Ω) in time and I-V domains are shown in Fig. 15. This is tested under the condition of irradiance equals to 1 kW/m^2, T=25 ºC and recorded settling time is found as approx. 130 µs as shown in Fig. 15 (a). The PVE reaches steady-state within a few switching actions and operating switching frequency is in the range of 8.3 kHz to 12.5 kHz. The I-V trajectory during this transient is presented by Fig. 15 (b). Similarly, transient response for an irradiance step up from 0.5 kW/m^2 to 1 kW/m^2 is shown in Fig. 16. The output voltage is maintained within specified voltage band and recovers within ~130 µs to ±3.5 % of steady-state output value. Even though, the proposed PVE is 13 times (i.e. 130 µs compared to 10 µs) slower than a real PV array, it is still capable for testing MPPT converters that has a transient response time that vary between a few milliseconds to several seconds. However, a detailed investigation is required to identify the influence of control bandwidth of PVE on the stability of load converters.

Fig. 17 shows the measured closed-loop frequency response of inner BC loop at an operating point near MPP (v_S=60 V, v_C=35 V, i_O=3.5 A, f_S=11.6 kHz). As seen, gain of the closed-loop TF decreases around 11.5 kHz resembling low-pass filter characteristics with crossover frequency equal to f_s. This verifies the closed-loop bandwidth of the inner control loop is equals to the operating switching frequency.

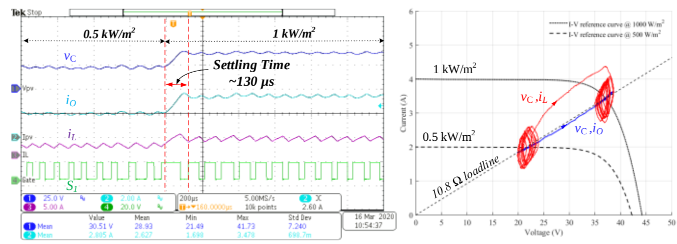
C. *Comparative Analysis with a Conventional PI-based PVE*

Experimental results of the proposed BC+IOIM control scheme is compared against a traditional VM PVE with PI+DRM as well as a PVE with PI+IOIM control to validate its fast dynamic performance and stable operation in both CVR and CCR of the I-V characteristic curve. Same parameters are used in the power stage for fair comparison, while the switching frequency of the PI-based PVE is chosen as 20 kHz. The PI



(a) (b)

Fig. 15 Experimental results for a load step down (23.8 Ω to 4.75 Ω at 1 kW/m^2) in (a) time domain (b) I-V plane.



(a) (b)

Fig. 16 Experimental results for a step change in solar irradiance from 0.5 kW/m^2 to 1 kW/m^2 at 10.8 Ω in time and I-V domain.

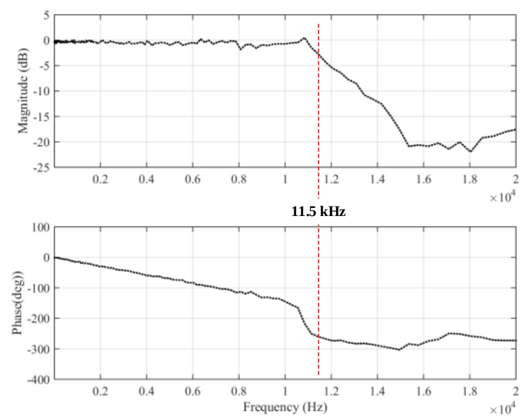


Fig. 17 Measured closed-loop frequency response of inner boundary control loop ($G_{inner}(s)$) at an operating point near MPP.

controller is designed with k_{P1}= 0.00057, k_{I1}= 38.45 to have a crossover frequency of 370 Hz at an operating point where the system is highly underdamped (i.e., near CVR, R_L = 87.7 Ω). Experimental results for the above mentioned three methods under load and irradiance transients are shown in Fig. 18 (a) and (b), respectively. As shown in Fig. 18, output waveforms of proposed PVE reach steady-state within 0.2 ms, providing a stable output in both regions of the I-V characteristic curve. In contrast, both PI-based PVEs show a slower response of about 2.8 ms, while the PVE with conventional DRM delivers an oscillatory output whenever it is operated in CCR. The PVE with PI+IOIM operates stably in both CVR and CCR since IOIM generates a stable reference signal allowing a design of a high bandwidth PI control loop. Similar outcome is noticed with a solar irradiance step change as shown in Fig. 18 (b) as the converter operates in CCR when conditions changed to 0.5 kW/m^2 at 10 Ω. The oscillatory output can be solved by designing a slower PI control loop as shown in Fig. 19 at the expenses of a slower dynamic response.

TABLE VI

DYNAMIC PERFORMANCE AND CHARACTERISTICS OF EXISTING PVES

Reference	Settling time for a load step change	Power Stage	Control Method		Controller Implementation
			Inner loop	RGA	
Nguyen-Duy 2016 [11]	10 μs (Fig.17 in [11])	Synchronous DC-DC buck converter with LCLC filter	PID (VM)	PV array small signal circuit	Analog circuit
Koran 2010 [14]	3.8 ms (Fig.17 in [14])	DC-DC buck converter with LCLC filter	PID (Current mode)	PV equivalent circuit	Analog circuit
Chang 2013 [29]	6 ms (Fig.12 in [29])	LLC resonant DC-DC converter	Frequency modulation control	Not found	Digital
Ayop 2019 [20]	21.25 ms (Fig.10 in [20])	DC-DC buck converter	PI control	Current-to-resistance PV model	Digital

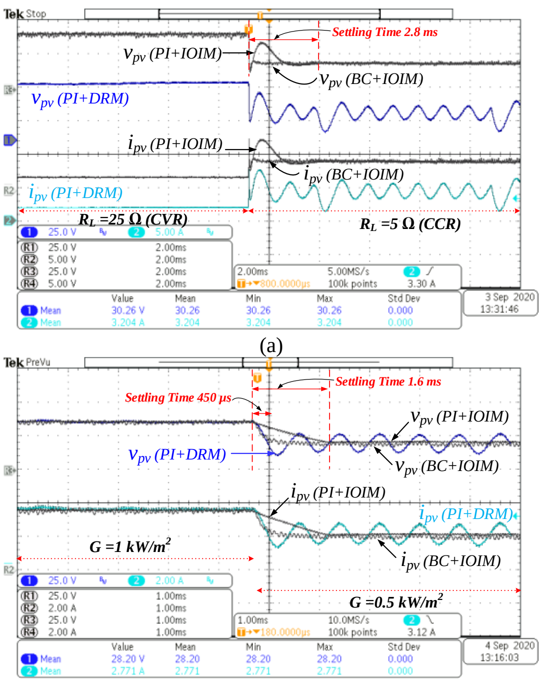


Fig. 18 Comparison of proposed PVE, traditional PVE with PI+DRM and PVE with PI+IOIM control under (a) a load step change from 25 Ω to 5 Ω at 1 kW/m² (b) a step change in solar irradiance from 1 kW/m² to 0.5 kW/m² at 10 Ω.

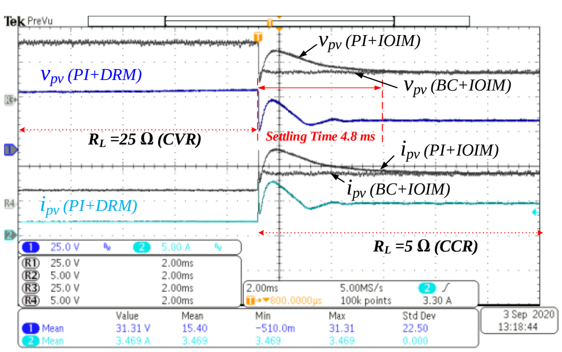


Fig. 19 Comparison of the proposed PVE, traditional PVE with PI+DRM and PVE with PI+IOIM control with a control bandwidth of 61 Hz (k_P= 0.00057, k_i= 6.4).

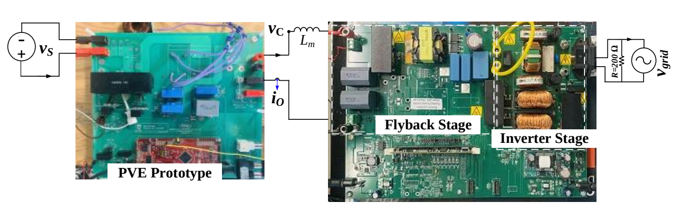


Fig. 20 Test setup schematic with the MPPT micro inverter.

Table VI summarises the dynamic performance of some of the key SMPS-based PVEs in recent works together with their characteristics. In [11], a control scheme is implemented via analog circuits with high switching frequency (i.e., 1 MHz) to achieve excellent dynamic characteristics. It is clearly seen from Table VI, and also from the experimental results of traditional PVE that the application of the BC+IOIM control for a synchronous buck converter can result in a better transient tracking performance and simultaneously having a stable operation in both CCR and CVR regions of the I-V characteristic curve.

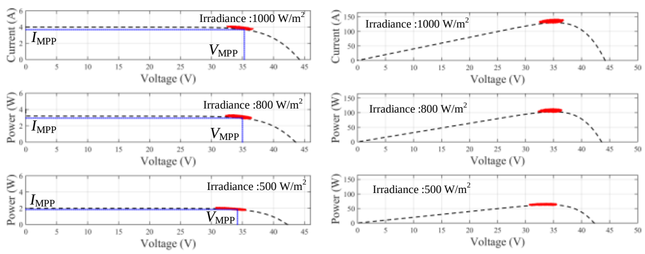
D. Proposed PVE – MPPT Micro Inverter Evaluations

The schematic of the experimental test setup is shown in Fig. 20. A filter inductor is placed between the PV emulator and the solar micro inverter to represent the EMI filter inductor. The flyback stage of the micro inverter controls the current from PV source such that the PV module operates at its MPP [30]. Technical specifications of the micro inverter are provided in Table VII. Experimental results under steady-state conditions are shown in Fig. 21, where I-V and P-V plots are presented for irradiance levels of 1 kW/m² 0.8 kW/m² and 0.5 kW/m². The plots verify its equilibrium operation around the MPP with a static MPPT efficiency above 94% and v_C is tightly regulated by the PVE at V_{mpp} with an accuracy of 1.7 %. Fig. 22 (a) shows the response of the proposed PVE for a solar irradiance step change from 0.5 kW/m² to 1 kW/m². It shows that the micro inverter was searching a new MPP after the change and reaches steady-state within 6.4 s. Here, the transient response time of the system depends on the control loop bandwidth of the flyback stage of the micro inverter. To demonstrate that it is operated at v_{mpp} and P_{max}, Fig. 22 (b) and Fig. 22 (c) present the waveform trajectory for different irradiance levels including 1 kW/m² and 0.5 kW/m² in the I-V and P-V plots. One possible reason for these minor discrepancies is the voltage drop across the equivalent series resistance (ESR) of the additional filter inductor. The micro inverter operated correctly with the proposed PVE since maximum power has been extracted under steady-state and transient conditions. Further, dynamic MPPT efficiency test is performed according to EN 50530 by applying test sequence for fluctuations between medium and high irradiation intensities [31]. The dynamic MPPT test result for a test sequence ramps of 40 % -100 % nominal power ($P_{DC,n}$) with a slope of 8.6 W/m²/s is shown in Fig. 23. It is seen that the PVE is fast enough to emulate such test patterns and micro inverter is capable of tracking the MPP under such irradiance fluctuations.

TABLE VII

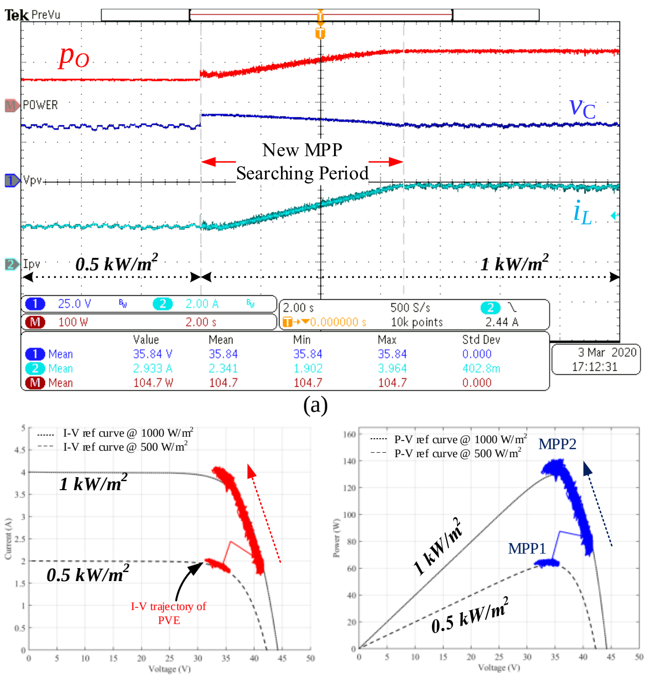
SPECIFICATIONS OF THE MPPT MICRO INVERTER

Parameter	Value	Parameter	Value
Solar Panel Output	25 V- 44V	EMI Filter Inductor	200 μH
Rated Power for 110Vrms	140 Wmax	Power Resistor	200 Ω



(a) (b)

Fig. 21 Steady-state experimental results of the proposed PVE with a MPPT micro inverter under 1000 W/m², 800 W/m² and 500 W/m² (a) I-V plot, (b) P-V plot.



(b) (c)

Fig. 22 Transient response of PVE with a MPPT micro inverter for irradiance step- up from 0.5 kW/m² to 1 kW/m² (a) time (b) I-V (c) P-V domain.

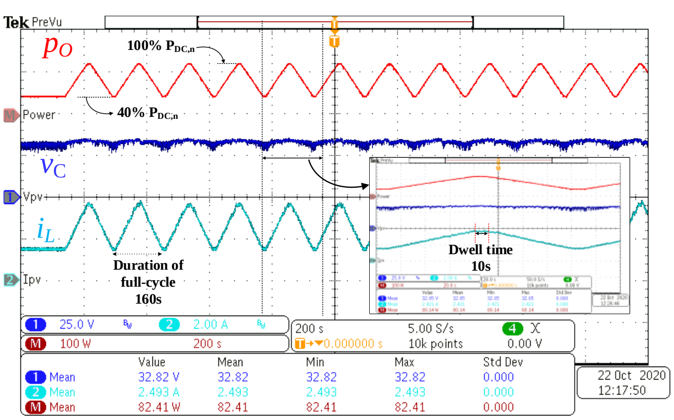


Fig. 23 Dynamic MPPT test under EN 50530 with proposed PVE.

VI. CONCLUSION

This paper presented a comprehensive voltage-mode control scheme for switch-mode PVEs to improve the dynamic response while maintaining the accurate emulation of I-V characteristic curve. An innovative IOIM controller is introduced to decouple the inner control loop response from the reference generation loop and to generate a stable voltage reference regardless of the operating point region in the I-V characteristic curve. A boundary control scheme is employed to control the output voltage at a given reference within two switching actions. Detailed mathematical procedures are provided to design the IOIM controller, BC loop and buck-stage inductor. The PVE parameters should be designed by taking the effect from load capacitance as well as considering the compromise between the switching frequency and the current ripple. The performance of the PVE was confirmed through experimental results in a 130 W laboratory prototype. Results shows that the dynamic response time of the system has reduced to hundreds of microseconds which enables the possibility to evaluate faster MPPT algorithms without increasing the switching frequency.

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