Design, Implementation, and Validation of Electro-Thermal Simulation for SiC MOSFETs in Power Electronic Systems

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***Abstract*– Silicon Carbide (SiC) MOSFETs are getting popular in high-frequency power electronic (PE) applications. More and more concerns for system efficiency and reliability are growing due to the increasing switching losses and thermal stress. In this paper, an electro-thermal simulation method for SiC MOSFETs in modern PE systems is proposed. In the device simulation, a behavioral transient model of SiC MOSFETs is developed and used for generating a multi-dimensional power loss table in a wide range of operating conditions. The effects of parasitic elements, temperature-dependent parameters, and reverse recovery effect of the diode are taken into account. Furthermore, the power loss look-up table is integrated into the PE system simulation with an additional Cauer-based dynamic thermal model considering heatsink impact. In this way, the instantaneous power losses and junction temperature can be obtained respectively with fast simulation speed, reasonable accuracy, and improved simulation convergence. The proposed approach is implemented in PSCAD/EMTDC and further validated by the experimental results of a double pulse test (DPT) setup and a Power Factor Correction (PFC) system.**

***Index Terms*—Silicon Carbide (SiC) MOSFETs, power loss, behavioral model, electro-thermal.**

I. INTRODUCTION

In the last decade, Silicon Carbide (SiC) MOSFETs as a kind of wide-bandgap (WBG) semiconductor devices have been rapidly developed with superior features such as high breakdown voltage, fast switching speed, and high thermal conductivity [2]. They are increasingly used in many modern power electronic (PE) applications (e.g. Photovoltaics (PV) [3], Power Factor Correction (PFC) [4], and power supply [5]). On one hand, the higher switching frequency enabled by the use of SiC MOSFETs can result in smaller filter size, higher power density, and higher efficiency for PE systems. On the other hand, the increase of switching losses and thermal stress along with the intense impact of circuit parasitic components on the switching behavior may lead to device fatigue failure and thus counteract the benefits of using SiC devices. Therefore, an accurate approach for evaluating the power losses and thermal performance of SiC MOSFETs in PE systems is necessary and promising for both system design and optimization.

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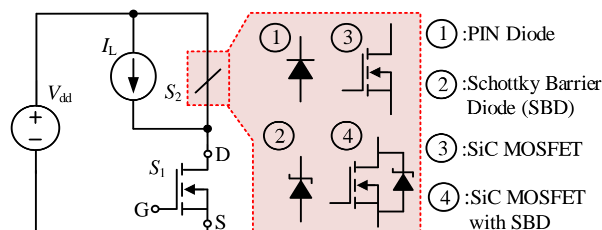


Fig. 1 Basic switching commutation unit.

One straightforward method of determining the power losses of semiconductors is capturing their switching transients with a double pulse test (DPT) setup [6]-[7]. Apart from the tedious process for different permutation of test conditions, it has to be a well-designed setup with low parasitics and high bandwidth probes are needed especially for SiC MOSFETs. The conduction loss can be obtained based on the conduction current and the on-state resistance in the datasheet, while the switching losses are more complicated and required transient analysis. For decades, a great research effort has been made in developing various SiC MOSFET loss models from various perspectives [8]. Physical models can accurately reproduce the device switching behavior based on the internal physical structure of the device [9]-[14]. The model in [11] features a physical description of the channel current and internal capacitances, whereas the interactive behavior of the diode is not fully considered. Built-in Spice MOSFET model [12] (in pair with Schottky diode [13] or a half-bridge module [14]) is widely used for device-level study but only for a specific device in a specific simulator and the impacts of parasitics as well as thermal-dependent parameters are normally ignored. Generally, it is difficult to obtain the physical parameters of the device, and additional measurement or numeric method (e.g. finite element analysis) is usually required. Behavioral models [15]-[17] can achieve fast simulation speed by mathematical fitting the external characteristics of the device, but hardly being able to describe the switching behavior in all the operating conditions.

Recently, several analytical loss models for SiC MOSFETs [18]-[19] have been developed to compute the power loss by the derived mathematical equations for transient equivalent circuits. Piecewise linearizing the switching process of the device is a commonly used method for loss calculation due to its simplicity [20]. However, the impacts of parasitics are not considered. To improve the accuracy, various impacts on the switching behavior of the device have been taken into consideration, such as the effects of parasitic elements [21], the interaction of the PIN diode or Schottky Barrier diode (SBD) [22], and other new insights (e.g. carrier-trap influences [23], ringing losses [24], non-flat miller plateau [25] and

displacement current [26]). Xuan Li, *et al.*[27] developed the model considering the effect of parasitic capacitance and D. Christen, *et al.*[28] proposed the loss model in a half-bridge configuration. Nevertheless, the temperature-dependent parameters [29] are not mentioned in these models and iterative processes for solving equations are normally involved. The idea of conservation of energy [30] has been applied to the losses calculation which usually requires numerical calculation (e.g., Laplace transform [31] and state equations [32]).

As for the thermal performance evaluation, simple thermal resistances between different layers are commonly used to represent the heat transfer process for steady-state thermal analysis and the junction temperature can be further computed. For dynamic thermal analysis, thermal impedance is required to be taken into consideration and the comprehensive thermal analysis can be conducted using the finite-element method (FEM) [33] with high accuracy. However, it is complicated and numerous geometry data, as well as thermal material properties, are not attainable for PE designers. Generally, RC thermal network such as Cauer network [34] and Foster network [35] are more widely used thermal models which can be transformed into each other by mathematical method. By combining a circuit simulator with a thermal model, several research efforts on developing an electro-thermal model have been made in the literature [36]-[38]. However, most of these models require the use of proprietary software or external solvers to accomplish the simulation, and convergence problem often exists.

To solve these issues, a comprehensive electro-thermal simulation method for SiC MOSFETs in PE systems is proposed in this paper. The commutation unit in Fig. 1 is considered here, which is widely used as a basic switching cell in PE systems. S_1 stands for SiC MOSFET and S_2 can be PIN diode (Conf.1), SBD (Conf.2), or SiC MOSFET with/without SBD (Conf.3/4). V_{dd} and I_L are the circuit voltage and current respectively. It is an enhanced method of [39]. There are two technical contributions in this paper.

1) A behavioral transient model of SiC MOSFETs is proposed in device simulation to reproduce the switching transient waveforms using equivalent voltage/current source with passive components. Moreover, the detailed switching process is discussed analytically considering various commutation units, the impacts of parasitics, reverse recovery behavior of diode, and thermal-dependent parameters. The parameter-extraction procedure is also introduced.

2) A multi-dimensional power loss look-up table (LUT) in a wide range of operating conditions (e.g. voltage, current, temperature) is generated by the device simulation using the proposed SiC MOSFETs model. A PE system simulation using a simple switch model is further implemented in PSCAD along with the additional dynamic thermal network. The instantaneous power loss of the device can be obtained by power loss LUT and inputs to the thermal model, meanwhile, the output temperature is influenced back to the PE simulation.

In this way, a closed-loop electro-thermal simulation is realized. Both the power loss and thermal performance of SiC MOSFETs in the PE system can be evaluated in the same simulator. Besides, the nano-second (ns) and micro-second (μs) time steps are adopted for the device and PE system simulation, respectively. Hence, a good tradeoff among accuracy, speed, and complexity can be achieved.

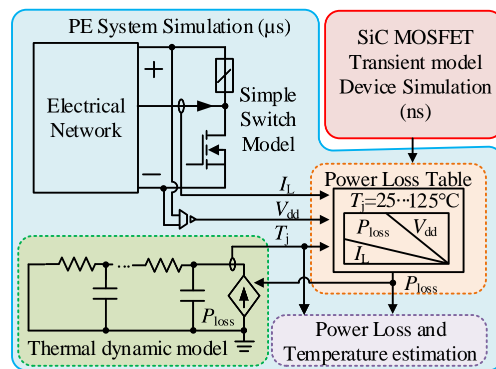


Fig. 2 Block diagram of the proposed simulation strategy.

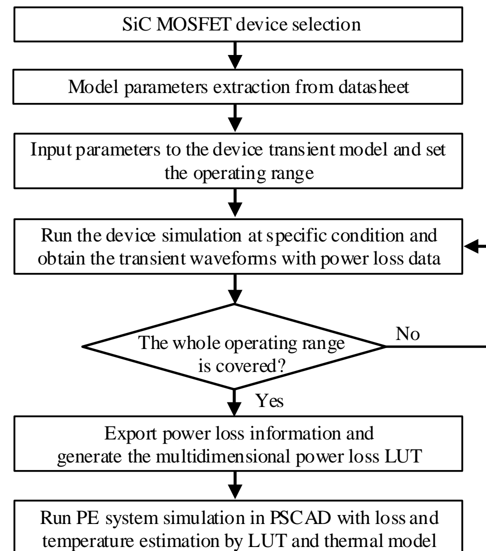


Fig. 3 Flow chart of the proposed simulation approach.

II. Overview of Simulation Strategy

Providing fast and accurate power losses and junction temperature estimation of SiC MOSFET in the PE system is the primary objective of the simulation. Fig. 2 shows a block diagram of the proposed simulation strategy which includes two stages, device simulation, and system simulation. The flow chart of the proposed approach is shown in Fig. 3.

In the device simulation, a clamped inductive switching circuit in Fig. 1 is implemented in the Electromagnetic Transients Program (EMTP) simulator (e.g. PSCAD/EMTDC) using the transient model of SiC MOSFETs for the switching devices. According to the operating region of the targeted PE system and the device datasheet, the model parameters along with corresponding system operating conditions can be obtained and set for the device simulation. The power losses of SiC MOSFETs including conduction and switching losses can be further computed by integrating the product of the device voltage and current. Generally, the switching transient time of SiC MOSFETs is within a few hundred ns. Thereby, the simulation time step is recommended to set 1 ns or less for the reason of high accuracy. Since only several tens of points will be simulated for one switching cycle, it will require a reasonable computational time. By setting the range of the desired operating conditions (junction temperature T_j, V_{dd} and I_L) in PSCAD, the power loss LUT can be generated and exported for further extension to system applications.

In the system simulation, a PE circuit with a simple switch model will be implemented in another simulation file with μs time step. At each switching action, the instantaneous power losses (P_{loss}) will be computed through LUT interpolation based on the instantaneous operating conditions (V_{dd}, I_L) as well as T_j from the additional dynamic thermal model. Moreover, T_j is also updated based on P_{loss}. This closed-loop simulation is a simple search method and mathematical calculation, thus it will not significantly increase additional computational time in comparison with the current method in PSCAD that using two-resistance for switches.

III. SiC MOSFET Model Description

A. Behavioral Transient Model of SiC MOSFET

A behavioral transient model of SiC MOSFET in Fig. 4 is proposed which consists of gate loop, MOS channel, and diode parts. The lower side switch S_1 is SiC MOSFET and the upper side switch S_2 serves as a freewheeling diode which can be realized by the four configurations as mentioned previously. Notice that C_{gd1}, C_{gs1} and C_{ds1} are the junction capacitances among gate, drain, and source nodes of S_1, respectively. Based on the realization of the switch S_1 and S_2, the corresponding equivalent parasitic capacitance (C_{eq}) can be expressed as,

$$C_{eq}=\begin{cases} C_{oss} & \text{, Conf.1 and Conf.3} \\ C_f & \text{, Conf.2} \\ C_{oss}+C_f & \text{, Conf.4} \end{cases} \quad , \qquad (1)$$

where C_{oss} is the output capacitance of SiC MOSFET and C_f is the junction capacitance of SBD. Note that, C_{eq1} equals to the output capacitance of S_1 (C_{oss1}) for the case of single SiC MOSFET as the switch S_1 in this paper. In addition, the drain current (i_d) of S_1 can be expressed by,

$$i_d = i_{ch} + i_{gd} + i_{ds} \qquad (2)$$

where i_{ch}, i_{gd} and i_{ds} are the MOS channel current, gate-drain current, and drain-source current, respectively.

The typical transient waveforms are shown in Fig. 5, which includes two switching actions, turn-on (t_0–t_4) and turn-off (t_5–t_8) [28]. The equivalent circuit for the voltage transition period is also shown in Fig. 6. The modeling process is illustrated in detail as follows.

1) Gate loop – the gate-drive voltage v_G is assumed to switch between V_{goff} (e.g. -5V) and V_{gon} (e.g. 20V). The internal gate resistance R_{gint} along with the external gate resistance R_{gext} forms the total gate resistance R_G. And the nonlinear junction capacitance is represented by the input capacitance C_{iss} with the equivalent voltage source v_{mil} for miller plateau [40].

$$v_{mil} = \frac{i_{mos}}{g_{fs}} + v_{th}. \qquad (3)$$

where v_{th} and g_{fs} denote the threshold voltage and the trans-conductance of SiC MOSFET respectively. i_{mos} is the total current flowing through the SiC MOSFET.

The common source parasitic inductance L_{cs} is also taken into account which exists both in the gate loop and MOS channel part for the reason of decoupling both parts. Additionally, an equivalent voltage source v_{Lcs}, is added in the gate loop to represent the corresponding interaction effect.

$$v_{Lcs} = L_{cs} \cdot \frac{di_{mos}}{dt}. \qquad (4)$$

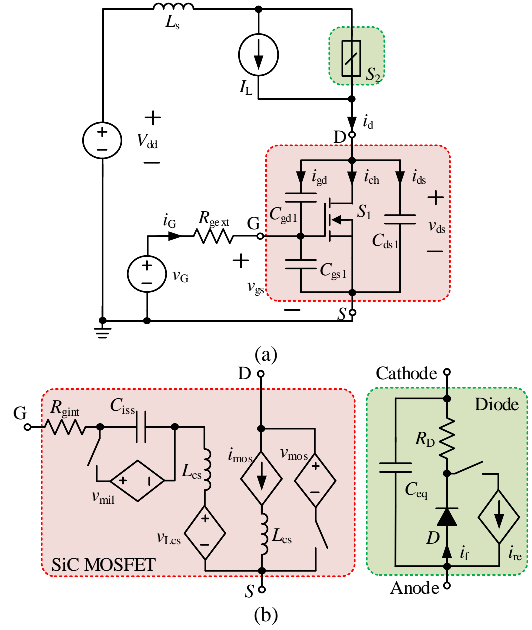


Fig. 4 (a) DPT equivalent circuit; (b) behavioral model of SiC MOSFET.

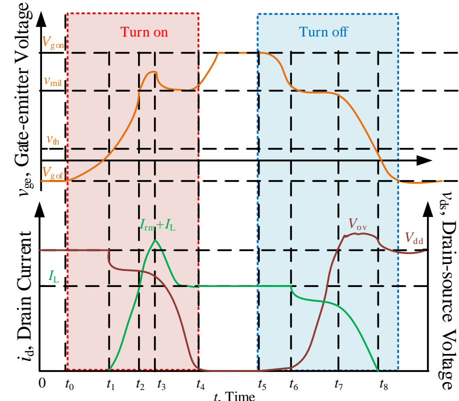


Fig. 5 Typical waveforms during switching transient.

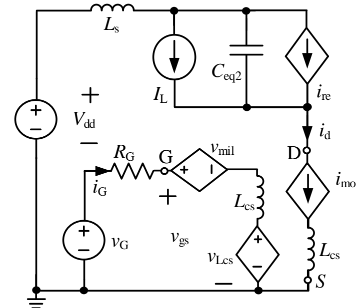


Fig. 6 Equivalent circuit during voltage transition.

2) MOS channel - an equivalent current source i_{mos} with the voltage source v_{mos} is used to represent the static characteristic of SiC MOSFET. v_{mos} stands for the on-state voltage drop which can be express as

$$v_{mos} = R_{DS(on)} \cdot I_L, \qquad (5)$$

where $R_{DS(on)}$ denotes the drain-source on-state resistance and I_L serves as the load current of the circuit. Detailed derivation of i_{mos} will be discussed in section III-B. Besides, it is also worthy to remark that all the stray inductances in the power loop are lumped and represented by L_s and the gate inductance is neglected here for simplicity.

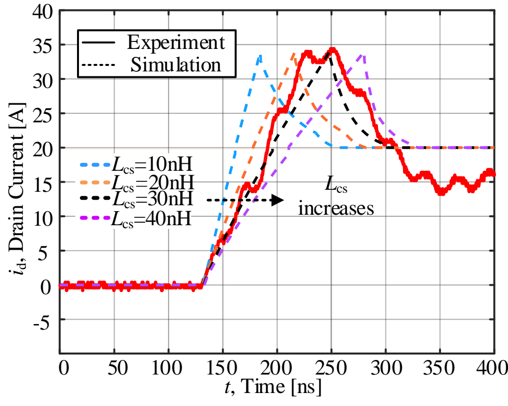
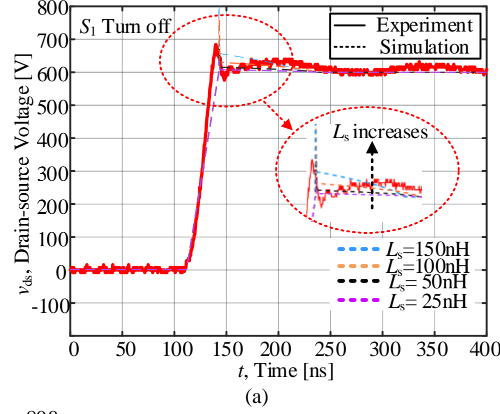
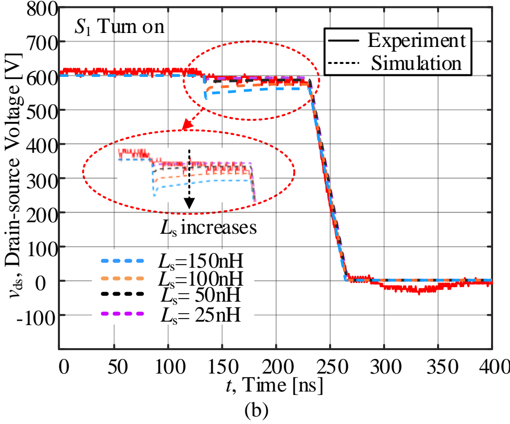


Fig. 7 Effect of common source parasitic inductance on current



(a)



(b)

Fig. 8 Effect of L_s on v_{ds} (a) turn-on, and (b) turn-off.

3) Diode - the static characteristic of body diode can be simply represented by the forward resistance R_D which can be obtained from the diode I-V curve in the datasheet. In addition, an equivalent current source i_{re}, as expressed in (6), is employed in this model to describe the reverse recovery behavior of diode. When the forward current i_f becomes negative and the reverse recovery process begins [39].

$$i_{re} = \begin{cases} di_f/dt \cdot t, t < t_{rm} \\ I_{rm} \cdot e^{\frac{t-t_{rm}}{\tau_{re}}}, t > t_{rm} \end{cases}. \quad (6)$$

where τ_{re} stands for decay time constant. The reverse current reaches the peak value I_{rm} at t_{rm}. It should be mentioned that the reverse recovery characteristic commonly exists in PIN diode or body diode of SiC MOSFET, while majority-carrier devices (e.g. SBD) can ignore the recovery time. In that case, the junction capacitance C_f is the main concern of SBD which will be discussed in Section III-B.

B. Switching Transient Modeling

Generally, the parasitic parameters such as inductance and capacitance are inevitable in PE systems and it will have a significant impact on the switching behaviors especially for SiC MOSFET due to its fast switching speed. Hence, the effect of parasitic elements is considered in the transient model and is studied in detail. It is assumed that during the switching transient, V_{dd} and I_L remain constant which is reasonable for such a short switching period.

1) Turn-on process (t_0~t_4) - V_{gon} is provided through R_G to charge C_{iss}, and subsequently the gate-source voltage v_{gs} will increase gradually. Once v_{gs} reaches to v_{th}, the conduction channel is built and i_d can be modeled as a current source i_{mos}, which is linked by g_{fs} and v_{gs},

$$i_{mos} = g_{fs} \cdot (v_{gs} - v_{th}). \quad (7)$$

It is noted that L_{cs} provides negative feedback from the power loop to the gate loop which will introduce an extra voltage drop v_{Lcs} due to the fast change of i_d. As shown in Fig. 7, the slew rate of i_d is influenced by L_{cs} and as a result, the turn-on time and corresponding power losses will increase.

As soon as i_d rise to I_L, v_{gs} will be clamped at v_{mil} and an additional current in (6) will be added to i_{mos} due to the reverse recovery behavior of the upper-side diode. During the current rising period, v_{ds} is almost constant with a slight decline due to the stray parasitic inductance L_s as shown in Fig. 8(a). Once i_{re} hits the peak I_{rm}, the voltage transition period begins and the equivalent circuit is shown in Fig. 6. Thereby, v_{ds} starts decreasing as

$$dv_{ds}/dt = -(v_G - v_{mil})/(C_{gd1} \cdot R_G). \quad (8)$$

As v_{ds} drops significantly, the special concern of the effects of parasitic capacitances of both switches (C_{eq1} and C_{eq2}) are required to be considered. A displacement current will be generated due to the charging and discharging process. Based on the definition of output capacitance of S_1 ($C_{oss1} = C_{gd1} + C_{ds1}$), the corresponding capacitance current (i_{oss1}) can be expressed by,

$$i_{oss1} = i_{gd} + i_{ds} = C_{oss1} \cdot dv_{ds}/dt = C_{eq1} \cdot dv_{ds}/dt. \quad (9)$$

During this period, v_{ds} is decreasing to v_{mos}, meanwhile C_{eq1} is discharged and, simultaneously, C_{eq2} is charged. Since the voltages of these parasitic capacitances are clamped to V_{dd}, they share the same absolute value of voltage slope (dv_{ds}/dt). Applying Kirchhoff's law to the drain node of S_1, i_d can be expressed as

$$i_d = i_{mos} = I_L + i_{re} - C_{eq2} \cdot dv_{ds}/dt. \quad (10)$$

Combining (2), (9), and (10), the MOS channel current (i_{ch}) can be further obtained,

$$i_{ch} = i_{mos} - i_{oss1} = I_L + i_{re} - (C_{eq2} + C_{eq1}) \cdot dv_{ds}/dt. \quad (11)$$

As a result, v_{mil} will change accordingly as expressed by,

$$v_{mil} = \frac{i_{ch}}{g_{fs}} + v_{th} = \frac{I_L + i_{re} - (C_{eq1} + C_{eq2}) \cdot dv_{ds}/dt}{g_{fs}} + v_{th}. \quad (12)$$

At t_4 in Fig. 5, SiC MOSFET is fully turned on, and v_{gs} will continue climbing until it reaches V_{gon}. The on-state device is modeled as v_{mos} in (5).

2) Turn-off process ($t_5 \sim t_8$) - The turn-off process is almost the inverse sequence of the turn-on process. As the negative V_{goff} is applied at t_5, v_{gs} begins decreasing by discharging C_{iss} and then v_{ds} starts to rise. Again, the displacement current will occur resulting in a reduction in current accordingly.

$$i_{mos} = I_L - C_{eq2} \cdot dv_{ds}/dt. \quad (13)$$

Once v_{ds} rises to V_{dd}, the current commutation between S_1 and S_2 begins and a resulting overvoltage V_{os} is induced by L_s. As shown in Fig. 8(b), this voltage spike can be significant and even damage the device. Therefore, a proper layout design to reduce L_s or sacrifice the switching speed may be the solution to mitigate this overvoltage issue.

Based on the above analysis, the expression of i_{mos} of SiC MOSFET can be summarized as,

$$i_{mos} = \begin{cases} 0, v_{gs} < v_{th} \\ g_{fs} \cdot (v_{gs} - v_{th}),\ v_{gs} > v_{th} \text{ and } i_{mos} < i_L. \\ I_L - C_{eq2} \cdot dv_{ds}/dt + i_{re}, dv_{ds}/dt > 0 \end{cases} \quad (14)$$

C. Thermal Dynamic Model

In a PE system, SiC MOSFET is typically mounted on a heat sink which can be basically separated into four thermal layers as shown in Fig. 9. The power loss heat energy generated from the junction is transferred to the case and heatsink with a thermal pad in between and eventually dissipated to the ambient. For steady-state thermal analysis, this heat transfer process can be represented by the thermal equivalent network using thermal resistance between different layers and the junction temperature of the power device T_j can be computed based on the power dissipation P_{loss} and the ambient temperature T_a which is considered as constant here.

For modeling the dynamic thermal behavior of the device, thermal capacitances are essential for forming a thermal dynamic model with thermal resistance. RC thermal networks in Cauer-type and Foster-type are commonly used. In essence, the former is based on the internal physical layers of the device and thus computationally complex to implement. While the latter is a behavioral model and the thermal parameters can be obtained from the device datasheet. In this paper, a thermal dynamic model of SiC MOSFET based on both Cauer and Foster RC network is developed and implemented in PSCAD as shown in Fig. 9.

The Foster-type RC elements of thermal impedance from junction to case Z_{jc} can be initially extracted by curve fitting the transient thermal curve in the datasheet.

$$Z_{jc} = \sum_{i=1}^{n} R_{thFi} \cdot (1 - e^{-\frac{t}{\tau_{thFi}}}). \quad (15)$$

It can be noted that a 2nd order Foster network is adopted in this paper for simplicity. Thus the number of exponential terms n equals 2 here and τ_{thFi} ($R_{thFi} \cdot C_{thFi}$) are time constants.

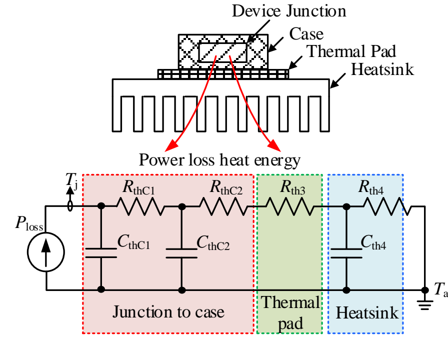


Fig. 9 Thermal dynamic model.

A thermal pad (Sil-Pad® 400 [44]) as thermal interface material is used and attached between the device case and heatsink. The corresponding thermal resistance R_{th3} can be obtained from the datasheet. In addition, an individual heatsink from Wakefield-Vette (OMNI-UNI-27-25) is adopted, and the thermal resistance and capacitance (R_{th4} and C_{th4}) can be further obtained based on heatsink datasheet and the material (Aluminum 6063-T5) data [45]. All the thermal-related parameters are illustrated in Table I.

D. Model Parameter Extraction

The main parameters of the device can be extracted from the device datasheet. As an example, the SiC MOSFET (SCT2080KEC) from ROHM is selected, which is normally operated at $V_{dd} = 600$V and I_L varies in the range of [0A, 40A]. The parameter extraction is discussed in detail as follows.

1) MOSFET parameters - To describe the switching transient behavior of SiC MOSFET, two key parameters (i.e. v_{th} and g_{fs}), are needed to be determined first. These two parameters are generally assumed as constant values. However, it is found that v_{th} is a thermal-dependent parameter that can be fitted by a quadratic function of T_j,

$$v_{th}(T_j) = k_{Ta} \cdot T_j^2 + k_{Tb} \cdot T_j + k_{Tc}, \quad (16)$$

where k_{Ta}, k_{Tb} and k_{Tc} are fitting constants.

Moreover, g_{fs} is nonlinear and related to the channel current which has been given little attention in the literature. According to the transfer curve from the device datasheet, i_{mos} can be fitted by (17) and comparing with (7), g_{fs} can be further derived as (18), where k_a and k_b are curve fitting coefficients.

$$i_{mos} = k_a \cdot (v_{gs} - v_{th})^2 + k_b. \quad (17)$$

$$g_{fs} = i_{mos} \cdot \sqrt{k_a/(i_{mos} - k_b)}. \quad (18)$$

It is well known that the junction capacitances, namely input, output, and reverse transfer capacitance (C_{iss}, C_{oss} and C_{rss}) of SiC MOSFET, is a function of v_{ds}. Besides, C_f in SiC SBD is associated with the reverse voltage. Based on that, all the capacitances can be obtained by fitting the capacitance curves in the datasheet by (19), where C_{hv} is the capacitance at high voltage range and k_{ca}, k_{cb}, k_{cc} and k_{cd} are all fitting constants which are listed in Table I for this case [32].

$$C = C_{hv} + k_{ca}/(1/k_{cb} + v^{k_{cd}}/k_{cc}). \quad (19)$$

As mentioned before, the on-state device can be modeled as v_{mos} which is related to $R_{DS(on)}$ and the drain current. It is noted that $R_{DS(on)}$ is also an important temperature-dependent parameter that can be fitted by (20) from the datasheet, where k_R is the fitting constant.

$$R_{DS(on)}(T_j) = R_{DS(on)}(T_a) \cdot \left(\frac{T_j+273}{T_a+273}\right)^{k_R}. \quad (20)$$

2) Body diode parameters - In the diode model, the forward conducting and reverse recovery behavior of the diode are considered. Note that the effect of reverse recovery current can be ignored for the SiC SBD case as mentioned previously. The reverse peak current I_{rm} and time constant τ_{re} can be extracted from the diode I-V curve and the charging curve in the datasheet based on the equations given as [46],

$$\begin{cases} \tau_{re} = \frac{1}{ln10}(t_{rr} - I_{rm}/(di_f/dt) \\ I_{rm} = \sqrt{Q_{rr} \cdot di_f/dt} \\ t_{rr} = 2 \cdot \sqrt{Q_{rr}/(di_f/dt)} \end{cases} . \quad (21)$$

TABLE I KEY PARAMETERS OF SIC MOSFET MODEL

Parameter	Value	Parameter	Value
R_{gint}	6.3Ω	$R_{DS(on)}(T_a)$	80mΩ
k_{Ta}	0.0000312	k_{Tb}	-0.01217
k_{Tc}	3.257	R_D	0.214Ω
L_{cs}	30nH	L_s	50nH
k_a	0.1314	k_b	-1.993
k_R	1.396	R_{th3}	1.13 K/W
R_{th4}	5 K/W	C_{th4}	28.13 J/K
R_{thF1}	0.2366	R_{thC1}	0.2296
R_{thF2}	0.2083	R_{thC2}	0.2153
C_{thF1}	0.2006	C_{thC1}	0.0098
C_{thF2}	0.01026	C_{thC2}	0.2102
Heat Capacity	0.900 J/(g·K)	Heatsink Density	2.7 g/cm^3

	C_{hv}	k_{ca}	k_{cb}	k_{cc}	k_{cd}
C_{iss}	2239	38.17	39.04	64.47	3.001
C_{oss}	77	35.45	104.1	90.48	0.8351
C_{rss}	16	26.47	68.47	96.76	2.279

3) Parasitic inductance - To accurately extract the parasitic inductance from the device datasheet is rather challenging. Often, only the parasitic inductance inside the semiconductor module is given by the manufacturer. While the others such as L_s and L_{cs} are dependent on the specific printed circuit board (PCB) design and the corresponding device package which are difficult to measure and can be computationally extracted by ANSOFT or Maxwell Q3D [47]. In this paper, L_s and L_{cs} are initially estimated based on the PCB trace length of the power loop and gate loop [48] as well as the device package (e.g. 2–5nH for TO-247 [49]). If the experimental results of switching transient waveforms are attainable, the parasitic inductance can be further calibrated and determined approximately, which is able to result in a good agreement between simulated and experimental results. For example, it can be seen from Fig. 7 and Fig. 8, the simulated results with the condition of $L_s =$ 50nH and $L_{cs} =$ 30nH matches well with the experimental results comparing with other conditions. Therefore, the inductance value can be estimated accordingly.

IV. EXPERIMENTAL VERIFICATIONS

The key objective of the proposed approach is to evaluate the power dissipation along with the thermal performance of SiC MOSFETs in a PE system simulation with acceptable accuracy and relative fast simulation speed.

A. Device-level Verification

In order to characterize the semiconductor and further validate the proposed transient model of SiC MOSFET, a DPT setup in Fig. 10 is designed and implemented based on Fig. 1. The device under test (DUT) is the lower side SiC MOSFET (SCT2080KEC, Rohm), and the upper side device using the body diode of the same SiC MOSFET as a freewheeling diode. These two devices are placed on top and bottom sides respectively to reduce the parasitic inductance. The driver IC with the type IXDN609SI is adopted as the gate driver providing 20V/-5V drive voltage. One 0.1 Ω current shunt resistor (SDN-414-01) is inserted to measure the switching current of the DUT. And v_{ds} is measured directly by a high-bandwidth passive voltage probe (TTP800). In addition, the DSP-controlled thermal heater and cooling fan are implemented for the operating junction temperature control. Also, the temperature is monitored by a thermal imager (Tis40, Fluke).

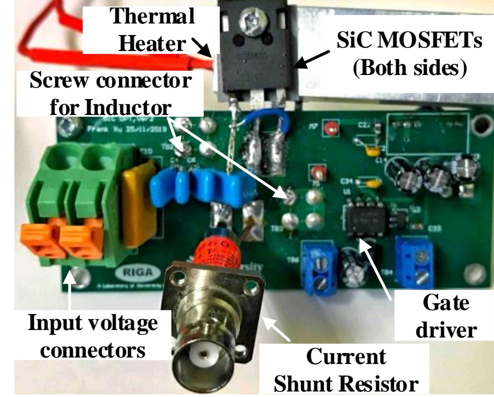


Fig. 10 Double pulse test setup.

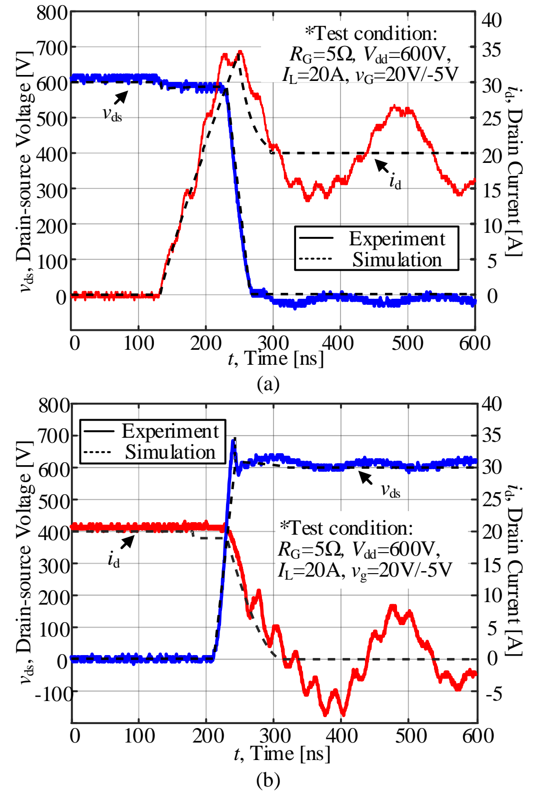


Fig. 11 Switching transient waveforms (a) S_1 turn on, (b) S_1 turn off @25℃.

1) Switching waveforms verification - The DPT simulation results of switching voltage and current waveforms using the proposed transient model in PSCAD/EMTDC are compared with experimental results in Fig. 11 (a) for turn-on transient and (b) for turn-off transient. It can be observed that during the

current rising period, around 50V voltage drop of v_{ds} occurs due to the impact of L_s and the additional overcurrent of i_d caused by the reverse recovery behavior of diode also can be seen. During the turn-off period, the peak voltage of v_{ds} can reach 700V due to the voltage across L_s. Therefore, special concern should be paid to reduce the parasitics in the PCB design process. Generally, the results show that the dynamic changes of voltage and current in simulation match well with the experimental results which validate the accuracy of the proposed model. However, it is also noticed that the current has a ringing period due to the resonance of parasitics which is ignored here for simplicity. Further investigation is needed.

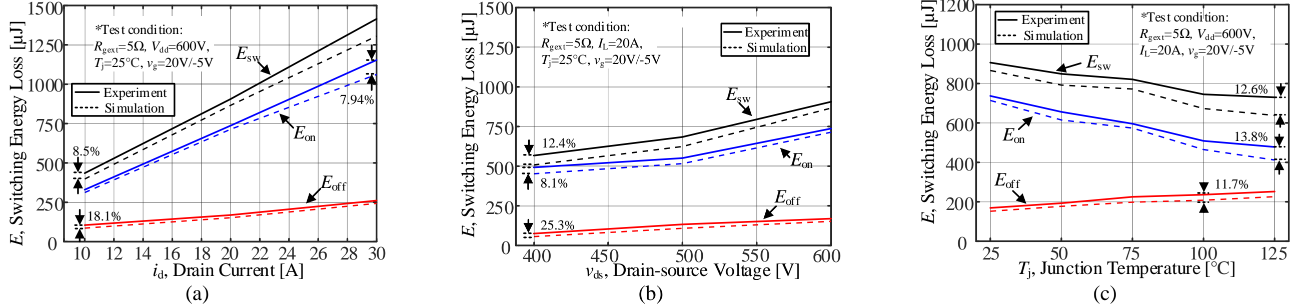


Fig. 12 Switching losses of SiC MOSFET in PFC application under different operating conditions (a) current, (b) voltage, (c) temperature.

2) Switching loss validation - The power losses of SiC MOSFET is further evaluated for different operating conditions. The simulated results in comparison with experimental results are presented in Fig. 12. In general, by using the proposed method, the power losses in a wide range of operating conditions can be estimated with reasonable accuracy. It is also found that the turn-on loss is more significant than the turn-off loss, while the latter has fewer changes than the former. The average error is within 10% and the loss discrepancy increase for the high-temperature condition. The main reason can be the ringing loss caused by ignorance of the impacts of the resonance of parasitics and the non-ideal recharging process of parasitic capacitance for simplicity. Apart from the error of parasitic parameter extraction, the thermal-dependent parameters (e.g. g_{fs} and diode parameters) cannot be fully considered [50]-[51]. This information is usually not available in the datasheet and further investigations are needed.

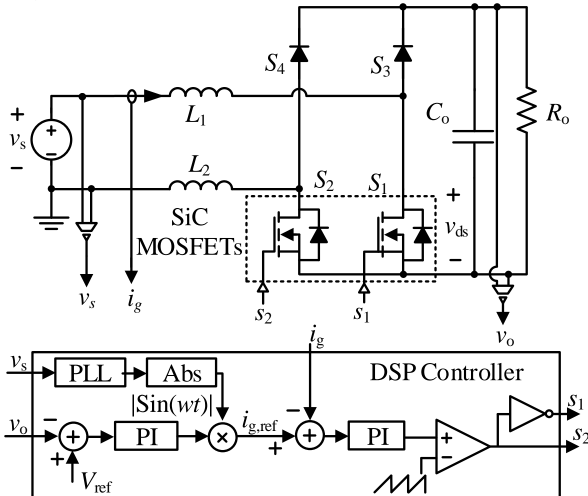


Fig. 13 Schematic of PFC application.

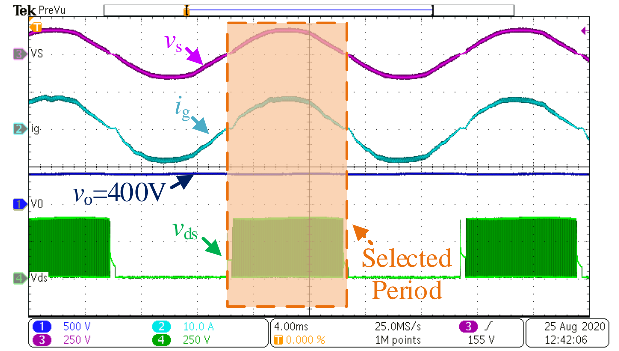


Fig. 14 Measured system waveforms of PFC.

TABLE II KEY PARAMETERS OF PFC APPLICATION

Parameter	Value	Parameter	Value
v_s(rms)	120V,60Hz	v_o	400-600V
L_1&L_2	1.03mH	C_o	453.33μF
R_o	226.67-680Ω	f_{sw}	50kHz
S_1&S_2	SCT2080KEC	S_3&S_4	C4D20120D

B. System-level Verification

In order to further validate the proposed approach for power loss and thermal estimation in a PE system, a bridgeless PFC converter [52] as an example in Fig. 13 is built and also implemented in PSCAD using a simple switch model with an additional LUT method and dynamic thermal model. This designed PFC converter uses SiC MOSFETs as high-frequency switches (S_1 and S_2) paired with SiC SBD (S_3 and S_4) and runs under different voltage and power conditions. The switching devices are operated as the complementary pairs S_1/S_3 and S_2/S_4 in accordance with grid voltage v_s. In addition, two PI loops are employed and implemented in DSP to control the output voltage v_o and grid current i_g. The PFC system are tested and simulated under three different v_o and resistive load R_o(Case 1: 400V, 267Ω; Case 2: 500V, 400Ω; Case 3: 600V, 680Ω). The key parameters are listed in Table II.

1) Power loss estimation - Fig. 14 shows the steady-state waveforms of the PFC converter for Case 1. It can be seen that v_o maintains at targeted 400V and i_g synchronizes well with v_s. The SiC MOSFETs cooperate well with SiC SBDs at half cycle high-frequency switching and half-cycle continuous conducting. Notice that one-half positive grid cycle data is

selected for conduction power loss computation. Since the conduction current of S_1 is the same as i_g when S_1 is on, thus the corresponding conduction power can be obtained by the product of i_g and v_{ds} for each on-state period. As the PFC starts running and reaches the thermal steady-state, the conduction power loss keeps changing due to the thermal-dependent $R_{DS(on)}$. The conduction power results at 10s and 1200s (considered as the thermal steady state) are measured respectively and compared with the simulated results in Fig. 15 and Table III. It can be noticed that the proposed model shows good reproducibility of the instantaneous conduction power. As v_o rises from 400V to 600V, the average conduction power decreases accordingly due to the decrement of the current. On the other hand, comparing the results at 10s and 1200s, a slight increment of conduction loss can be observed which can be explained by the positive correlation between $R_{DS(on)}$ and T_j. The average error is below 10% for various operating conditions which verifies the accuracy of the proposed model.

TABLE III CONDUCTION POWER LOSS RESULTS OF PFC APPLICATION

Condition	Case 1		Case 2		Case 3	
Time	10s	1200s	10s	1200s	10s	1200s
Measured	2.24W	3.12W	1.93W	2.61W	1.42W	1.94W
Simulated	2.41W	3.39W	2.01W	2.78W	1.51W	2.09W
Error	7.59%	8.65%	4.14%	6.51%	6.33%	7.73%

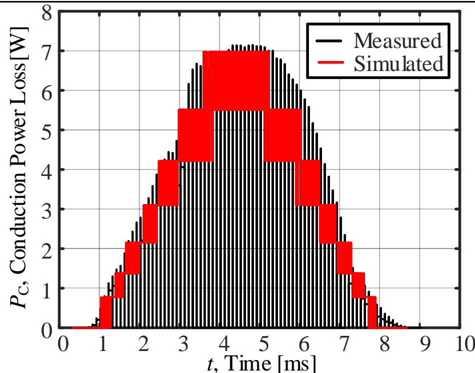
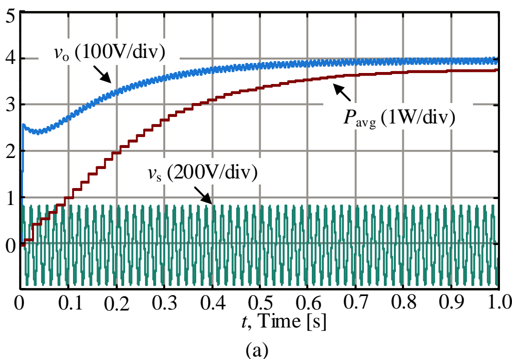
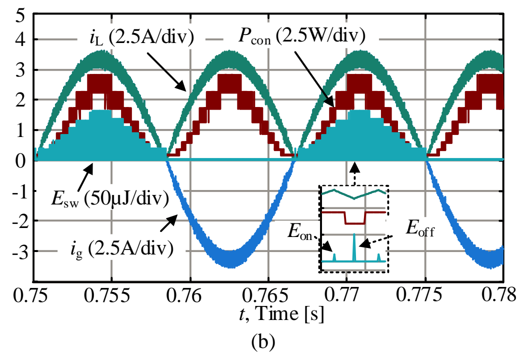


Fig. 15 Conduction power results of PFC at 10s for Case 1.



(a)



(b)

Fig. 16 Simulation results of PFC circuit for Case 1, (a) Overall system performance, and (b) Detailed power loss waveforms.

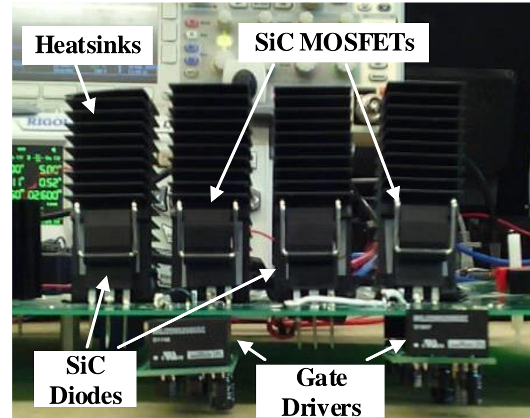


Fig. 17 PFC converter setup.

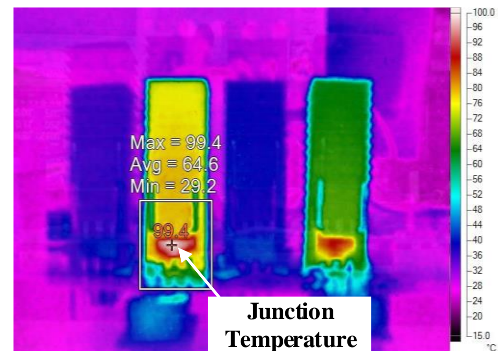


Fig. 18 Thermal image of SiC MOSFETs in PFC circuit.

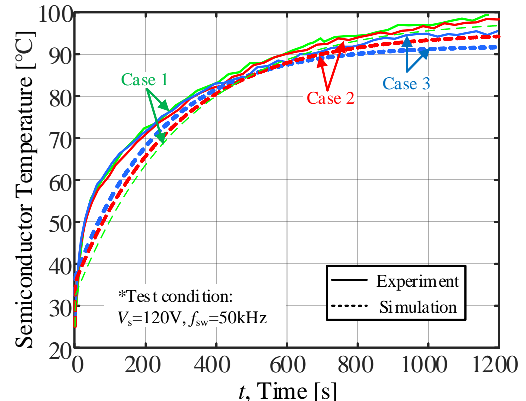


Fig. 19 Transient temperature estimation of SiC MOSFET in PFC circuit.

Also, the simulated results of overall system performance, as well as detailed power loss estimation, are demonstrated in Fig. 16. Note that the computed average power losses of SiC

MOSFET in one switching cycle (P_{avg}) rises to steady state in accordance with v_o. Moreover, the detailed losses breakdown of the device including conduction, turn-on, and turn-off losses can also be predicted during each operation cycle and updated based on the instantaneous operating conditions. Since all the power loss data are pre-obtained from the power loss LUT of the device simulation, the accuracy of the power losses within the available operating range can be promised. It should be mentioned that this additional loss information will not affect the electrical circuit simulation.

2) Thermal performance - To evaluate the thermal performance of the semiconductor, the dynamic thermal network is implemented in PSCAD for electro-thermal simulation of PFC application. As shown in Fig. 17, each switching device is attached to the heatsink individually by the thermal pad and the transient junction temperature of SiC MOSFET which is usually the hottest spot is monitored by the thermal imager. Fig. 18 gives the thermal image of the semiconductor devices in the PFC converter at 20 minutes (1200s) running time for Case 1. It can be seen that SiC MOSFETs have much higher junction temperature up to 100 ℃ than the SiC SBD which means the losses of high switching frequency devices are more significant and thus are of particular concern for device selection and thermal management.

Furthermore, the transient junction temperature of SiC MOSFET in the PFC converter is also simulated in PSCAD and compared with the experimental results in Fig. 19. It can be observed that the temperature for various cases increases gradually from the same ambient temperature (25ºC) and reach different steady-state values at 1200s due to the power loss difference. In addition, the simulated results are generally in good agreement with the experimental results for various cases which verifies the accuracy of the proposed method. The average error at 1200s is within 5% and the simulated thermal trajectories slightly deviate from the experimental results. The reasons can be the underestimation of thermal capacitance as well as the power losses in the low current range.

C. Discussion

1) Applicability - The proposed model is applicable to an EMTP simulator with programmable functions for device simulation under various operating conditions. In addition, the proposed model can be used to estimate the losses of the four types of commutation units in Fig. 1. Further modifications are needed when it extends for other semiconductor devices, such as Si IGBT and Gallium nitride (GaN) transistor. The switching behavior of the BJT and tail current effect in IGBT as well as the reverse conducting characteristic of GaN should be considered respectively. However, the parameter extraction and simulation strategy are still applicable. Besides, the power loss database used in the PE systems simulation can come from the device simulation using the proposed model, other device simulators (e.g. SPICE-like software), or measurements.

2) Efficiency - In general, there is always a tradeoff between accuracy and speed. A reasonable accuracy of power loss estimation requires a complex device model considering lots of parasitic elements and thermal effects with a relatively small simulation time step (e.g. 1ns). However, with such a small time step, it is difficult for the PE systems simulation to run until the steady-state resulting from the out-of-memory issue or time-consuming problems. To evaluate the efficiency of the proposed method, a simulation comparison of different methods is conducted for the PFC converter as illustrated in Table III. As noticed, the simulation in LTspice using device model from manufacturer is running at 1ns time step instead of 1µs due to the convergence problem. As a result, it is capable of obtaining accurate loss information by sacrificing much more time for simulating only 100 ms in comparison with the same simulation in PSCAD using the proposed method and simple-switch model. Since the simple-switch model only uses two-state resistance to represent the switching device, the average power losses thus are much lower than the other two methods due to the missing part of switching loss. Concretely, by using the proposed method in PSCAD, both fast simulation speed and acceptable accuracy of power estimation can be achieved with additional transient temperature information.

TABLE III SIMULATION COMPARISON OF PFC APPLICATION

Quad 3.60GHz Intel Core i7-4790, RAM(8GB)		Case1		Case 2		Case3	
Simulator	Time step	Time (s)	P_{avg} (W)	Time (s)	P_{avg} (W)	Time (s)	P_{avg} (W)
Simple-switch in PSCAD	1µs	10.6	2.37	10.3	1.96	10.8	1.48
Proposed method in PSCAD	1µs	11.2	3.82	10.9	3.66	11.4	3.36
Device model in LTspice	1ns	12866	3.93	12466	3.71	13191	3.67

V. CONCLUSION

In this paper, an electromagnetic transient simulation methodology for power loss and junction temperature estimation of SiC MOSFET in PE applications is designed, implemented in PSCAD/EMTDC, and validated by experiments. In device simulation, a behavioral transient model of SiC MOSFET is developed to generate the device power loss table. This model provides insight into the impacts of parasitics and the interaction between the diode and SiC MOSFET in the switching process. In addition, the parameter extraction from the datasheet is also investigated in detail. The switching waveforms and power losses results in device simulation are consistent with the DPT test results (the average error is around 10%). Furthermore, the bridgeless PFC system simulation is carried out using a simple-switch model along with power loss LUT and the dynamic thermal model. Eventually, the instantaneous average power losses of SiC MOSFET as well as the switching losses and conduction losses for each switching cycle can be predicted. Moreover, the simulation results of the transient junction temperature are in good agreement with measurements in a wide range of operating conditions. In comparison with various models and simulators, the proposed approach shows better reproducibility of the transient power losses indicating its advantage of fast simulation speed as the simple-switch model and comparable accuracy with device model from the manufacturer.

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