

# System Modeling and Stability Analysis of Single-Phase Transformerless UPQC Integrated Input Grid Voltage Regulation

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**Abstract**—This paper extends the conventional features of a transformerless unified power quality conditioner (TL-UPQC). An enhanced control methodology is presented to allow exchanging reactive power between the system and the grid to provide input grid voltage regulation. Therefore, both load side and input grid side voltages are regulated with one converter. In this regard, a phase angle is created between the input current and the input voltage. Thereby, the system behavior as a capacitive or an inductive reactance is controlled. An additional ac voltage control loop has been designed. The inner current loop has been reformed to receive reference information from two outer voltage loops. The enhanced control strategy takes action based on local information collected by the TL-UPQC with no requirements of additional sensor circuits. Since the conventional functions of the TL-UPQC system have been extended, aspects related to system modeling and control design should be developed. Small-signal model that characterize the dynamics of the power stage and the controller are presented. Design guidelines considering grid impedance to achieve a desired performance are developed. A 500VA / 120V, 60 Hz prototype has been built to verify the models and the overall system performance. Steady-state and transient experimental results are presented and discussed.

**Index Terms**— Grid impedance, modeling, power quality, reactive power compensation, transformerless, UPQC, voltage control, voltage regulation.

## I. INTRODUCTION

HIGH penetration of small-scale distributed energy resources (DER) is now connected to low voltage (LV) distribution ac networks. For example, a photovoltaic (PV) system offers a reliable and a clean source of energy that becomes a popular choice to meet the increasing load demand. Large-scale wind power plants are widely adopted in electric power transmission, while small-scale wind farms are integrated with ac microgrids. However, the intermittent nature of renewable energy sources conveys many challenges to the power quality of the utility grid. A sudden voltage rise might occur due to reverse power flow at peak PV generation [1], [2]. The stochastic nature of wind active and reactive power results into power quality problems by exceeding voltage flickering levels [3]. Voltage variation in the network is a critical issue that causes system shutdown, loss of data, high losses, overheating of equipment and reduced lifetime.

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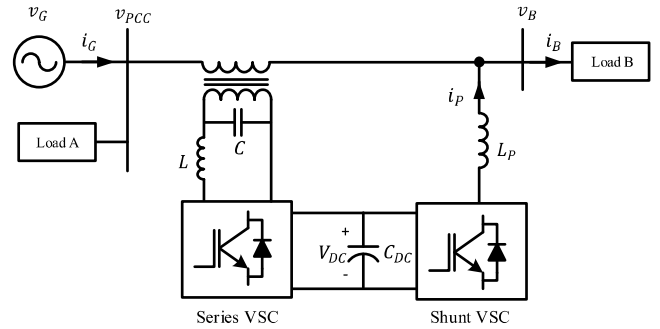


Fig. 1. Conventional UPQC topology.

Considerable work has been reported in the literature adopting the recent advancements of semiconductor technology to provide grid voltage support. A centralized distribution static synchronous compensator (D-STATCOM) that is connected to medium voltage (MV) distribution networks is widely employed to provide line voltage regulation due to its large dynamic range [4]-[6]. In [7], the behavior of a D-STATCOM as a controlled voltage source has been adopted to implement a generalized impedance control. Generally, a D-STATCOM can support the grid voltage by means of controlling the reactive power injection into the power system. However, installing a high rating D-STATCOM at MV lacks the capability of identifying local problems happening at the LV side and cannot guarantee a stable voltage profile for long distance loads. Since massive number of DER units are being installed at the residential or commercial side, power quality improvement techniques should be installed adjacent to these points. This will allow more units to join grid operation without affecting the upstream voltage.

A unified power quality conditioner (UPQC) is an effective solution since it can perform both series and parallel compensation in LV distribution networks. A conventional topology of a UPQC system is shown in Fig. 1. It consists of two voltage source converters (VSCs) and is mainly connected between the ac supply and critical nonlinear loads. In a UPQC system, the shunt converter injects current into the grid to compensate for load current harmonics and reactive power consumption. On the other hand, the series converter injects voltage to mitigate voltage disturbances propagating in the network, such as flickering, voltage swells and voltage sags. The work reported in the literature mainly focused on developing control strategies to improve the conventional features of a UPQC system including active power control and minimum active power injection control [8]-[11]. In the latter,

the injected voltage is controlled at an appropriate angle based on operational requirements. In other words, active reactive power control technique where the series converter delivers complex power can be achieved. Hence, the series converter shares load reactive power with the shunt converter under steady-state and transient conditions. This will enlarge the reactive power compensation range of the system, and optimum sizing can be realized. In [12], a data-driven based control methodology implementing adjustable phase angle for optimal operating point has been proposed. A conventional UPQC topology requires a series transformer to reduce the voltage stress of the converter as indicated in Fig. 1. Nevertheless, transformers are bulky, increase cost and limit the power density of the converter. In addition, achieving a fast-dynamic response at the output voltage can be challenging [13]. The structure of a single-phase UPQC system can be a full-bridge, a three-leg, or a half-bridge topology [8]. A single-phase transformerless full-bridge UPQC topology has been proposed in [14], [15], where circulating current has been addressed. Adopting full-bridge topology requires a high number of switches which leads to high losses and low efficiency. A single-phase three-leg transformerless UPQC topology requires six switches; therefore, it can attain higher efficiency and power density [16], [17]. However, the shared leg introduces leakage current into the system and decoupling the operation between the series and parallel converters becomes essential. In general, most proposed conventional TL-UPQC topologies are able to provide a stable and sinusoidal voltage across loads connected to its output terminal, e.g. load B in Fig. 1. Nonetheless, loads that are connected to the input grid voltage directly are still exposed to voltage variations in the network, e.g. load A in Fig. 1. Thereby, an additional compensator is still required to be installed at the point of common coupling (PCC). A three-phase improved topology of UPQC (iUPQC) that includes the functionality of reactive power injection for input grid voltage regulation has been proposed in [18] where instantaneous reactive power theory (P-Q) control methodology has been adopted. This control methodology requires an extra current sensor at the load side. It is worth mentioning that system modeling for stability studies of a UPQC system to provide input grid voltage regulation in addition to output voltage regulation has not been developed yet in the literature. Also, the effect of the grid impedance has not been considered in the design process.

A transformerless UPQC (TL-UPQC) system adopting half-bridge topology has been proposed in [13], [19], [20]. The system proved to successfully support critical loads against long and short duration voltage variations with fast dynamic response. It is important to highlight that only the load side voltage power quality issues have been mitigated while input grid voltage regulation has not been introduced or studied for the TL-UPQC system yet. This paper extends the features of the TL-UPQC system offered in [13], [19], [20]. The paper presents an enhanced control strategy to expand the functions of a TL-UPQC system to include input grid voltage regulation. The TL-UPQC will be able to support loads that are connected to the grid side voltage besides its ability to support critical loads that are connected to the load side voltage, i.e. sustain the voltage across critical loads and general loads at the same time as

depicted in Fig. 2. A comparison between reported TL-UPQC topologies in the literature is provided in Table I. The work in this paper presents a comprehensive study implementing three control loops and their coordination. Theoretical analysis considering the grid impedance, mathematical models and stability analysis for the proposed comprehensive system are presented with experimental justifications. Controller design guidelines for the proposed system to achieve a specific performance is provided as well.

## II. SYSTEM DESCRIPTION AND OPERATION

Fig. 2 shows the detailed structure of a single-phase TL-UPQC connected to the PCC at a LV distribution network. The TL-UPQC consists of two half-bridge bi-directional VSCs. The topology is formed by one shunt converter and one series converter. Both converters share a common dc link. A shunt filter capacitor  $C_f$  is added to the system to act as a low impedance for the high frequency components introduced by the converter. This will minimize the switching harmonics injected by the shunt converter into the grid. The TL-UPQC topology offers the following features,

- a) Transformerless – no transformer in between the VSC and the grid. It leads high efficiency and cost effective.
  - b) Low common-mode (CM) voltage – since the transformer is absent, CM voltage and leakage current become significant. The topology can maintain low CM voltage since the potential difference between the ac and dc grounds is clamped [21].
  - c) Mitigates harmonics of nonlinear loads and provides reactive power to linear loads connected to the load bus.
  - d) Protects critical loads against voltage flickering, and voltage disturbances with fast dynamic response.
  - e) Allows amplitude voltage variation control to achieve energy saving at the load bus [22].
- While, TL-UPQC is intended to be installed at a LV distribution network, its functions can be maximized to include the following,
- f) Provides reactive power compensation to achieve input grid voltage regulation to the loads connected to the PCC.
  - g) Improves the PCC voltage profile and eventually improve the voltage quality of the upstream voltage.
  - h) Eliminates the need to install a D-STATCOM at the PCC and copes with the new distributed nature of a microgrid grid to mitigate power quality issues elevated at LV distribution networks.
  - i) Relies on means of locally collected information and does not require additional sensors.

To illustrate the operation of the TL-UPQC, Fig. 3 shows the equivalent circuit of the system which consists of a controlled current-source to model the shunt converter and a controlled voltage-source to model the series converter. In a typical TL-UPQC system, the shunt converter injects current harmonics and reactive current  $i_p$  to compensate the distorted current of the nonlinear load  $i_B$  connected to bus B. This will shape the input current  $i_{PCC}$  to be sinusoidal and in-phase with the PCC voltage. The grid current  $i_G(t)$  will carry the apparent power demand of the PCC load that is quantified by the PCC load current  $i_A(t)$ . It will also carry the active power demand

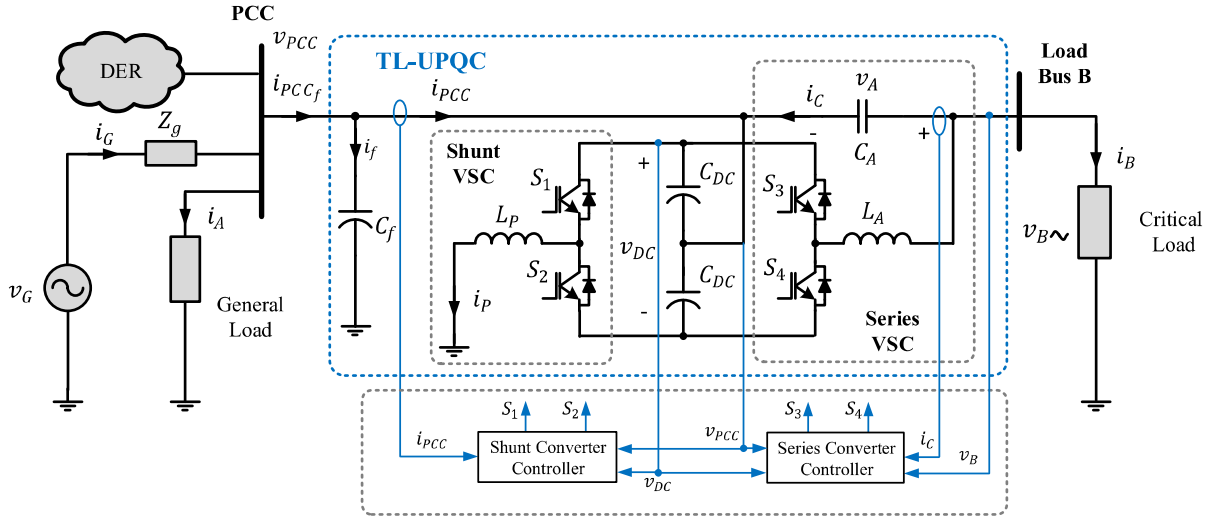


Fig. 2. TL-UPQC topology for low voltage distribution network.

TABLE I  
COMPARISON BETWEEN SINGLE-PHASE TL-UPQC TOPOLOGIES

Topology	Number of Switches	Number of Sensors	Voltage stress across switches	Isolation	Current Quality	Output Voltage Profile	Input Grid Voltage Profile
Full-bridge [14], [15]	8	5	Low	Not required	Improved	Improved	Low
Three-leg [16], [17]	6	5	Low	Not required	Improved	Improved	Low
Half-bridge [13], [19], [20]	4	5	High	Not required	Improved	Improved	Low
Proposed solution	4	5	High	Not required	Improved	Improved	Improved

consumed by the load connected to the load bus in addition to the necessary active power required to maintain the dc link voltage and compensate for converter losses. The enhanced control methodology proposed in this paper contains an additional control degree of freedom. If reactive power compensation is needed at the grid side, a phase angle  $\theta$  is created between  $v_{PCC}$  &  $i_{PCC}$  as depicted in Fig. 3. The active and reactive power at the PCC can be expressed as follows,

$$P_{PCC} = V_{PCC} I_{PCC} \cos \theta \quad \& \quad Q_{PCC} = V_{PCC} I_{PCC} \sin \theta \quad (1)$$

where  $V_{PCC}$  is the steady-state rms value of the PCC voltage,  $I_{PCC}$  is the steady-state rms value of the feeder current, and  $\theta$  is the PCC current displacement angle with respect to its voltage.

By controlling the phase angle  $\theta$ , the TL-UPQC will be able to operate in three reactive power compensation modes. The phasor diagrams shown in Fig. 4 illustrate the operation of the three modes: a) power factor correction (PFC) mode in which no reactive power compensation is needed at the grid side, b) capacitive mode in which reactive power is being injected to the grid and c) inductive mode in which reactive power is being absorbed from the grid.  $I'_{PCC}$ ,  $I'_G$  and  $V'_{PCC}$  represent the steady-state values before enabling grid reactive power compensation.

#### A. Power Flow Analysis

Fig. 5 shows a block diagram of the power flow in a TL-UPQC system. The amount of grid active and reactive power transferred from the grid to the PCC bus can be expressed by,

$$P_G = \frac{V_G V_{PCC}}{Z_g} \cos(-\delta + \phi_g) - \frac{V_{PCC}^2}{Z_g} \cos(\phi_g) \quad (2)$$

$$Q_G = \frac{V_G V_{PCC}}{Z_g} \sin(-\delta + \phi_g) - \frac{V_{PCC}^2}{Z_g} \sin(\phi_g) \quad (3)$$

where  $Z_g$  represents the grid impedance with a displacement angle of  $\phi_g$ .

A linear load represents the load connected to the PCC. The load active and reactive power are given as follows,

$$P_A = \frac{V_{PCC}^2}{Z_A} \cos(\phi_A) \quad \& \quad Q_A = \frac{V_{PCC}^2}{Z_A} \sin(\phi_A) \quad (4)$$

where  $Z_A$  is the load impedance connected to the PCC with a displacement angle of  $\phi_A$ .

The nonlinear load connected to the TL-UPQC system in this study is chosen to be dimmable LED lamps, due to their extreme sensitivity to voltage flickering and their nonlinear characteristics [23]. The TL-UPQC system will compensate for the load harmonics, the LED lamps is assumed to be seen as a resistive load from the grid point of view. The amount of active power consumed by this critical load is given by,

$$P_B = \frac{V_B^2}{R_B} \quad (5)$$

where,  $R_B$  is the equivalent fictitious resistance of the LEDs and  $V_B$  is the output rms voltage maintained by the TL-UPQC system across the load bus.

The power going through the shunt converter  $P_1$ , assuming no losses in the converter, is used to charge up the dc link capacitor and maintain the dc link voltage by compensating for the power needed by the series converter  $P_2$ . The indicator is the dc link voltage reached steady-state, in other words, a constant value. At system equilibrium, the input power  $P_{PCC}(t)$  equals the output power  $P_B(t)$ . From which, the following equation can be found,

$$\frac{V_G V_{PCC}}{Z_g} \cos(-\delta + \phi_g) - \frac{V_{PCC}^2}{Z_g} \cos(\phi_g) = \frac{V_B^2}{R_B} + \frac{V_{PCC}^2}{Z_A} \cos(\phi_A) \quad (6)$$

Consequently, the power angle  $\delta$  can be obtained. The TL-UPQC system regulates the PCC voltage by injecting/absorbing reactive power  $Q_{PCC}(t)$  into/from the grid. Thus, the amount of reactive power needed by the TL-UPQC system to accomplish voltage regulation can be found using the following equation,

$$Q_{PCC}(t) = \frac{V_G V_{PCC}}{Z_g} \sin(-\delta + \phi_g) - \frac{V_{PCC}^2}{Z_g} \sin(\phi_g) - \frac{V_{PCC}^2}{Z_A} \sin(\phi_A) \quad (7)$$

### B. Enhanced Controller Strategy and Implementation

#### Shunt Converter Enhanced Control Methodology

Fig. 6 shows the shunt converter circuit of the TL-UPQC that is responsible of regulating the input grid voltage under the proposed enhanced control methodology. A current source is connected to the dc link voltage to model the power required by the series converter to maintain the output voltage. The shunt converter's control block diagram is depicted in Fig. 7, which involves three controllers. Two voltage control loops and one current control loop can be described as follows,

- 1) Dc link voltage controller – maintains the dc link voltage between the two VSCs.
- 2) Ac voltage controller – provides input voltage regulation to the PCC bus through means of reactive power injection.
- 3) Input current controller – shapes the PCC current to operate in three modes (PFC, capacitive and inductive mode).

If neglecting the load current  $i_B$  in Fig. 6 the system is a simple PFC when no reactive power support is required. This is the default operating mode of the TL-UPQC system. In order to provide input grid voltage support, the system will operate in either the inductive or the capacitive mode, hence controlling the phase angle  $\theta$  of the PCC current. The phase angle  $\theta$  is governed by the amount of reactive power needed to regulate the PCC voltage. It will also take role to define the absorption of active power. So that the system is decoupled,  $i_{PCC}(t)$  is converted into the d-q axis,

$$I_D = I_{PCC} \cos \theta \quad \& \quad I_Q = I_{PCC} \sin \theta \quad (8)$$

where,

$$I_{PCC} = \sqrt{I_D^2 + I_Q^2} \quad (9)$$

$I_{PCC}$  represents the steady state rms values of the PCC current, while  $I_D$  and  $I_Q$  represent the direct and quadrature components of the PCC current respectively.

The dc voltage control loop is a PI controller, which is used to fix the dc link voltage and determine the direct component of the injected current. The ac voltage control loop is also a PI

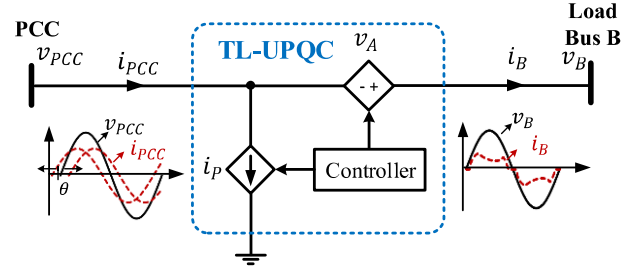


Fig. 3. Equivalent circuit model of a TL-UPQC system.

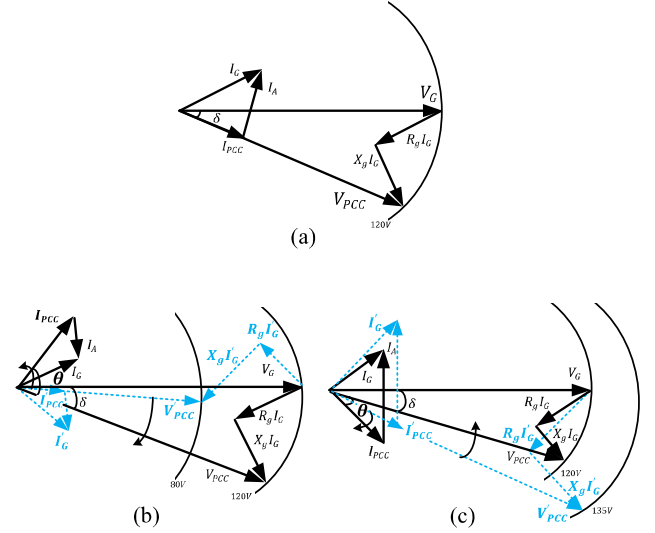


Fig. 4. Phasor diagrams of (a) PFC mode (b) capacitive mode (c) inductive mode.

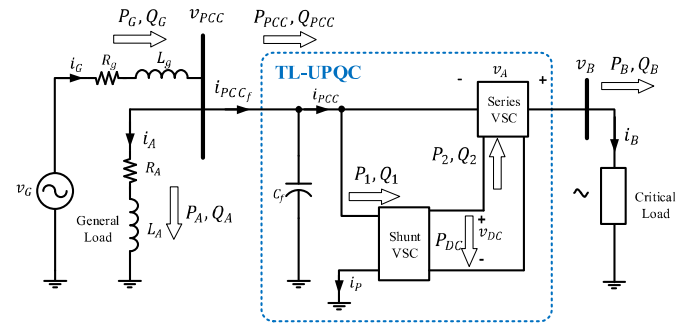


Fig. 5. A block diagram of power flow in a TL-UPQC system.

controller that is used to regulate the PCC voltage and generate the quadrature component of the PCC current.

The inner current control loop is a hysteresis controller that shapes the shunt inductor current by comparing it to its reference signal. Since the shunt converter circuit is connected in parallel to the source and considering the load current to be constant, the PCC current ripple is the same as the inductor current ripple. Therefore, a reference signal for the PCC current can be formed with specified upper and lower bands to guide the inductor current following the reference. The reference current signal is generated by the two outer voltage loops and phase locked loop (PLL) as follows,

$$i_{PCC}^*(t) = i_D^*(t) + i_Q^*(t) \quad (10)$$

Since the generated reference current is a sinusoidal and following the PCC voltage, harmonics mitigation can be achieved. The switching criteria of the shunt converter semiconductor switches can be written as follows,

$$i_{PCC}(t) \leq i_{PCC}^*(t) - \frac{\Delta I_{PCC}}{2} \quad (11)$$

$$i_{PCC}(t) \geq i_{PCC}^*(t) + \frac{\Delta I_{PCC}}{2} \quad (12)$$

where  $\Delta I_{PCC}$  is the inductor current hysteresis ripple band, and  $i_{PCC}^*(t)$  is the reference PCC current.

#### Series Converter Control Methodology

Fig. 8 shows the half-bridge configuration of the series converter circuit of the TL-UPQC. One controller is formalized in the series converter which represents the fourth controller in the system as follows,

4) Load bus voltage controller – maintains the output voltage to be sinusoidal and constant amplitude.

The controller strategy adopted for the load bus voltage controller is boundary control with second order switching surface. In boundary control, the switching trajectory is used to predict the moves of voltages and currents of passive components. These predictions ensure a very fast dynamic response to any external disturbance. Fig. 9 indicates the switching trajectories of the series converter system for a resistive load on the state plane ( $v_A - i_L$ ), which have been obtained solving the state-space equations of the system. The solid lines represent the on-state trajectory, while the dotted lines represent the off-state trajectory. The figure shows that the system operating points are realized following the switching trajectories with a defined reference voltage band. The switching criteria of  $S_3$  and  $S_4$  is governed by,

$$v_B(t) - v_{B,min} - \left[ \frac{k_A}{\frac{v_{DC}}{2} - v_B + v_{PCC}} \right] i_C^2(t) \leq 0 \quad (13)$$

$$\& i_C(t) \leq 0 \quad (14)$$

$$v_B(t) - v_{B,max} + \left[ \frac{k_A}{\frac{v_{DC}}{2} + v_B - v_{PCC}} \right] i_C^2(t) \geq 0 \quad (15)$$

$$\& i_C(t) \geq 0 \quad (16)$$

$k_A$  represents a constant value and is calculated as follows,

$$k_A = \frac{L_A}{2C_A} \quad (17)$$

$v_{B,min}$  and  $v_{B,max}$  are minimum boundary and maximum boundary of reference signal, respectively.

The detailed derivation of (13)-(17) and control structure are given in [13], [24].

### III. SYSTEM MODELING

For a better insight of the system's dynamic behaviors, small-signal models are determined [25]. The state-space model of the converter can be found by determining circuit equations of the converter. The state variables are basically energy storage elements of the system. For each switching interval, the system can be described by a set of linear time invariant equations,

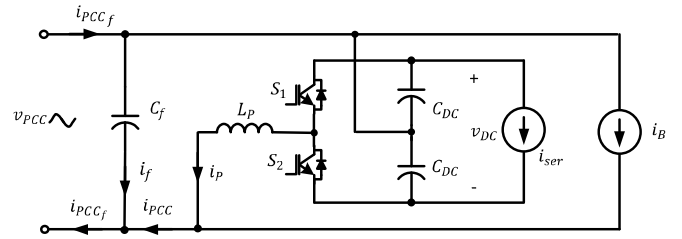


Fig. 6. Half-bridge inverter configuration of the shunt converter.

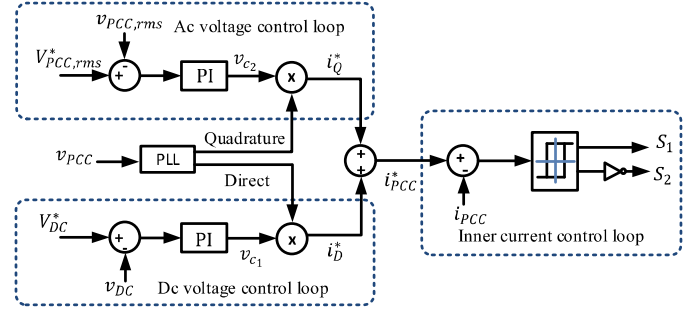


Fig. 7. Shunt converter control block diagram.

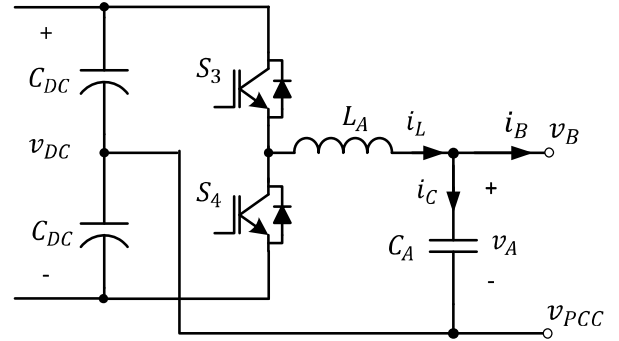


Fig. 8. Half-bridge inverter configuration of the series converter.

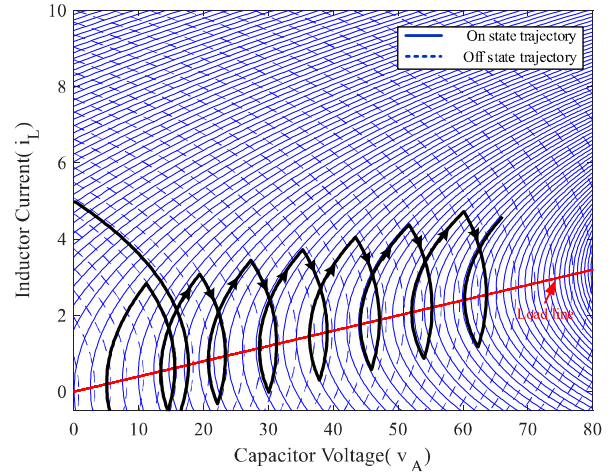


Fig. 9. Switching trajectories of the series converter.

$$\text{Let } x(t) = \begin{bmatrix} v_{PCC}(t) \\ i_{PCC}(t) \\ v_{DC}(t) \\ i_A(t) \\ i_G(t) \end{bmatrix}, u(t) = v_G(t), y(t) = \begin{bmatrix} v_{PCC}(t) \\ v_{DC}(t) \end{bmatrix} \quad (18)$$

$$x = \begin{bmatrix} 0 & -\frac{1}{C_f} & 0 & -\frac{1}{C_f} & \frac{1}{C_f} \\ \frac{1}{L_P} & 0 & \frac{1-2q(t)}{2L_P} & 0 & 0 \\ 0 & \frac{2q(t)-1}{C_{DC}} & 0 & 0 & 0 \\ \frac{1}{L_A} & 0 & 0 & -\frac{R_A}{L_A} & 0 \\ -\frac{1}{L_g} & 0 & 0 & 0 & -\frac{R_g}{L_g} \end{bmatrix} x + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \frac{1}{L_g} \end{bmatrix} u \quad (19)$$

$$y = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{bmatrix} x \quad (20)$$

The state-space matrices are derived using circuit analysis and circuit equations, where  $q(t)$  is the switching function. An assumption has been made that the current control loop is fast enough and will not dynamically affect the voltage control loops. Therefore, the perturbation in duty cycle can be neglected. By introducing small perturbation, the transfer functions of the power stages can be obtained,

$$T_{ac}(s) = \frac{\tilde{v}_{pcc}(s)}{\tilde{i}_{pcc}(s)} = \frac{-(s+\frac{R_g}{L_g})(s+\frac{R_A}{L_A})}{sC_f(s+\frac{R_g}{L_g})(s+\frac{R_A}{L_A})+\frac{1}{L_g}(s+\frac{R_A}{L_A})+\frac{1}{L_A}(s+\frac{R_g}{L_g})} \quad (21)$$

$$T_{dc}(s) = \frac{\tilde{v}_{dc}(s)}{\tilde{i}_{pcc}(s)} = \frac{2V_{PCC}}{sC_{DC}V_{DC}} \quad (22)$$

The PCC current  $i_{pcc}(t)$  is the same shape as its reference signal with a current sensor gain  $K_{Ti}$  as follows,

$$\tilde{i}_{pcc} = \frac{\tilde{i}_{pcc}^*}{K_{Ti}} \quad (23)$$

The PCC current reference signal is generated by adding the two output of the compensators multiplied by the PLL output with a gain of  $K_{PLL}$ , if only rms values are considered,

$$i_{pcc}^*(t) = K_{PLL}(v_{c_1}(t) \sin \omega t + v_{c_2}(t) \cos \omega t) \quad (24)$$

Introducing perturbations to  $i_{pcc}^*$ ,  $v_{c_1}$  and  $v_{c_2}$  and taking Laplace transformation, the following relation can be found,

$$\tilde{i}_{pcc}(s) = \frac{K_{PLL} \cos \theta}{\sqrt{2}K_{Ti}} \tilde{v}_{c_1} + \frac{K_{PLL} \sin \theta}{\sqrt{2}K_{Ti}} \tilde{v}_{c_2} \quad (25)$$

Fig. 10 shows the small-signal model block diagram of the dc voltage loop in a TL-UPQC system. To study the dc voltage loop separately,  $\tilde{v}_{c_2}$  is assumed to be zero, thus the transfer functions of the inner loop  $T_{in}(s)$  and the process  $T_d(s)$  are,

$$T_{in}(s) = \frac{\tilde{i}_{pcc}(s)}{\tilde{v}_{c_1}} \Big|_{\tilde{v}_{c_2}=0} = \frac{K_{PLL} \cos \theta}{\sqrt{2}K_{Ti}} \quad (26)$$

$$T_d(s) = T_{in}(s) \cdot T_{dc}(s) = \frac{K_{PLL} \cos \theta}{\sqrt{2}K_{Ti}} \cdot \frac{2V_{PCC}}{C_{DC}V_{DC}} \cdot \frac{1}{s} \quad (27)$$

A PI controller is applied to control the overall process, which has the following transfer function,

$$T_{C_1}(s) = \frac{\tilde{v}_{c_1}(s)}{\tilde{v}_{dc}(s)} = K_{Tdc} \left( K_{P_1} + \frac{K_{I_1}}{s} \right) \quad (28)$$

where  $K_{Tdc}$  is the sensor gain of the dc link voltage.

The frequency response of the overall open loop system can be found by combining the process and controller transfer functions,

$$T_{OLd}(s) = T_{C_1}(s) \cdot T_d(s) = \frac{2K_{Tdc}K_{PLL}V_{PCC} \cos \theta (K_{P_1}s + K_{I_1})}{\sqrt{2}K_{Ti}C_{DC}V_{DC}s^2} \quad (29)$$

Now, to study the ac voltage loop separately,  $\tilde{v}_{c_1}$  is assumed to be zero as shown in Fig. 11,

$$T_{in}(s) = \frac{\tilde{i}_{pcc}(s)}{\tilde{v}_{c_2}} \Big|_{\tilde{v}_{c_1}=0} = \frac{K_{PLL} \sin \theta}{\sqrt{2}K_{Ti}} \quad (30)$$

$$T_q(s) = \frac{K_{PLL} \sin \theta}{\sqrt{2}K_{Ti}} \frac{-(s+\frac{R_g}{L_g})(s+\frac{R_A}{L_A})}{sC_f(s+\frac{R_g}{L_g})(s+\frac{R_A}{L_A})+\frac{1}{L_g}(s+\frac{R_A}{L_A})+\frac{1}{L_A}(s+\frac{R_g}{L_g})} \quad (31)$$

Since the open loop gain of the system is negative, the PI controller is designed to include a negative component, so the overall gain of the system is positive.

$$T_{C_2}(s) = \frac{\tilde{v}_{c_2}(s)}{\tilde{v}_{dc}(s)} = -K_{Tpcc} \left( K_{P_2} + \frac{K_{I_2}}{s} \right) \quad (32)$$

where  $K_{Tpcc}$  is the sensor gain of the PCC voltage.

Now, the transfer function of the overall loop gain of the system is expressed by,

$$T_{OLq}(s) = \frac{K_{Tpcc}K_{PLL} \sin \theta (K_{P_2}s + K_{I_2})}{\sqrt{2}K_{Ti}s} \times \left[ \frac{(s+\frac{R_g}{L_g})(s+\frac{R_A}{L_A})}{sC_f(s+\frac{R_g}{L_g})(s+\frac{R_A}{L_A})+\frac{1}{L_g}(s+\frac{R_A}{L_A})+\frac{1}{L_A}(s+\frac{R_g}{L_g})} \right] \quad (33)$$

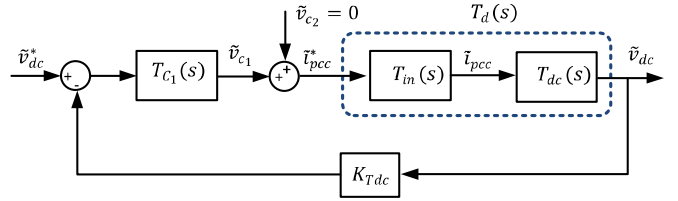


Fig. 10. Small-signal block diagram of the dc voltage loop.

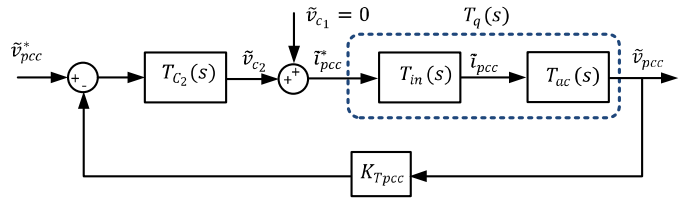


Fig. 11. Small-signal block diagram of the ac voltage loop.

#### IV. SYSTEM STABILITY AND CONTROLLER DESIGN

The parameters used for this study are tabulated in Table II. Two criteria have been considered while designing the PI parameters. The first criterion is the limitation of the controller's bandwidth, while the second criterion is that the phase margin of the overall system should be sufficient enough to provide control system stability. The dc voltage loop establishes the reference component in which the dc link capacitor charges. The output voltage ripple across the dc link can be expressed as,

$$\Delta v_{dc}(t) = \frac{V_{PCC}}{2\pi f C_{DC} V_{DC}} [-I_{PCC} \sin(2\omega t - 2\delta \pm \theta) + I_B \sin(2\omega t - 2\delta - \phi_B)] \quad (34)$$

where  $f$  is the line frequency and  $I_B$  is the steady-state rms value of the load current connected to bus B with a displacement angle of  $\phi_B$ .

It can be observed from (34) that the dc link voltage ripple contains 2<sup>nd</sup> order harmonic components. Therefore, the parameters selection of the PI controller  $T_{C_1}$  should be selected to have an overall dc voltage loop bandwidth of approximately one-tenth the double line frequency. Based on (27), the frequency response of the dc voltage loop  $T_d(s)$  before adding the controller under different operating conditions is highlighted in Fig. 12. The figure indicates a cross over frequency range of  $\omega_{co_1}$ : 672.3 – 2714.3 rad/sec, which is clearly much higher than the double line frequency.

By defining  $\omega'_{co_1}$  as the frequency at which the magnitude of the overall open loop system including the controller  $T_{OLd}(s)$  is zero dB,

$$|T_{OLd}(j\omega'_{co_1})| = 1 \quad (35)$$

Then, the selection of  $K_{P_1}$  and  $K_{I_1}$  should satisfy the following criteria,

$$\frac{2K_{Tdc}K_{PLL}V_{PCC} \cos \theta \sqrt{[K_{P_1}^2 \omega_{co_1}^2 + K_{I_1}^2]}}{\sqrt{2} K_{T_i} C_{DC} V_{DC} \omega_{co_1}^2} = 1 \quad (36)$$

and,

$$\omega'_{co_1} \leq 0.1 * 4\pi f \quad (37)$$

Since the controller encloses adding a pole at the origin to the overall system, the system is subjected to a phase lag causing a drop in the available phase margin. Consequently, the PI parameters should be selected to provide a sufficient phase margin to the overall system as follows,

$$PM'_1 = 180 + \angle T_d(j\omega'_{co_1}) - \tan^{-1} \frac{K_{I_1}}{\omega'_{co_1} K_{P_1}} \geq 45^\circ \quad (38)$$

where,  $PM'_1$  is the phase margin of the overall dc voltage loop open-loop transfer function at the frequency  $\omega'_{co_1}$ .

Satisfying (36) to (38), the PI parameter have been chosen to shift the cross over frequency to 13.6 rad/sec maximum at light loads with a minimum phase margin of 74° at heavy loads as shown in Fig. 13. Light loads indicate that the injected reactive power from the TL-UPQC system to the grid is minimum. It can be concluded that the mathematical model of the dc voltage loop appears to provide a stable operation under different operating points.

The PI parameters of the ac voltage loop  $T_{C_2}$  are selected to provide a slower dynamic response than the dc voltage control loop. To avoid any possible interference between the two loops, the bandwidth of the ac voltage loop is designed to be at least ten times slower than the dc voltage loop. It is clear from equation (33) that the load connected to the PCC point constitutes the ac voltage control loop. This is true since PCC voltage fluctuation in a weak grid is dramatically affected by whether the load is light or heavy. In addition, the Thévenin impedance of the connected ac system governs the variation of the PCC system. Based on (31) and (32), the controller parameters  $K_{P_2}$  and  $K_{I_2}$  are selected to satisfy the following criteria,

$$K_{T_{PCC}} \times \frac{\sqrt{K_{P_2}^2 \omega_{co_2}^2 + K_{I_2}^2}}{\omega'_{co_2}} \times |T_q(j\omega'_{co_2})| = 1 \quad (39)$$

and,  $\omega'_{co_2} \leq 0.1 * \omega'_{co_1}$  (40)

Similarly, the second criteria to design the PI parameters is,

$$PM'_2 = 180 + \angle T_q(j\omega'_{co_2}) - \tan^{-1} \frac{K_{I_2}}{\omega'_{co_2} K_{P_2}} \geq 45^\circ \quad (41)$$

where,  $PM'_2$  is the phase margin of the overall ac voltage loop open-loop transfer function at the frequency  $\omega'_{co_2}$ .

The controller design of the ac voltage loop should take into consideration the maximum loading of the feeder where the TL-UPQC is to be connected. Fig. 14 depicts the frequency response of the overall system considering the ac voltage loop under different operating points. Satisfying (39) to (41), the phase margin is maintained at 91.4°, while the cross over frequency is 0.2 rad/sec for maximum load (e.g. maximum reactive power injection). To investigate the controller's performance under variations in grid impedance parameters, Fig. 15 shows the frequency responses of the overall system for  $L_g = 0.1$  mH, 20 mH and 100 mH. The results show that since the location of the system's poles and zeros are at a higher frequency, the bandwidth of the system will not be significantly affected. Higher  $R_g$  will indicate a higher damping on the grid side.

## V. SIMPLIFIED FILTER DESIGN PROCEDURES

The values of the filter components  $L_P$ ,  $C_P$ ,  $L_A$  and  $C_A$  have been selected based on the following procedures,

1) The design value of  $L_P$  depends on the shunt inductor ripple current. Assuming that the grid current ripple  $\Delta I_G$  is the same as the inductor current ripple then,

$$L_P = \frac{v_{DC}}{4f_{s_1} \Delta I_G} \quad (42)$$

where  $f_{s_1}$  is the switching frequency of the shunt converter.

The capacitor  $C_P$  together with the inductor  $L_P$  form an LC filter at the grid side. The resonant frequency of the LC filter is designed to be one tenth of the switching frequency of the converter to avoid any interaction, hence  $C_P$  is chosen as follows,

$$C_P \geq \frac{1}{L_P} \left( \frac{1}{0.2\pi f_{s_1}} \right)^2 \quad (43)$$

2) The series VSC filter components  $L_A$  and  $C_A$  are designed based on [24]. The selection of  $L_A$  depends on the output current since,

$$L_A < \frac{v_{L_A}}{2\pi f I_{O,max}} \quad (44)$$

where  $v_{L_A}$  and  $f$  are the voltage drop across  $L_A$  and the fundamental line frequency respectively.

The maximum current  $I_{L_A,max}$  that will go through the series converter depends on the maximum output current plus the inductor ripple current  $\Delta I_{L_A}$ ,

$$I_{L_A,max} = I_{O,max} + \Delta I_{L_A} \quad (45)$$

The resonant frequency of the converter is required to be at least 10 times (e.g.  $x = 0.1$ ) lower than the switching frequency

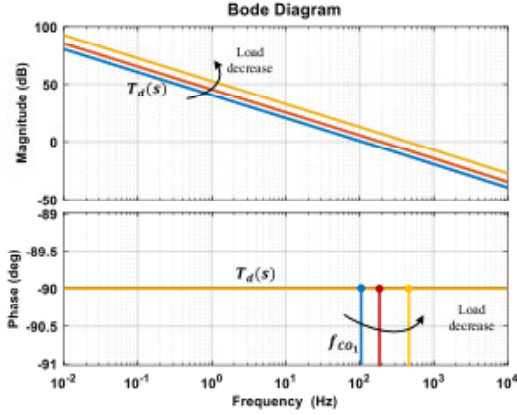


Fig. 12. Frequency response of the dc voltage loop without a compensator.

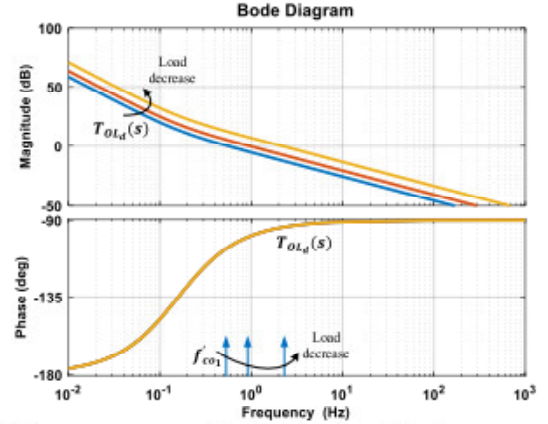


Fig. 13. Frequency response of the dc voltage loop including a compensator.

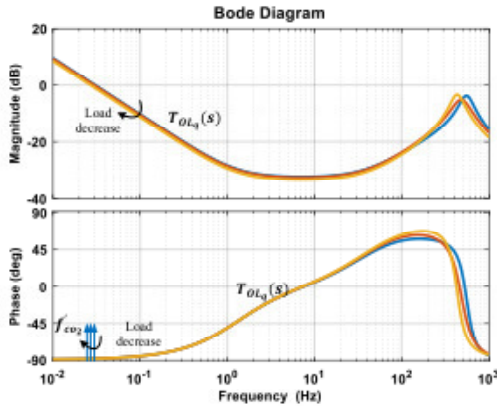


Fig. 14. Frequency response of the ac voltage loop including a compensator under different loads.

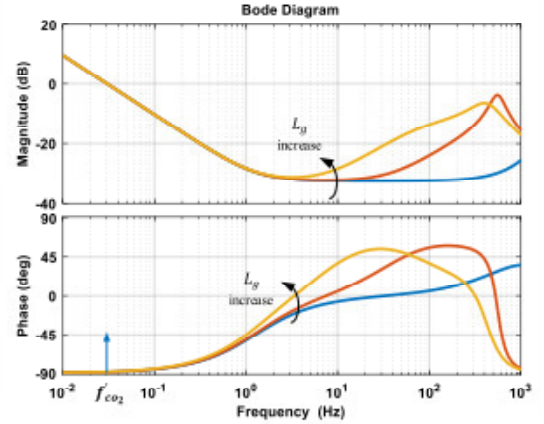


Fig. 15. Frequency response of the ac voltage loop including a compensator under different grid inductances.

of the series converter  $f_{s2}$ . Therefore, the value of  $C_A$  is selected as follows,

$$C_A \geq \frac{1}{L_A} \left( \frac{1}{0.2\pi f_{s2}} \right)^2 \quad (46)$$

## VI. SYSTEM BENCHMARKING

In this section, the system performance has been verified through PLECS simulations. To bench mark the proposed enhanced control methodology, the conventional TL-UPQC, presented in [13] has been developed, simulated and compared with the proposed solution. In this test, the grid voltage has been simulated to fluctuate rapidly to mimic voltage variations in the network at the PCC bus. As mentioned in the introduction section, the conventional control strategy is limited to regulate the load voltage with a fast-dynamic response, while loads that are connected to the PCC side are still exposed to these variations as shown in Fig. 16. Conversely, both sides, input voltage and output voltage of the TL-UPQC, are regulated and maintained at 120V rms under the proposed solution as depicted in Fig. 17.

## VII. EXPERIMENTAL VERIFICATIONS

### A. Experimental Setup and Controller Implementation

A 500VA / 120 V, 60 Hz TL-UPQC converter prototype has been implemented to experimentally verify the proposed control strategy for grid voltage support. The laboratory block

diagram and setup are shown in Fig. 18 and Fig. 19 respectively. In order to emulate a weak grid with a low short circuit ratio (SCR), a programmable ac power source ( $v_G$ ) and a high source impedance ( $Z_g$ ) have been used in the experimental setup. An actual resistor and an inductor have been linked between the grid emulator and the system. By varying the system loading, a varying voltage profile is reflected across the PCC voltage. The programmable ac power supply is used to simulate different voltage power quality problems. A power analyzer has been used to perform power quality measurements. The TL-UPQC prototype is connected to the PCC through a relay to bypass the system in case of faults. The whole control law has been implemented using Texas Instruments TMS320F28377S digital signal processor (DSP). The PI parameters given in Table II, have been chosen based on the small-signal model to satisfy the controllers bandwidth specified in Table III.

### B. Verifications of Mathematical Model

In order to validate the mathematical model, ac sweep analysis has been performed on PLECS simulation model. A perturbation signal has been defined by specifying the frequency sweep range and the number of points on a logarithmic scale. In addition, an experiment test has been employed to analyze the stability of the system using Bode100 Gain-Phase Analyzer. For the test purpose, a small resistance is added to inject a disturbance signal. The Bode100 will provide



the disturbance signal and measures the loop gain of the system. Fig. 20 indicates the suitable injection point and the test setup. Fig. 21 shows good agreement between the mathematical, circuit simulation model results and the measured magnitude and phase.

### C. Nonlinear Load at Bus B

The LEDs used in this test are 9 dimmable LEDs each of 12W that is equivalent to 60W incandescent lamp. Meanwhile the ac voltage under this test signifies the characteristics of a weak grid. Consequently, nonlinear loads connected to the distribution feeders will not only increase the harmonic contents of the input grid current, their nonlinear behavior will also have a significant impact on the PCC bus voltage quality. Fig. 22 (a) displays waveforms of the PCC voltage, grid current, the voltage across the LEDs and the LEDs current without the connection of the TL-UPQC system. Due to the characteristics of the weak grid, the PCC voltage and the load bus voltage are dropped. Also, since the load is nonlinear, the grid current contains high harmonic contents and subsequently the PCC voltage waveform is distorted. Fig. 22 (b) depicts the same waveforms after the TL-UPQC is in operation. It can be noted that the system is capable of retaining both PCC voltage and the load bus at 120V rms at the same time. Moreover, the figure validates the ability of the system to perform harmonics mitigation in the PCC voltage, grid current and load voltage as well. To support the results, power quality measurements with and without the system have been performed and given

Table IV The results in the table demonstrate the improved power quality measurements with the operation of the TL-UPQC system for input voltage, output voltage, input grid current and load current.

TABLE II  
TL-UPQC SYSTEM PARAMETERS

Parameter	Value	Parameter	Value
PCC voltage	120 V	$L_A, C_A$	3.4 mH, 14.1 $\mu$ F
Grid frequency ( $f$ )	60 Hz	$K_{Tdc}, K_{T_{pcc}}$	1, 9.6
DC link Voltage	400 V	$K_{P_1}, K_{I_1}$	0.01, 0.08
$R_g, L_g$	5 $\Omega$ , 20 mH	$K_{P_2}, K_{I_2}$	0.5, 0.5
$C_{DC}$	1500 $\mu$ F	$R_A, R_{sag}$	100 $\Omega$ , 100 $\Omega$
$L_p, C_f$	10 mH, 6.8 $\mu$ F	LED lamps ( $R_B$ )	141.18 $\Omega$
Nonlinear load at bus B		$R_B, L_B$	50-100 $\Omega$ , 40 mH
Linear load at bus B			

TABLE III  
TL-UPQC CONTROLLER DESIGN

Control loop	Bandwidth
Output voltage	6.35 kHz
Input current	1 kHz
DC voltage	2.17 Hz
Load bus control loop	0.03 Hz

TABLE IV  
Power Analysis Measurements without and with UPQC system

Parameters	W/O TL-UPQC	With TL-UPQC
$V_{pcc}$	111.668 V rms	120.008 V rms
$THD - v_{pcc}$	9.60 %	1.78 %
$THD - v_B$	9.76 %	1.75 %
$THD - i_g$	13.73 %	1.43 %
$THD - i_B$	28.21 %	28.09 %

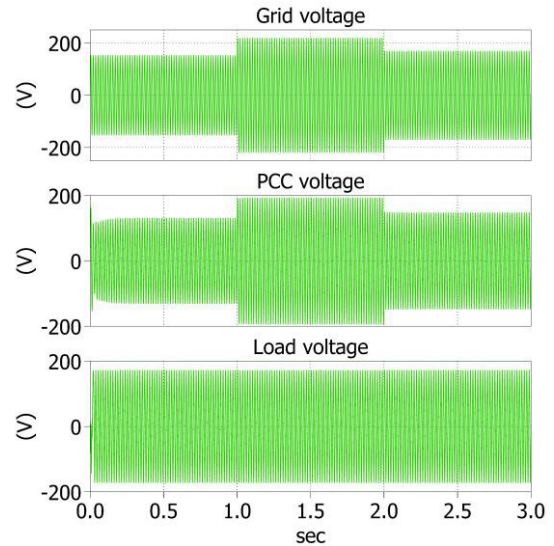


Fig. 16. Simulation results adopting conventional TL-UPQC system under random voltage variations in the network.

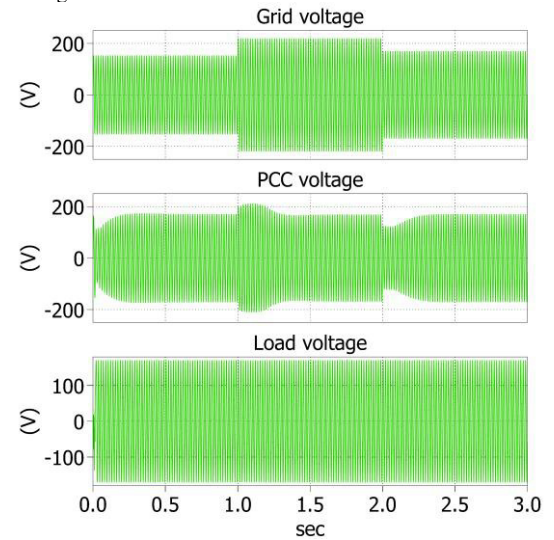


Fig. 17. Simulation results adopting proposed solution under random voltage variations in the network.

### D. Linear Load at Bus B

To show the ability of the system to provide reactive power support for all types of loads. In this test, the LEDs will be replaced by a linear load. If no voltage regulation is required, the system will be operating in the PFC mode. It follows that, the shunt converter injects reactive power rather than harmonics to achieve unity power factor. The linear load parameters connected to load bus B in this test are given in Table II. Fig. 23 (a) shows the voltage waveforms of the grid voltage, the PCC voltage, and the grid current before assisting by the TL-UPQC system. In this case, there is an under voltage at the PCC with 108V rms. Fig. 23 (b) shows the waveforms after activating the TL-UPQC. It can be seen that the shunt converter current  $i_p(t)$  leads the PCC voltage in order to inject reactive power and increase the PCC voltage level, which indicates the operation of the system in the capacitive mode. Alternatively, to emulate an over voltage at the PCC bus, the programmable ac power supply voltage was raised to deliver an over voltage of 132V rms at the PCC bus as shown in Fig. 24 (a). Despite

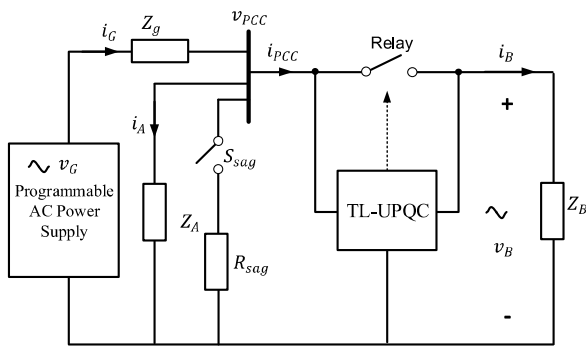


Fig. 18. Experimental test block diagram.

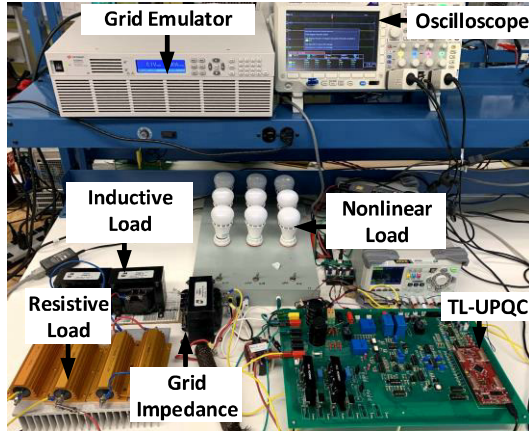


Fig. 19. Laboratory setup.

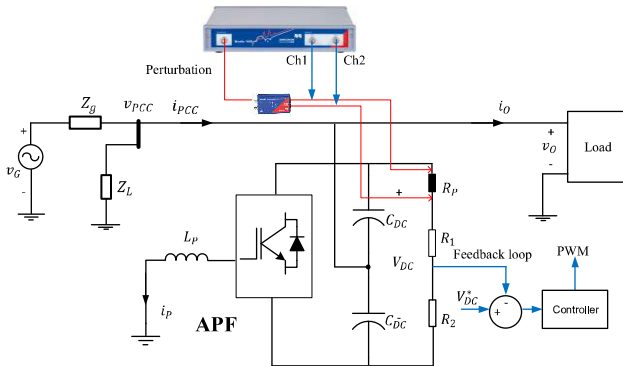


Fig. 20. Connection diagram for frequency response analyzer Bode100.

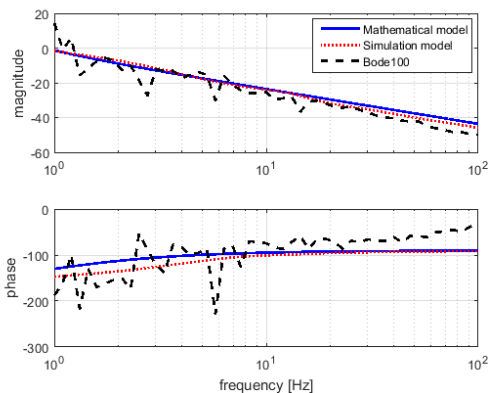


Fig. 21. Frequency response of mathematical model, simulation and experiment.

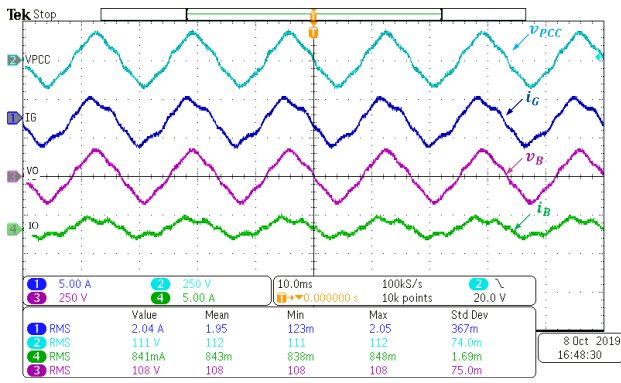
the reflected over voltage at the PCC, the voltage has been maintained at 120V rms by enabling the TL-UPQC as depicted in Fig. 24 (b). In this case, the TL-UPQC system emulates the behavior of an inductive load absorbing reactive power. In other words, the shunt converter current lags the PCC voltage.

### E. Performance Under Transients

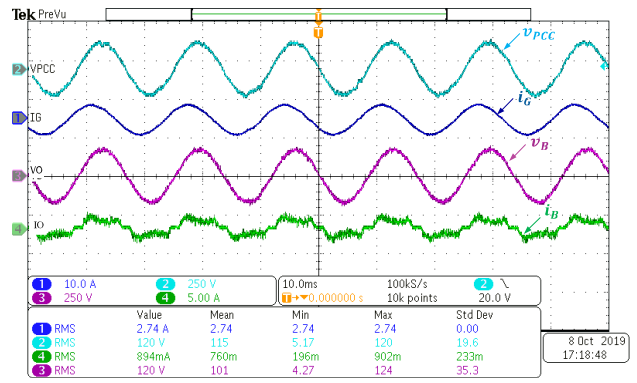
The next experimental case has been carried out to verify the behavior of the UPQC system under dynamic voltage change. The closure of circuit breaker  $S_{sag}$  results in a voltage sag in the network due to a sudden load increase. Fig. 25 validates the ability of the UPQC to react and regulate the PCC voltage under a sudden load increase at the PCC from  $R_A = 100 \Omega$  to  $50 \Omega$ . Under this test, the PCC voltage has been maintained at 120V rms. Fig. 26 demonstrates the system reaction for a voltage swell in the network. The programmable ac power supply has been increased to 155 V rms to emulate a voltage swell at the PCC voltage of 132 V rms. The TL-UPQC system changed its operation from the capacitive mode to the inductive mode as illustrated in the figure. To emulate rapid voltage fluctuations of the PCC voltage due to the connection of DER, the ac power supply has been programmed to emulate a voltage sag followed by a voltage swell and another voltage sag in the network while  $S_{sag}$  is on. Considering the voltage drop across the grid impedance and before enabling the TL-UPQC system, the PCC voltage was correspondingly fluctuating between 92V and 132V rms. The transitory response of the PCC voltage waveform depicted in Fig. 25 (b), shows that by enabling the TL-UPQC, the PCC voltage has been successfully maintained sinusoidal with a constant amplitude. Fig. 28 provides the dc link voltage response during input grid voltage fluctuations while the TL-UPQC system is in operation. The figure validates the performance of the dc link voltage outer loop controller to achieve power balance.

## VIII. CONCLUSION

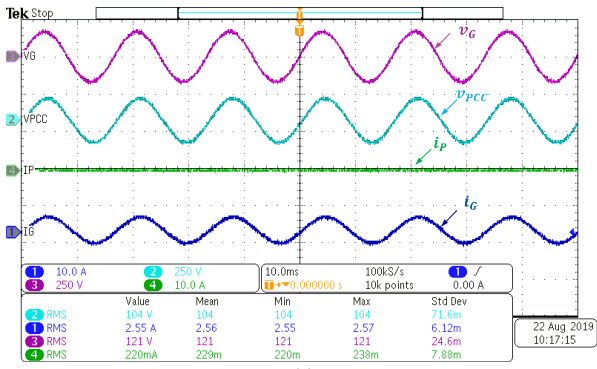
The paper expands the control strategy of a TL-UPQC system to be capable of injecting and absorbing reactive power into and from the input grid in low voltage distribution networks. Employing the proposed enhanced control strategy, the TL-UPQC was able to filter out harmonic components generated by nonlinear loads, compensate all voltage fluctuations across sensitive loads with fast dynamic response and improve the voltage profile of the input grid. A detailed stability analysis and control design criteria employing small-signal models were presented. The experimental results validated the capability of the system to provide voltage regulation at the PCC while supplying linear and nonlinear sensitive loads at the same time. The system was able to reduce the total harmonic distortion of the PCC voltage, the load bus voltage and the grid current. The system was competent to deliver a stable voltage with a constant amplitude to the loads connected to the PCC in the event of voltage sags and swells. Experimental results favorably showed good agreement with the theoretical findings. It is to be noted that adopting a half-bridge topology would increase the voltage stress across the semiconductor switches. Safety mechanisms should be considered if the proposed transformerless system is to be adopted in residential applications.



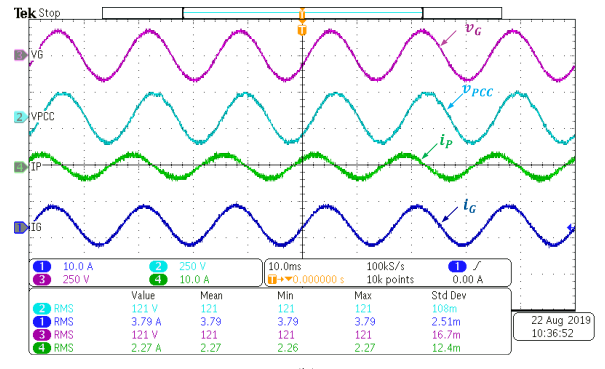
(a)



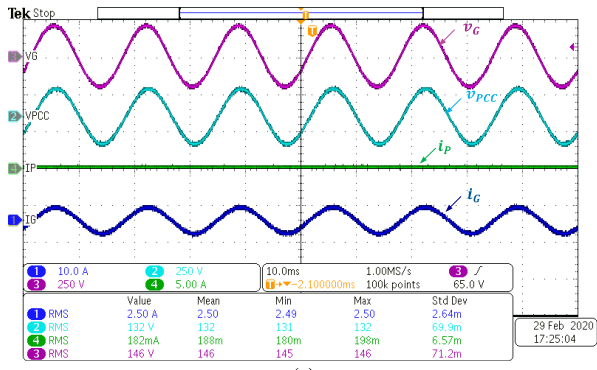
(b)

Fig. 22. PCC voltage  $v_{PCC}$ , grid current  $i_G$ , load bus voltage  $v_B$  and load B current  $i_B$  for nonlinear loads (a) without TL-UPQC (b) with TL-UPQC.

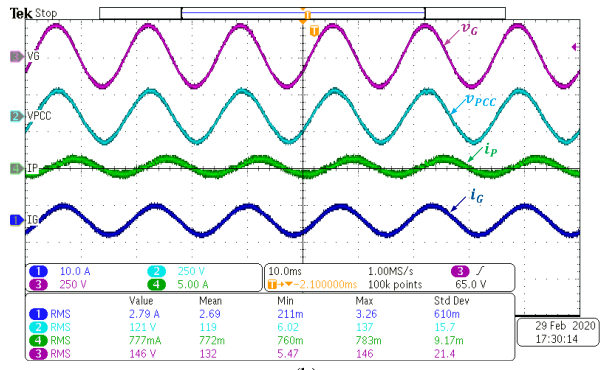
(a)



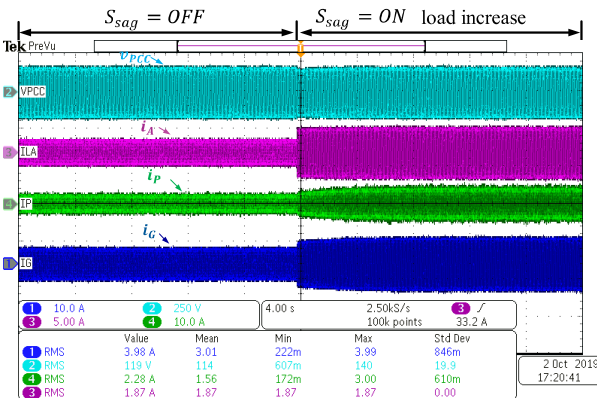
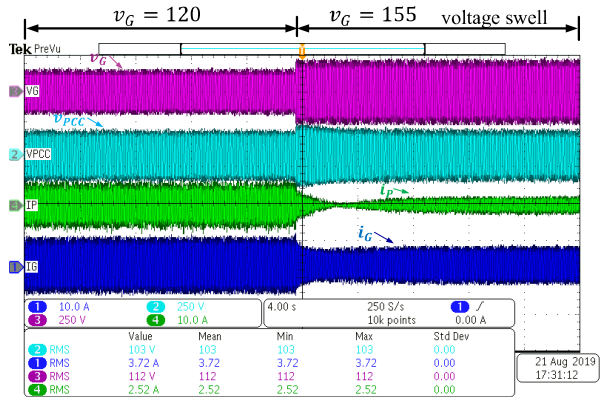
(b)

Fig. 23. Grid voltage  $v_G$ , PCC voltage  $v_{PCC}$ , injected current  $i_p$  and grid current  $i_G$  during an under voltage (a) without TL-UPQC (b) with TL-UPQC.

(a)



(b)

Fig. 24. Grid voltage  $v_G$ , PCC voltage  $v_{PCC}$ , injected current  $i_p$  and grid current  $i_G$  during an over voltage (a) without TL-UPQC (b) with TL-UPQC.Fig. 25. PCC voltage  $v_{PCC}$ , load A current  $i_A$ , injected current  $i_p$  and grid current  $i_G$  for a sudden load change (voltage sag).Fig. 26. Grid voltage  $v_G$ , PCC voltage  $v_{PCC}$ , injected current  $i_p$  and grid current  $i_G$  for a sudden voltage change (voltage swell).

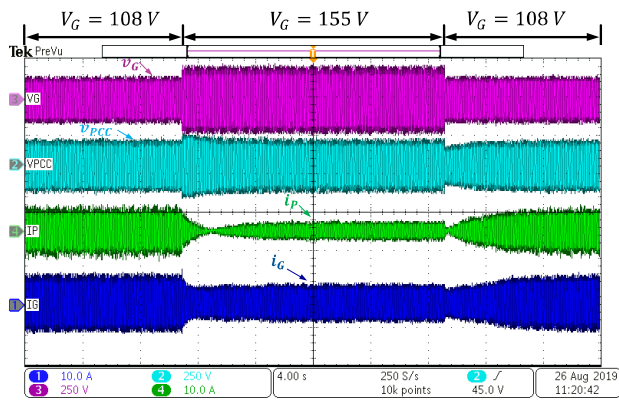


Fig. 27. Grid voltage  $v_G$ , PCC voltage  $v_{PCC}$ , injected current  $i_P$  and grid current  $i_G$  during rapid voltage fluctuations.

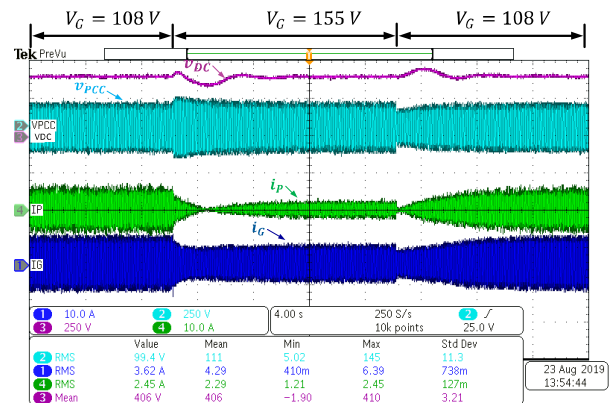


Fig. 28. DC link voltage  $v_{DC}$ , PCC voltage  $v_{PCC}$ , injected current  $i_P$  and grid current  $i_G$  during rapid voltage fluctuations.

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