Development of Interface Model and Design of Compensator to Overcome Delay Response in a PHIL Setup for Evaluating a Grid-Connected Power Electronic DUT

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***Abstract*— The Power Hardware in the Loop (PHIL) is an attractive way of performing various studies for testing a non-linear power electronic converter in laboratory scale and yet get a result that resembles an actual like scenario. This approach, however promising, suffers from various stability problems arising due to the interface between the hardware and software environment required to create a PHIL. This paper presents a thorough analysis of the stability problem in PHIL by individually studying the interface device that forms the Ideal Transformer Method (ITM) interface. The model of the ITM interface is developed and verified experimentally using a frequency sweep approach. The developed model can serve as a tool to understand the factors affecting the stability in a PHIL set up. Utilizing the developed model, this paper proposes a Smith Predictor compensator that eliminates the effect of delay in the closed loop response of the system. The Smith Predictor compensator is designed and implemented in a Real Time Digital Simulator (RTDS) platform and the performance of the compensator is verified through various experiments. A case study of a compensator employed resistor divider network is presented to validate a stable PHIL, both theoretically and experimentally. Further, the proposed compensator is tested to evaluate a 250 W grid connected Photovoltaic (PV) inverter in a PHIL.**

***Index Terms*— Ideal Transformer Method (ITM), Photovoltaic (PV) Inverter, Power Hardware in the Loop (PHIL), Smith Predictor Compensator**

I. INTRODUCTION

THE increasing trend towards renewable based energy sources demand more system level investigations. The impact of integrating these sources at different power coupling point becomes important for system engineer to ensure stability as well as to aid in system planning. Microgrids that integrate renewable energy sources are new approach for overcoming high operating costs for delivering power to remote communities and providing improved energy efficiency of electrical networks in modern buildings [2][3]. However, most of research in this topic is at the computer simulation level or individually testing of a power apparatus in microgrid. These studies entail a wide technology gap between the reported research results and the realities of practical performance [4]-[6]. In order to achieve results more accurate to the practical system, it has been proposed to use Power-Hardware in-the-Loop (PHIL) to evaluate microgrids with actual power flowing into the electrical networks and devices [7]-[13]. Unlike the existing real-time simulation where the entire system with controllers and power-networks are simulated in real-time, PHIL is an extension to these real-time simulations and existing Controller-Hardware-in-the-Loop (CHIL) simulations. PHIL architecture involves exchange of power between a power-network in real-time simulation environment with an actual hardware device. With this feature, PHIL stands out among real-time simulations for running a wide variety of tests ranging from evaluating power converters, performing various grid interaction studies, integration of renewables in microgrid to various source emulation applications.

In industries, PHIL platforms have been widely adopted to evaluate systems with real energy sources and energy storage elements to study the interactions between them [14]. In order to enhance power process efficiency and enable full manual control of element characteristics, full power electronics PHIL platforms have been proposed that use power electronic emulators instead of real energy sources and storage elements. One example is a Fuel Cell (FC) energy source. This requires a power electronic converter and a controller to emulate the electrical behaviors of the FC to have reactions with the connecting system [15][16]. For the PHIL applications described above, it is a common practice to usually evaluate a single element, e.g. FC, single device-under-test (DUT), or Electronic Ballasts, in the power loop.

To set up a PHIL arrangement for testing and evaluation of various DUTs, it is obvious that an interface is needed to interact the actual hardware (DUT) with the real-time software model. This interface is created with devices like Analogue to Digital Converter (ADC) cards, Digital to Analogue Converter (DAC) cards, power amplifier and sensors which are arranged in ways to come up with various interface algorithms [17][18]. Among other interface algorithms like Damping Impedance Method (DIM) and Partial Circuit Duplication method (PCD), Ideal Transformer Method (ITM) is preferred considering its

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balance between accuracy and ease of implementation [17] [19]. ITM, in general, requires an amplifier to amplify the signal fed out from digital Real Time Simulator (RTS) to the required power level and then fed back to RTS using a sensor. The amplified signal and sensed signal could be either a voltage or a current and vice versa. Based on the type of signal amplified and sensed, ITM algorithms are termed as voltage or current ITM. A typical voltage ITM is shown in Fig. 1 for a test setup used to evaluate a Power Electronics (PE) based DUT [17][20]. The choice of voltage mode and current mode ITM is generally dependent on the DUT. For example, in case of source emulation like the battery and the grid, the voltage mode would simplify the emulation but for sources like Photovoltaic (PV) it could be either.

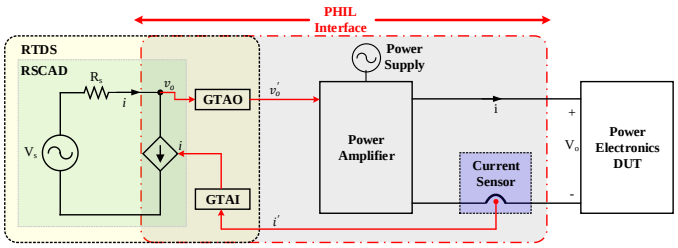


Fig. 1. Power Hardware in the Loop Arrangement.

The PHIL architecture offers a variety of advantages while evaluating a DUT in terms of the flexibility to create various testing conditions in the laboratory set up. At the same time, this way of system evaluation suffers from a major disadvantage of stability and accuracy due to interface device delays and inaccuracies. There are literatures that discuss the stability of an ITM interface by modelling each interface devices with their respective transfer functions (TF) and delays [17][19]-[23]. These stability studies are made mostly with Nyquist and Routh-Hurwitz criteria based on the models with delays [20]-[22]. While both these tools offer advantages in stability assessments, there is no clear mention on the accuracy of these models which are relied on theoretical formulations only. Besides, it is vital that any stability or accuracy analysis made henceforth with the existing interface models be handled with extra caution. Instead, a better approach would be to first ensure that the interface model is accurately reflecting the actual interface hardware in action. Taking this into consideration, this paper proposes an operational-sequence-based model of interface devices and validates this model experimentally using frequency sweep approach. The frequency sweep is carried out using a Gain Phase Analyser (GPA) to the interface consisting of analogue cards and a linear amplifier with RTS in the loop. In this paper, RTDS with its Giga-Transceiver Analogue Output (GTAO) and Giga-Transceiver Analogue Input (GTAI) cards is used for validation of the model experimentally.

The stability analysis of PHIL has made the part of many research literatures [17][20][21]. This is due to the fact that if a system is decoupled at a certain power exchange point and an interface is introduced to complete this power flow loop, it comes at an expense of delay and limited bandwidth within the interface that raises the concern of stability. While, ideally, it is desirable to have an infinite bandwidth interface with no delays, practically it is not achievable as the conversion time within the ADC, DAC cards, the computation of the RTS and the response of the amplifier contributes to this delay and bandwidth restrictions. With this, it is therefore required that a comprehensive analysis of the stability of PHIL system be performed.

Taking the advantage of the experimentally verified model of the interface device, this paper presents the design and implementation of a Smith Predictor compensator that eliminates the effect of delay on a closed loop response of a PHIL system. This enables to achieve a stable PHIL loop to test and evaluate a grid connected PV inverter. Subsequent sections in the paper describe the details of work in following order; the mathematical model of ITM interface is developed in Section II followed by experimental evaluation and model validation in Section III, Section IV discusses the stability problems in PHIL due to delay and proposes a concept of overcoming delay responses, finally in Section V experimental results of a stable PHIL implementation with case studies are presented.

II. Mathematical Model of ITM Interface

The general arrangement of a PHIL in ITM interface is shown in Fig. 1. As seen in Fig. 1, the combination of GTAO, Power Amplifier, sensors and GTAI forms the interface device in an ITM. Considering this, the sections following studies each of this interface devices and develops a working model that can be used in performing stability and accuracy studies. The analyses made throughout this paper considers the sensor's response to be fast enough to model it as a device with unity gain.

A. Model of an Analogue Input Card

The Analogue Input (AI) card, labelled as GTAI in arrangement of Fig. 1, takes signals from the physical system into simulation environment for further processing. This requires that the physical analogue signal be first converted to digital before it can be used in the simulation system.

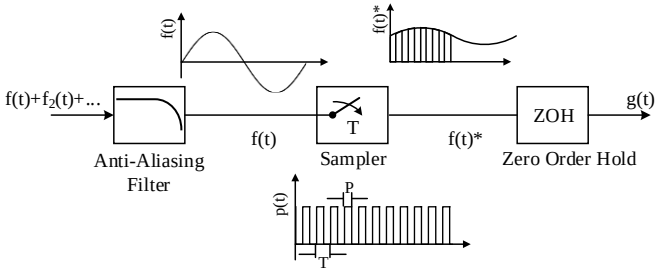


Fig. 2. Functional Block of an AI card.

The operational sequence of an AI card can be represented by a functional block in Fig. 2. The AI card consists of 12 channels, 16-bit resolution ADC with an Anti-Aliasing Filter (AAF) at each input before the ADC to remove the aliasing due to sampling. The TF representing the AAF model can be expressed as a first order low pass filter given as;

$$G_{aaf}(s) = \frac{G_{aaf}}{1+sT_{aaf}} \quad (1)$$

Where, G_{aaf}=gain of the filter, and $T_{aaf} = \frac{1}{2\pi f_{aaf}}$ is the cut-

off of the AAF. The AAF cut-off is to be selected based on the sampling or the time-step used in the RTS model.

Further, the ADC process can be represented in two steps; first, by a sampler which samples the continuous time signal $f(t)$ by a series of pulse train with width P and period T, and followed by a zero-order hold (ZOH). If the width of the pulse P is very small, the sampling operation can be simplified using an impulse sampler. Mathematically, the sampling operation in frequency domain can be expressed by the convolution of original signal with a pulse train.

$$F^*(\omega) = \frac{1}{2\pi} F(\omega) * P(\omega) \tag{2}$$

Where, $P(\omega) = 2\pi \sum_{k=-\infty}^{k=+\infty} P_k \delta(\omega - k\omega_s)$ and using Fourier Transform P_k can be derived as $\frac{1}{T_s}$ for all Fourier series coefficients with ω_s being the radial sampled frequency given by $\omega_s = T_s/2\pi$. This yields the frequency domain representation of an impulse sampling train.

$$P(\omega) = \frac{2\pi}{T_s} \sum_{k=-\infty}^{k=+\infty} \delta(\omega - k\omega_s) \tag{3}$$

Substituting (3) in (2) and using convolution property with impulse we arrive at the final expression of sampled signal.

$$F^*(\omega) = \frac{1}{T_s} \sum_{k=-\infty}^{k=+\infty} F(\omega - k\omega_s) \tag{4}$$

Equation (4) shows that a sampled signal contains an infinite collection of the shifted version of the original signal frequency spectrum $F(\omega)$ scaled by a factor $\frac{1}{T_s}$. The above deductions are directly interchangeable with the Laplace domain. Therefore expressing (4) in s-domain results in;

$$F^*(s) = \frac{1}{T_s} \sum_{k=-\infty}^{k=+\infty} F(s - \mathrm{j}k\omega_s) \tag{5}$$

Unlike an impulse sampler which cannot be physically realized, more practical way to sample is ZOH which can be understood as an impulse sampled signal fed to a low pass filter.

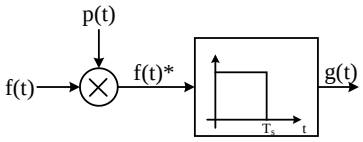


Fig. 3. Mathematical Model of a ZOH.

The block diagram formulation of ZOH is shown in Fig. 3 , where $f(t)$, $p(t)$ and $f(t)^*$ are the continuous time signal, sampler signal and sampled signal respectively. The ZOH operation in Fig. 3 can be explained as; for every impulse sample that comes in, a rectangular pulse comes out. The frequency domain representation of a ZOH operation can be expressed by (6).

$$H_{zoh}(s) = \frac{1 - e^{-sT_s}}{s} \tag{6}$$

From (5) and (6) the overall TF that models the ADC process in general can be obtained. It is also valid to assume that the high frequency components due to sampling will have minimal to no effect due to the low pass nature of ZOH. Hence, only considering the low frequencies would yield to:

$$G(s) = \frac{1 - e^{-sT_s}}{sT_s} F(s) \tag{7}$$

From (1) and (7) the complete model of AI card can be obtained as;

$$G_{AI}(s) = \frac{G_{aaf}(1 - e^{-sT_s})}{sT_s(1 + sT_{aaf})} \tag{8}$$

B. Model of an Analogue Output Card

The Analogue Output (AO) card, labelled as GTAO in Fig. 1, functions to feed out the signal specified in the simulation environment to signal that can be directly processed for real world applications. This includes use of this signal as control signal when working with CHIL applications or as a power signals after amplifying for PHIL applications. Irrespective of the application, the conversion in the AO card is carried out by a high precision DAC and therefore can simply be represented by the conversions delay specified in the hardware manual.

$$G_{AO}(s) = e^{-sT_1} \tag{9}$$

Where, T_1 is the conversion time it takes for the digital value to be converted to its corresponding analogue value.

C. Model of a Linear Amplifier

For a PHIL application with linear amplifier, the transfer function model can be estimated with a first order low pass characteristic. The model contains a gain to represent the amplification and a low pass cut-off frequency that represents the bandwidth of the amplifier. Additionally, a delay function is needed to incorporate the delay between input and output of the amplifier. The complete model of amplifier is given by (10).

$$G_{AMP}(s) = \frac{A}{1 + sT_{amp}} e^{-sT_2} \tag{10}$$

Where, A= amplifier gain, T_{amp}=amplifier bandwidth=$\frac{1}{2\pi f}$, and T_2=delay between input and output.

III. Experimental Evaluation and Model Validation

The individual model of interface devices developed in Section II needs to be verified to check for their accuracy. For this, the combination of AO and AI cards are configured in real hardware set up to extract their frequency responses. The frequency response obtained from the experimental measurements can then be compared with the frequency response from the developed model for their accuracy. For the purpose of this paper, the models are developed considering RTDS along with its accessories cards as the RTS. A four-quadrant linear amplifier from AE TECHRON 7224 is used as the amplification device for PHIL application. To extract the experimental frequency response of these devices, a GPA from Bode-100 is employed. A GPA is used to inject various frequencies into the system and measure the sweep response back from the GPA. This approach allows to generate the gain and phases at various frequencies experimentally for the DUT.

A. AO-AI Card Model Extraction and Validation

The experimental determination of frequency response of individual AO and AI cards is not possible as either of input or output points are inaccessible in physical hardware. The way around this is to set up a GPA such that it feeds multi frequency sinusoid as an input to the AI card and measures the response at the AO card. With this, the sinusoid fed through AI card from GPA experiences AAF, ADC, a time step delay at the simulation environment through its path before it is fed out of high precision DAC by AO card back into the GPA. This allows to extract the frequency response of both the AO and AI cards combined at once. The system implementation setup to achieve the experimental determination of frequency response of AO-AI card combination is shown in Fig. 4. As explained in Fig. 4, GPA labelled as Bode 100 feeds the multi frequency sinusoid into AI card which is monitored at Channel-1 and the response out from AO card monitored at Channel-2. The resulting frequency response from GPA is extracted through the interfacing software.

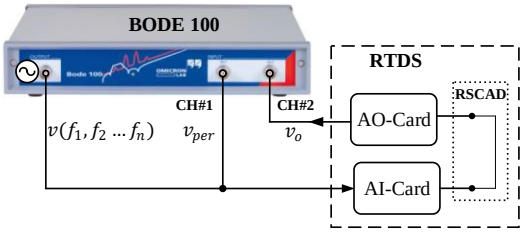


Fig. 4. Hardware Setup for frequency response extraction of AO-AI card.

To compare the individual interface model with the experimental result, a similar setup as in Fig. 4 is considered. The combined AO-AI card model can be derived from (8) and (9). However, an additional time-step delay is required in order to rightly represent the setup of Fig. 4. With this the TF of the AO-AI card combination can be written as;

$$G_{AOAI}(s) = \frac{G_{aaf}(1-e^{-sT_s})}{sT_s(1+sT_{aaf})} e^{-s(T_1+T_d)} \qquad (11)$$

Where, T_1 is the conversion time of DAC and T_d the time step delay. Usually the effect of T_1 is very minimal as compared to that of time step and hence can be excluded from the analysis.

To verify that a signal experiences a time step delay while going through AI to AO card, a ramp signal with a flat top and bottom is manually generated using a Keysight function generator and fed into AI. The input to AI and output from AO is overlaid together to measure the delay between input and output. The fact that RTDS has a projection advance factor at AI input to compensate for the time step, for a waveform with sharp slope, this would distort the signal at the point of rapid change. Therefore, a flattened ramp would give a good estimate of the round-trip delay. The experimental result estimating the time delay from input AI to output AO is shown in Fig. 5.

TABLE I
PARAMETERS OF AO-AI MODEL

Parameter	Value	Parameter	Value
G_{aaf}	1	T_1	1.8 µs
T_{aaf}	$1/(2\pi f_{aaf})$, $f_{aaf} = 10.1\ kHz$	T_s , T_d	20 µs, 50 µs

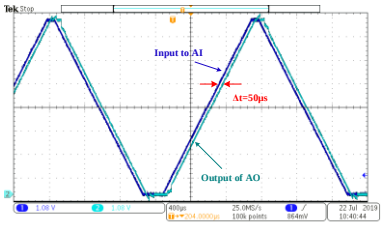


Fig. 5. Delay measurement from AI to AO for a time step of 50µs.

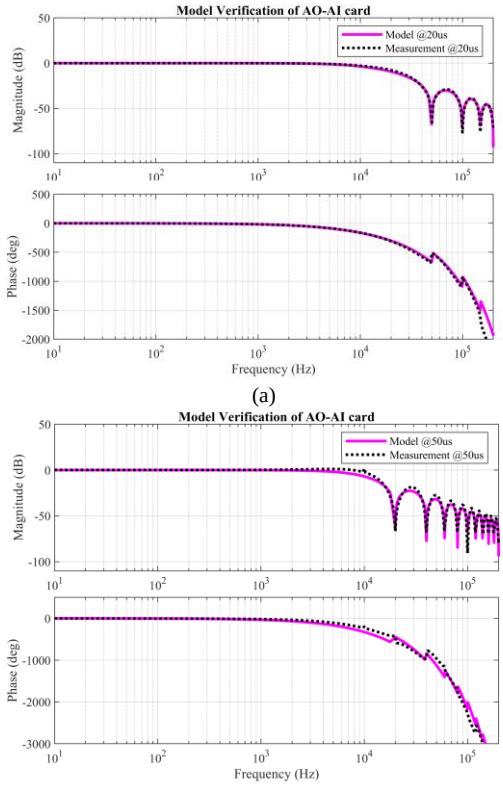


Fig. 6. AO-AI frequency response for a time step of (a) 20 µs (b) 50 µs.

The gain and phase plot of AO-AI model with the parameters described in TABLE I for a time step of 20 µs and 50 µs is compared with the experimentally obtained data with the setup shown in Fig. 4. The plots of gain and phase are overlaid and presented in Fig. 6. The results show a good agreement between the experiment and theoretical model in a certain frequency range. Also, as the Nyquist criteria would be violated after a certain frequency, the measured signal cannot entirely follow the modelled response. Again, it is irrelevant to consider the model after the Nyquist frequency. Therefore, considering linearity, the proposed model gives an accurate response as that of the actual system.

B. Linear Amplifier Model Extraction and Validation

The frequency response measurement for a linear amplifier is made in a way similar to the method mentioned for AO-AI card. The GPA is used to inject a multi-frequency sinusoid at the input of amplifier and the gain of the amplifier is set to its maximum, a value of 20. It is important to pay extra care when feeding back the amplified output to the GPA so that it is within the range supported by GPA. For this purpose, a probe with

suitable attenuation is selected such that amplified voltage can be lowered. Also, this attenuation can be recovered back in the software with proper calibration.

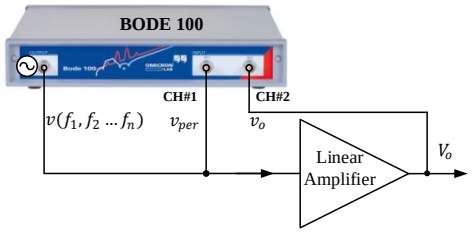


Fig. 7. Hardware Setup for frequency response extraction of Linear amplifier.

The experimental setup for frequency response measurement of a linear amplifier is presented in Fig. 7. Similar to that of AO-AI card, the output from GPA is fed to the input of amplifier and is also monitored by GPA in Channel-1. The output of the amplifier is fed back to Channel-2 of GPA through a Testec differential probe with attenuation 1:1/10.

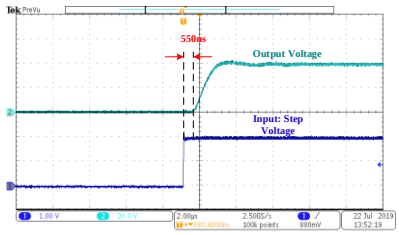


Fig. 8. Delay measurement of a Linear amplifier.

The linear amplifier model is expressed by its TF in (10). The parameters, like, the gain and bandwidth, required to plot frequency response of (10) is taken from its datasheet. The delay however is determined experimentally. The delay measurement recorded is shown in Fig. 8. Multiple runs were made, and each measurement were averaged to estimate the delay. With the parameters of TABLE II, the frequency response of linear amplifier is plotted. Also, the frequency response obtained experimentally is overlaid with the developed model, the results are overlaid and presented in Fig. 9.

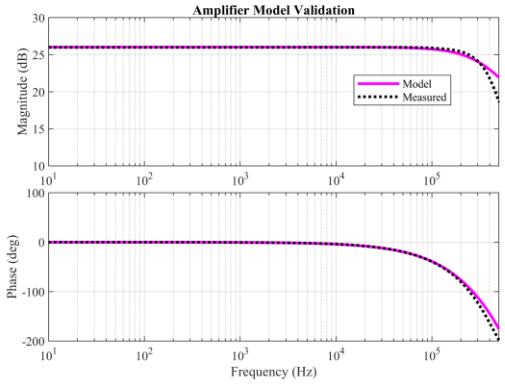


Fig. 9. Linear Amplifier frequency response, model and measured.

TABLE II
PARAMETERS OF A LINEAR AMPLIFIER

Gain (A)	Bandwidth (T_{amp})	Avg. Delay (T_2)
20	$1/(2\pi f)$, f= 400 kHz	687 ns

C. *Linear Amplifier with AO-AI*

The measurement setup of a combination of linear amplifier with AO-AI card follows the similar setup as that of AO-AI except the amplifier comes after the output of AO before it is fed back to the GPA, shown in Fig. 10. Careful consideration as that of linear amplifier frequency response measurement is to be taken, especially when the output of amplifier is fed back to the GPA. Probe compensations are to be made beforehand.

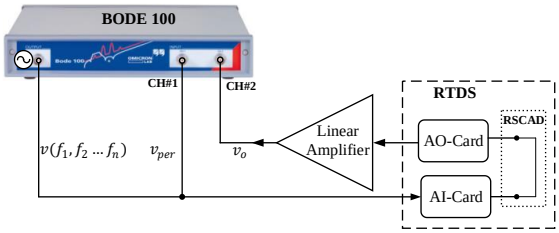


Fig. 10. Hardware Setup for frequency response extraction of Linear amplifier with AO-AI card.

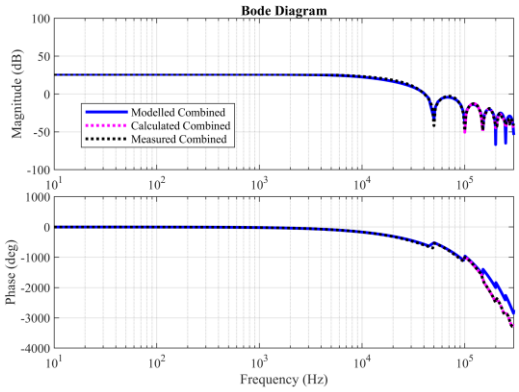


Fig. 11. Frequency responses of modelled, calculated and measured AO-AI-Amplifier combination.

The model developed for the AO, AI and linear amplifier forms the basis for verification of similar other architectures. Considering the linearity of the system and using superposition, the system of TFs can be lumped to obtain the overall system model consisting of AI-AO-amplifier combination. The setup shown in Fig. 10 can be used to export the frequency response experimentally of such combination. The result from the experiment and model are overlaid in Fig. 11. The theoretical frequency response is in close agreement with experimental responses. In addition, the linearity of the system is also verified by adding the individual experimental responses of AO-AI and amplifier and compared with combined experimental and theoretical responses. As seen from Fig. 11, all three responses overlap each other until a frequency close to 100 kHz. This therefore validates the developed model that can be used to further the studies in PHIL.

IV. STABILITY OF A PHIL WITH ITM INTERFACE

The stability studies in PHIL has made the focus of many research works. Moreover, before investigating the stability, it is important to understand the PHIL operation. As the interface differentiates the PHIL system from its actual counterpart, from the standpoint of system performance, the interface in PHIL

plays a significant role in defining stability as well as accuracy. Therefore, it is evident that an in-depth examination of the interface is required to gain clarity on the PHIL performance.

To decouple the problem; first major concern is the time delay of the PHIL loop and its effect on the stability and second challenge is to obtain a near real-time results with acceptable errors. Subsequent sections on the paper present in-detail analysis considering the delay effect on stability and methodology to overcome the delay response in a PHIL system.

A. Time Delay in PHIL

The time delay in PHIL is the result of interface devices cascaded to form the power exchange medium. Ideally, it is desirable to have a system without any delays. Moreover, with the digital RTS running at a certain time-step, even if the interface is designed to have no delays the unavoidable time-step delay is inherently present within.

A time dependent function *f(t)* with a time delay T_d when exposed to a unit step input can be represented as *f(t-Td)*. Taking Laplace transform, it can be expressed in frequency domain by (12).

$$f(t - T_d) \xrightarrow{\mathcal{L}} F(s)e^{-sT_d} \tag{12}$$

The function in (12) represents an exponent with constant magnitude and infinitely growing phase. This infinite phase lag resulting from time delay leads to a non-rational TF and mathematically be seen as a system with infinite dimension state vector which makes it difficult to control and analyze [24]. In order to avoid such situation, it is a general practice to rationalize the exponential TF of time delay using Taylor, and Padé Approximations (PDA) [25][26]. Among other methods, it is observed that rational approximation of delay using PDA has the highest accuracy when the order of numerator is one less than the denominator [25]. The analysis that follows considers PDA with denominator and numerator of the order three and two respectively expressed as:

$$PDA_{23}(e^{-sT_d}) \approx \frac{60-24\cdot sT_d+3\cdot(sT_d)^2}{60+36\cdot sT_d+9\cdot(sT_d)^2+(sT_d)^3} \tag{13}$$

B. Compensation Design for a Delay Free Response

One of the feasible solutions to eliminate the effect of delay in PHIL is to compensate for it in the result. A compensation method that addresses the phase delay introduced by the time delay is reported in [27]. This compensation method uses a high pass filter to provide the additional phase to compensate for the delay. Another method to compensate for the effect of delay is to add a phase advance to the fundamental and harmonic component obtained after Fourier analysis of original signal in RTS [28]. The original signal is then recreated from the phase advanced signal and amplified to get rid of the time delay in PHIL loop. However, this method suffers from a lot of limitations like number of harmonics order, time to solve Fourier by RTS, and power angle of DUT at software node. Another work by [29] considers the entire PHIL loop like a classical control block and introduces a pole-zero compensator that overcomes any inaccuracies within the specific frequency range. It is also shown that the stability limit of a PHIL loop is improved with the compensator; specially for a DIM interface.

Time delay compensation has been popular in process control systems where the time delay originates from the sluggish nature of the plant. This delay in system to respond to any control actions has led system to run towards instability. This has been a trivial problem for researchers for decades and numerous solutions to overcome the effect of time delay have been proposed. One among many solutions was proposed by O.J.M.Smith, which eliminates the delay effect in the closed loop response by inserting a feedback loop in the original system, termed as Smith Predictor (SP) [30][31]. Another advantage of SP is that it can be incorporated with the system with existing controllers [32][33]. This makes SP an ideal application for PHIL to eliminate delay in its closed loop response and incorporating compensators as [29] to improve the stability. As per the best of authors knowledge, such application of SP in PHIL has not been reported in the literature so far and therefore makes the study of this work.

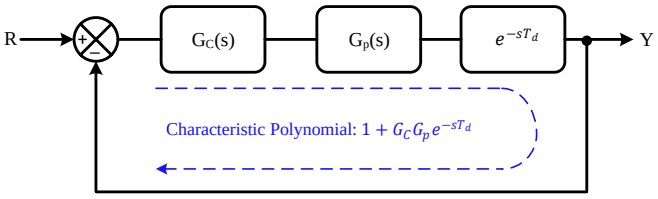


Fig. 12. Control of a plant with delay.

A standard block representing a delay inherited plant G_p controlled by a controller G_C is shown in Fig. 12. The closed loop response of such delayed plant with a standard controller would contain the delay term with infinitely growing phase. This makes the system difficult to achieve the set design criteria and controller design becomes extremely difficult. However, if the delay term in the forward path is pushed after the feedback node, the closed response of the resulting system would no longer contain the delay term. To achieve this objective, a SP based compensator can be designed.

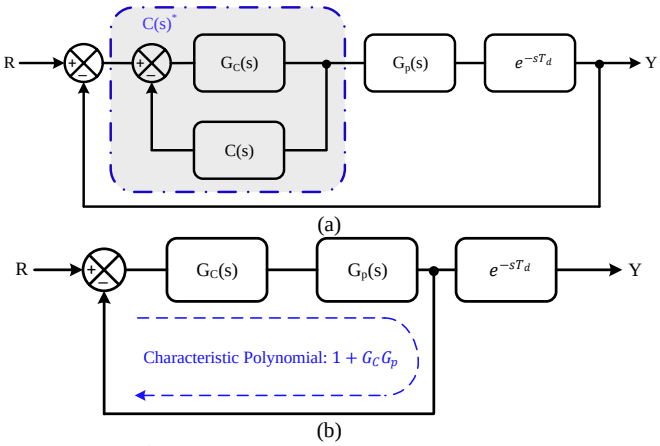


Fig. 13. Control of plant with delay (a) SP employed block (b) equivalent block.

Following up with the control block in Fig. 12, the SP employed block with compensator $C(s)$ and the expected equivalent block is presented in Fig. 13. The input to output

closed loop TF from Fig. 13(a) and Fig. 13(b) can be derived and equated to obtain the compensator TF $C(s)$. From Fig. 13(a),

$$\frac{Y(s)}{R(s)} = \frac{G_p(s)C(s)^* e^{-sT_d}}{1+G_p(s)C(s)^* e^{-sT_d}} \tag{14}$$

Where, $C(s)^*$ is the combined controller and compensator TF. Similarly, from Fig. 13(b), the equivalent closed loop response that is expected by employing a SP can be obtained and is given by (15).

$$\frac{Y(s)}{R(s)} = \frac{G_p(s)G_c(s)}{1+G_p(s)G_c(s)} e^{-sT_d} \tag{15}$$

Equating the closed loop TF of (14) and (15), the TF of $C(s)^*$ can be obtained;

$$C(s)^* = \frac{G_c(s)}{1+G_c(s)G_p(s)(1-e^{-sT_d})} \tag{16}$$

Also, referring to block in Fig. 13(a), $C(s)^*$ can be derived;

$$C(s)^* = \frac{G_c(s)}{1+G_c(s)C(s)} \tag{17}$$

The SP compensator TF can finally be found by comparing (16) and (17);

$$C(s) = G_p(s)(1 - e^{-sT_d}) \tag{18}$$

Equation (18) gives the model of compensator to be employed in the forward path along with existing controller to achieve a delay free response. Moreover, an important observation from (18) is that it requires the model of plant and delay. When such compensator is realized for a system consisting of delays like the PHIL, it becomes critical that each device in the PHIL loop is modelled accurately. And, this is where the experimentally verified model in Section II and Section III comes particularly handy. So is the case with delay model, whose accuracy with PDA is well discussed in literatures [24][25][26]. With the interface and delay model, it is apparent that there is enough information to go forward with the compensator design for a PHIL system.

C. *Delay Compensation of a PHIL System*

To demonstrate the delay compensation in a PHIL system, a standard case of a resistor divider network arranged in PHIL configuration shown in Fig. 14 is considered. The input is a controlled voltage source which could be a DC, or an AC connected to an input resistor R_s. The network is decoupled by an ITM interface at the node between two resistors R_s and R_h.

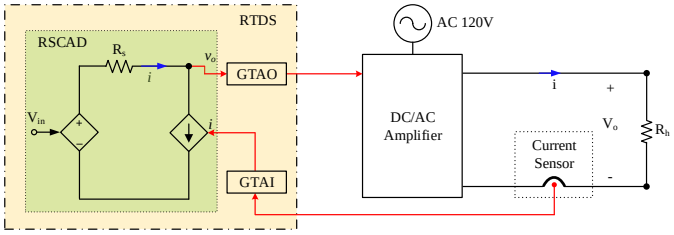


Fig. 14. PHIL arrangement of a Resistor divider network.

The system in Fig. 14 can be developed to form a standard control block like structure by expressing individual interface devices by their respective TFs developed in Section II. The architecture of the PHIL for resistor divider replicates the combination of AO-AI-amplifier as in the model validation section. This can also be seen from the control block in Fig. 15. A delay due to time step is included in the forward path to accurately model the arrangement in Fig. 14.

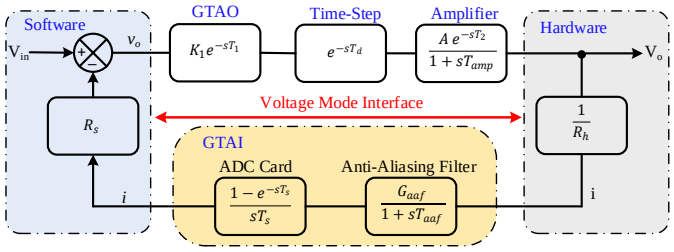


Fig. 15. Control block representation of a PHIL resistor divider network.

The system in Fig. 15 closely resembles the standard control of Fig. 12, except the controller $G_c(s)$ and an additional transfer function in the feedback path. Similar sequence of mathematical formulations can be made to design the compensator that eliminates the effect of delay in forward path in the closed loop response. However, before that, it is essential to study the system response without the compensator. For this, Nyquist plot and step response of the system are analyzed for the parameters of the interface specified in TABLE I and TABLE II for resistances ratio $R_s/R_h = 1.4$ with a time step of 50 µs.

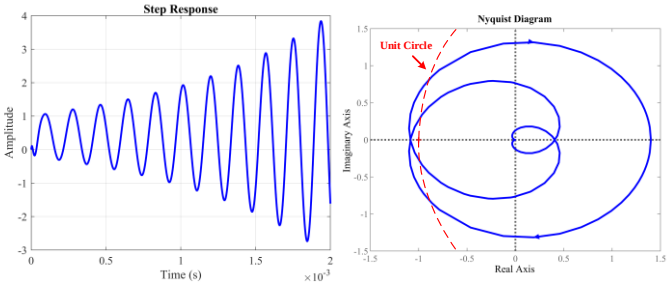


Fig. 16. Response of an uncompensated PHIL network.

As can be seen from the plot of Fig. 16, the time response of the uncompensated PHIL shows an increasing oscillatory response, and the Nyquist plot shows an unstable closed loop response as the unit circle is encircled in a clockwise direction. Further, it is observed that the system response degrades as the time delay increases. This proves the need for improvement of the uncompensated PHIL system.

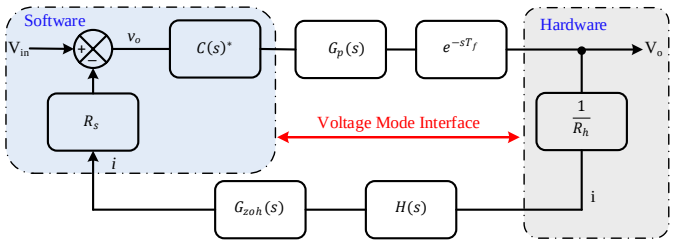


Fig. 17. Architecture of a compensated PHIL network.

Once the response of an uncompensated system is studied, it becomes evident the need to overcome the effect of delay. To achieve this, a SP based compensator can be designed and placed in the software environment. Other advantage of having the compensator in software environment is the flexibility with which it can be redesigned to match the design specifications. The redesigned control block of Fig. 15 with compensator inserted is shown in Fig. 17. All the delays in the forward path are lumped into T_f, the gain K_1 and A are configured to cancel out each other and other notations in Fig. 17 follows as;

$$\left.\begin{aligned} G_p(s) &= \frac{1}{1+sT_{amp}} \\ G_{zoh}(s) &= \frac{1-e^{-sT_s}}{sT_s} \\ H(s) &= \frac{1}{1+sT_{aaf}} \end{aligned}\right\} \tag{19}$$

From Fig. 17 and by comparing with the equivalent delay free system, the compensator structure can be derived as;

$$C(s)^* = \frac{1}{1+G_p(s)H(s)G_{zoh}(s)\left(\frac{R_s}{R_h}\right)\left(1-e^{-sT_f}\right)} \tag{20}$$

Comparing (20) with a standard SP controller structure in (17), the SP compensator model can be obtained.

$$C(s) = G_p(s)H(s)G_{zoh}(s)\left(\frac{R_s}{R_h}\right)\left(1-e^{-sT_f}\right) \tag{21}$$

In (21), the presence of exponent representing delays and ZOH makes it difficult to realize it practically. Therefore, (21) needs to be studied further to transform it into a physically realizable form. Looking carefully at (21), ZOH can be understood as the discretization term that converts continuous TF to discrete domain. This term can be eliminated for implementation purposes but is essential during design for checking the Nyquist frequency limit. Further, the exponential delay term can simply be expressed in rational form with PDA. With this, the compensator becomes practically implementable and can be tested for the unstable system of Fig. 16.

The response in Fig. 18 shows a stable Nyquist plot for a compensator employed resistor divider PHIL system of Fig. 15. Also, the time response of this compensator employed network shows a steady state value of 0.4167 (for $R_s = 1.4\,R_h$). This theoretically verifies the use of SP compensator for PHIL application. Further, the compensator will be tested in an actual PHIL application to validate its operation in real time.

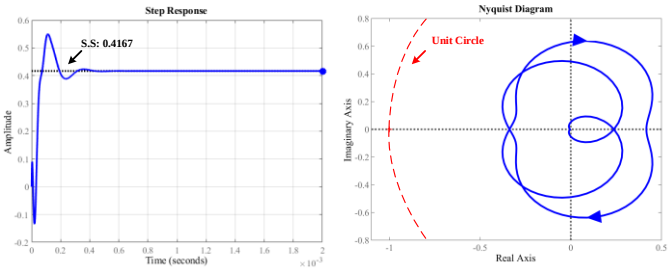


Fig. 18. Response of a PHIL network with a compensator.

To further understand the importance of a compensator employed system a comparison can be made with an equivalent system that represents a compensated system. To make this comparison, a frequency response is plotted overlaying the compensated, uncompensated and an equivalent system for resistor divider network with parameters described to obtain responses in Fig. 16 and Fig. 18.

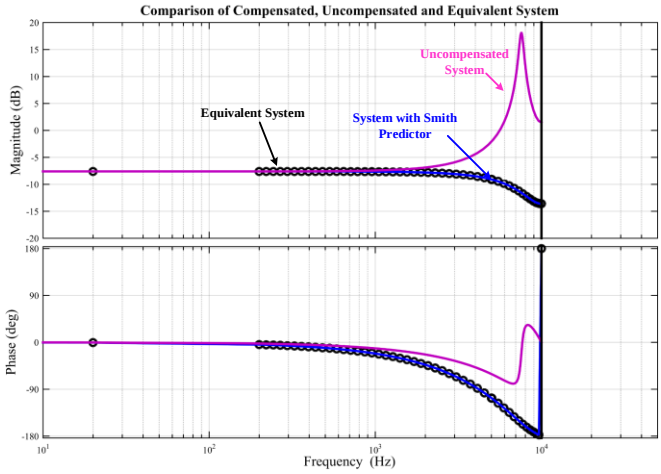


Fig. 19. Frequency response of uncompensated, compensated, and equivalent system.

The closed loop frequency response in Fig. 19 demonstrates that the smith predictor compensator employed system behaves in a manner similar to its equivalent system. This demonstrates the benefit of employing such compensator. The uncompensated system on the other hand experiences a very large gain on the magnitude plot which explains the growing oscillatory response seen in the step response in Fig. 16. Similar results were also observed in the experiments.

V. Experimental Verification of a Compensator Employed PHIL

In Section IV, a detailed procedure for designing a SP compensator to overcome the delay response in a PHIL system was presented. The compensator was tested for an unstable PHIL network to check for any improvement in the stability. Even though the system shows a stable operation in design, it is important to check its operation when employed in a real time system with an actual DUT. Since the application of PHIL in evaluating power electronic converters is popular, this paper follows the trend and presents the experimental validation of compensator to evaluate a PV microinverter. Also, a case study of a resistor divider network is presented to compare with the theoretical predictions.

A. A Case Study of Resistor Divider Network in PHIL

The system of resistor divider network in PHIL is shown in Fig. 14. The compensator is designed based on (20) and implemented in RSCAD using a TF block. With the compensator, the layout of implementation is similar to that of Fig. 17. To test the PHIL of resistor divider network, an AC voltage of 120 V (RMS), 60 Hz is applied at the input resistor in the software end which is transferred to the physical resistor

through interfaces in between. The hardware resistor of 100 Ω is used and the resistance from the software end is varied to check the stability limit for a time step of 50 µs. This is done for both compensated and uncompensated system to highlight the advantage of the SP compensator.

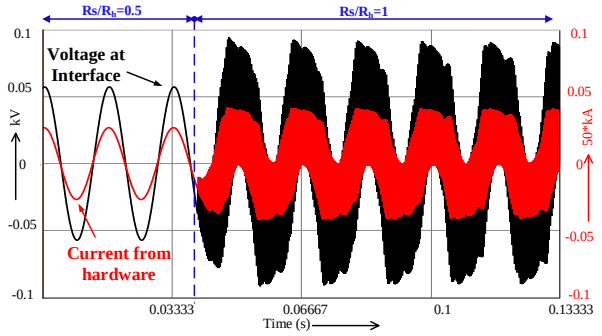
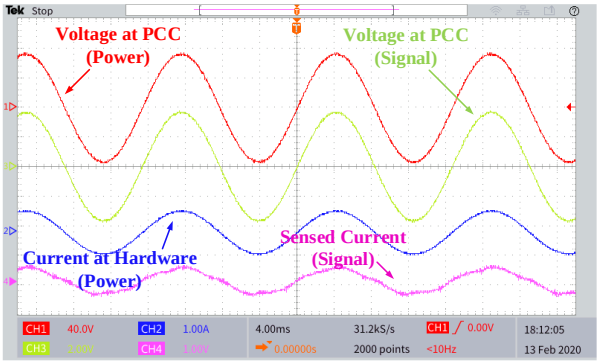
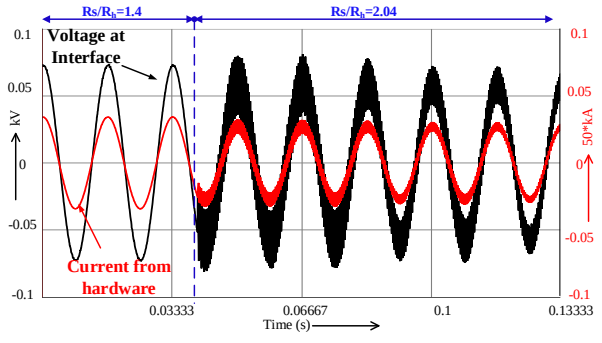


Fig. 20. Uncompensated PHIL result for varying resistances ratio.

The waveforms in Fig. 20 shows the result of a resistor divider network for resistor ratios of 0.5 and 1 for an uncompensated PHIL resistor divider. The input resistance is varied in real time and the system starts to show oscillation when the source and hardware resistances are equal. No further increase in the source resistance is made to avoid any potential damage to the system.



(a)



(b)

Fig. 21. Compensated PHIL result (a) for R_s/R_h=1.4 (b) for increasing R_s/R_h.

Now, a similar set of experiment is repeated with the compensator in the PHIL network. To validate the theoretical response of Fig. 18, the resistor ratio is set to 1.4 and the compensator is implemented with the TF block in RSCAD. As predicted, a stable PHIL is achieved in the real implementation as well. The results are shown in Fig. 21. The experimental result from the hardware side for $R_s/R_h = 1.4$ is presented in Fig. 21 (a) which shows a steady state value of ~0.426. The error compared to the theoretical value is 2.4%. This is acceptable given the fact that actual hardware resistance used has a tolerance of ±5% and the voltage source in software has a small resistance of 1 Ω. With this, it is valid to claim an accurate performance of compensated PHIL. Further, to check the robustness of the system, the resistance ratio is increased until an oscillation is observed. As recorded in Fig. 21 (b), system starts to exhibit an oscillatory response after $R_s/R_h = 2.04$. This proves a robust operation of the compensator as it operates stably to almost 1.5 times its designed value.

B. A Case Study of Evaluating a PV Inverter in PHIL

The evaluation of a grid connected PV inverter requires performing a steady state as well as transient performance during grid voltage change. Additionally, the performance of a PV inverter with weak grid is of particular interest as it comes with problems like, harmonic resonances and control loop interaction as mentioned in [34] and [35].

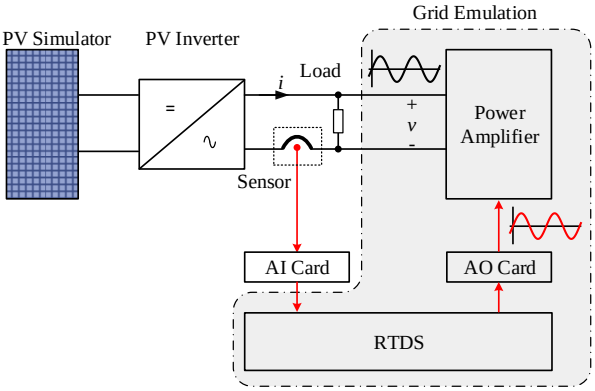


Fig. 22. PHIL architecture of PV inverter evaluation.

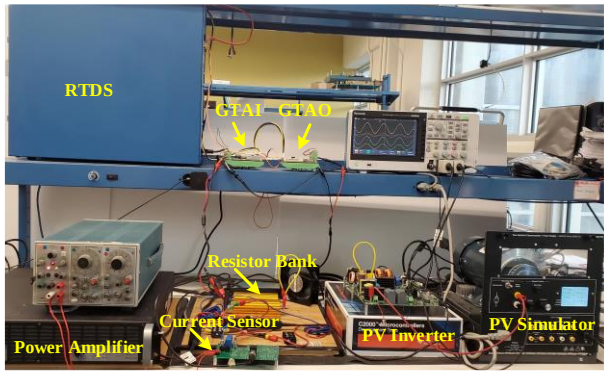
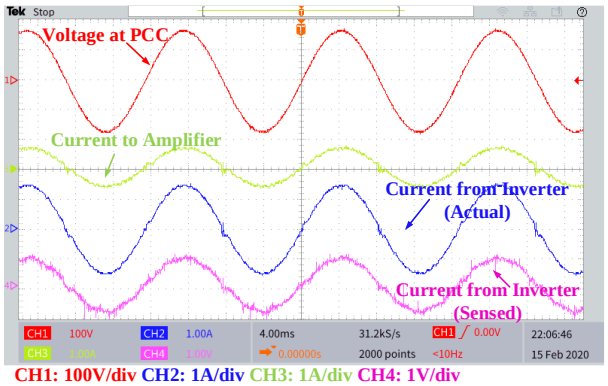


Fig. 23. Experimental set up for PV inverter evaluation in PHIL.

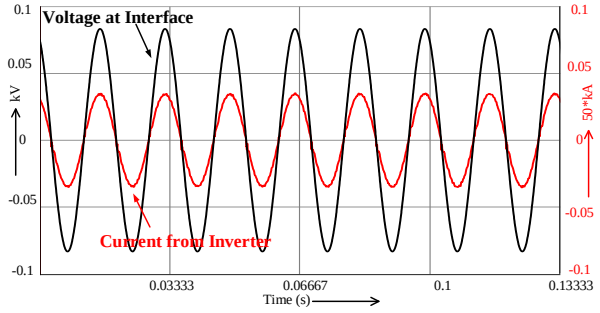
The PHIL scheme for evaluating a PV inverter is shown in Fig. 22. A PV simulator from LabVolt is configured with 4 series and 45 parallel modules (total of 134.5 W maximum power) as an input to the PV micro inverter (TI evaluation board) with L-C-L filter at the output. The grid is emulated inside the RTDS and the amplifier. The PHIL loop is completed with ITM interface. A resistor bank is connected at the point of

common coupling (PCC) of inverter. This resistor helps create a circulating power as well as protects the amplifier from any potential large current surges [21]. Similar setups have been reported in literatures that require the testing of PV inverter for unintentional islanding test in a distributed generation system [36]. The experimental test set up for the system in Fig. 22 is shown in Fig. 23.

Similar to the case study of resistor divider, first a compensator is designed considering the worst-case scenario with $R_s = R_h$. Once the compensator is designed, PV inverter can now be tested with stiff and weak grid conditions. The Stiff Grid (SG) is emulated in the RSCAD with a voltage source in series to a small resistance while the Weak Grid (WG) is emulated with inductor in series to a voltage source.



(a)

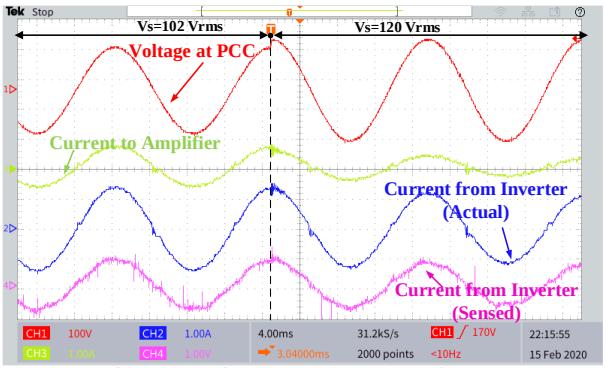


(b)

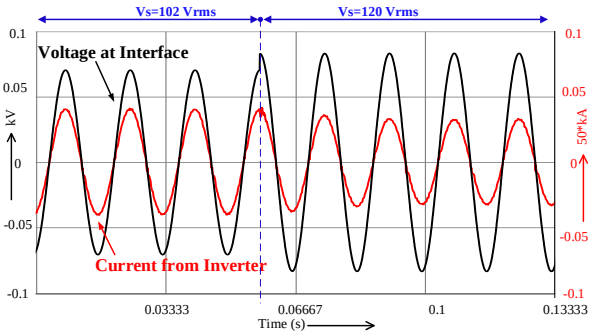
Fig. 24. PV inverter steady state results with stiff grid (a) measurement at inverter (b) measurement at software node.

The steady state performance of PV inverter in PHIL with SG is presented in Fig. 24. The measurements are made at the inverter end as well as at the corresponding node in the software. During steady state, the PV with maximum power point tracking (MPPT) enabled showed delivering 134.5 W. At the inverter end, it showed 125.69 W delivered to the grid out of which 75 W is consumed by the resistor bank and remaining is sink-in by the amplifier. It is due to this reason, for PHIL applications, selection of amplifier is crucial and therefore a 4-quadrant amplifier is necessary. The steady state performance of PV inverter in PHIL showed an efficiency of 95.15% which accounts for losses in the converter as well as in the voltage source resistors.

Similarly, PV inverter is tested during grid transient of 15% voltage swell (102 V_{rms} to 120 V_{rms}). The result is presented in Fig. 25. As expected, the PV inverter responds to voltage swell by lowering the current to the grid to maintain the power. This is the result of maximum power point regulating the power at the inverter end. The result showing this phenomenon at the software environment is presented in Fig. 25 (b).



(a)



(b)

Fig. 25. PV inverter during voltage swell with stiff grid (a) measurement at inverter (b) measurement at software node.

Further, the PV inverter is tested with WG to evaluate its performance during steady state and transients. The steady state performance of PV inverter showed 123.45 W delivered to the grid against an input power of 134 W from the PV. The loss of 10.55 W (efficiency of 92.1%) accounts for converter losses, PHIL inaccuracies and the effect of additional grid inductance in the current controller of the inverter. As also mentioned in [35], the current control of the PV inverter needs to incorporate the active damping scheme to damp out the harmonic resonances to achieve a superior current control scheme. The PV inverter under study lacks the active damping on its current controller and therefore it is expected to have a detrimental effect on the current waveform as the strength of the grid reduces. This can also be observed in the experimental results of Fig. 26.

In Fig. 26 (c), the PV inverter is operating in a weak grid emulated by connecting an inductor in series with the grid and the grid transients are also emulated to create a voltage swell. Even during this scenario, the PHIL is able to operate stably to evaluate the inverter. The plots at software node during the steady state and grid transient operating on a weak grid is also presented in Fig. 26 (b) & (d) respectively. This scheme with PHIL allows systems engineer to evaluate the PV inverter under various scenarios of the grid which will aid to design and test an actual power electronic renewable converter in a laboratory

set up and the results obtained would reflect an actual like phenomena. Since an actual hardware is reacting to the grid, the results obtained from such tests would benefit in understanding the effect of such power electronic converters in a real grid.

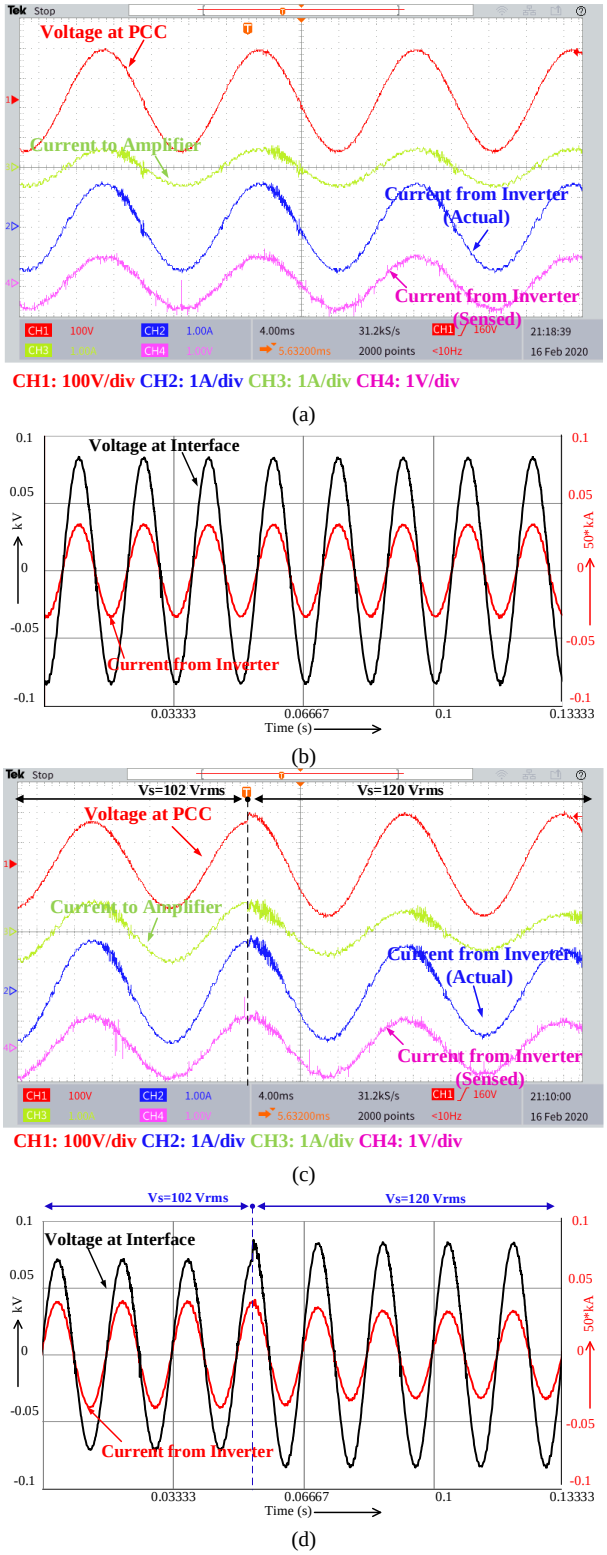


Fig. 26. PV inverter with weak grid (a) steady state measurements at inverter (b) steady state measurements at software node (c) transient measurements at inverter (d) transient measurements at software node.

VI. Discussion: SP Compensator with Impedance

To highlight the benefit of SP compensator experiments were provided in Section V of this paper. The analysis to show the rationale behind SP compensator's effectiveness with the presence of grid impedance required further investigation. In this context, first a mathematical model of the DUT (PV inverter) is required which is always not an easy task to determine as it may be a black box. Therefore, in this paper the output impedance of the grid connected inverter is measured and the transfer function is estimated from the measured data. The impedance plot in Fig. 27 shows the output impedance of a grid connected PV inverter estimated with a second order system.

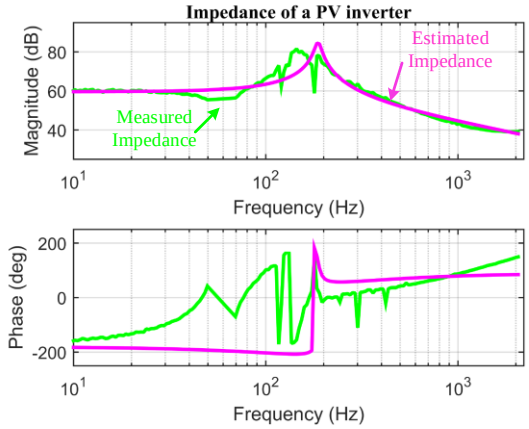


Fig. 27. PV inverter Output impedance measured and estimated.

With the DUT model known and the SP controller synthesized based on the worst-case scenario of $R_s = R_h$, as mentioned in Section V, the step response of the PHIL system in the presence of grid impedance (inductor and resistor combination) can show the effectiveness of the controller. The time response in Fig. 28 for of an uncompensated system shows an oscillatory behavior while the compensator employed system shows a stable operation. This validates the stable operation of PV inverter with SP compensator.

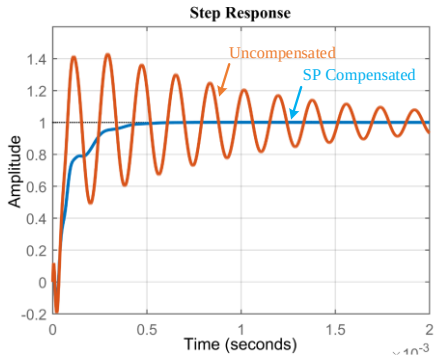


Fig. 28. Time response of uncompensated and compensated system in the presence of grid impedance.

VII. Conclusion

This paper presented a comprehensive model of ITM interface along with their experimental verifications. The developed model was further utilized to propose a smith

predictor-based compensator for PHIL applications. The detailed design procedure along with the stability improvement of PHIL network with the proposed compensator was presented. The theoretical as well as the experimental verifications were made to highlight the performance of the proposed compensator. To validate the superior performance of the compensator, a PHIL set up was used to evaluate a linear as well as a non-linear DUT. A resistor divider network in PHIL was used as the case study to validate the operation of compensator with linear load. Similarly, a grid connected PV inverter was evaluated with a compensator employed PHIL. Finally, the experimental results were presented which showed a good agreement with the theoretical predictions. Similar approach can be followed with the use of a switched mode amplifier which becomes the choice of amplifier for evaluating a high-power PHIL. Moreover, it is important to select an amplifier with bandwidth high enough to emulate the transients within the system

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