Comprehensive study and performance evaluation of an interleaved GaN-based PFC with magnetic component size reduction

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***Abstract*—Power factor correction (PFC) converters can be significantly reduced in size by integrating control circuits, sensing circuits, gate drivers, and power switches. However, magnetic components are the main parts that are bulky and prevent further PFC size reduction. Recently, a highly integrated commercial PFC called Gallium Nitride-controller module (GaN-CM) was introduced which employs a novel controller in discontinuous conduction mode (DCM) to reduce the size of the boost inductor. The question remains, however, of how to quantify the inductor size reduction while maintaining high efficiency. Moreover, the power rating of GaN-CM is up to 240W with a single module operation. In this paper, steady-state analysis, loss analysis, and inductor optimization of GaN-CM are conducted to show how DCM PFC can lead to a small inductor with high efficiency. Furthermore, GaN-CM interleaving is proposed to increase the power rating of GaN-CM. The proposed interleaved PFC is verified by a 400W prototype with an advanced GaN transistor.**

***Index Terms*—Power factor correction, Discontinuous conduction mode (DCM), interleaving, gallium nitride.**

I. Introduction

POWER Factor Correction (PFC) converters are the front-end stage of grid-connected and offline converters. The boost PFC topology is widely used in low-power applications like laptop chargers, tools chargers, and TVs due to its cost-effectiveness and simple controller implementation. The converter has three operation modes, i.e., continuous conduction mode (CCM), critical conduction mode (CRM), and discontinuous conduction mode (DCM). CCM has smaller current ripple by applying higher switching frequency or a larger boost inductor. Therefore, the smaller current ripple leads to lower turn-OFF switching loss although the turn-ON switching loss and diode reverse recovery are inevitable. In contrast, CRM and DCM have intrinsic zero-current switching (ZCS) turn-ON which can use a low-cost diode. Moreover, a smaller boost inductor can be achieved by CRM and DCM since the current ripple is higher than CCM [1].

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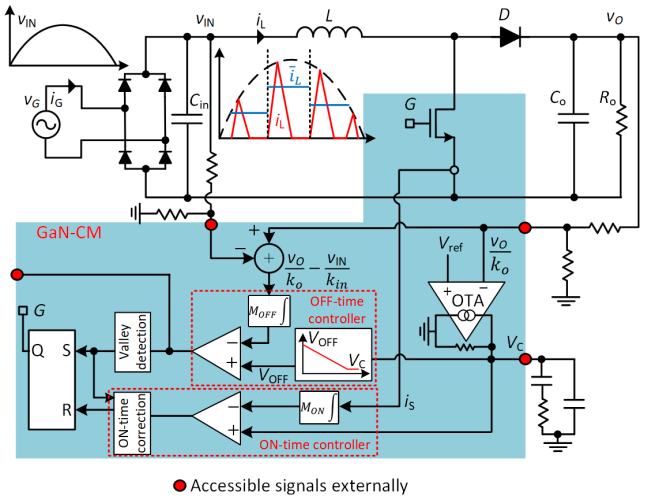

Fig. 1. GaN-CM block diagram.

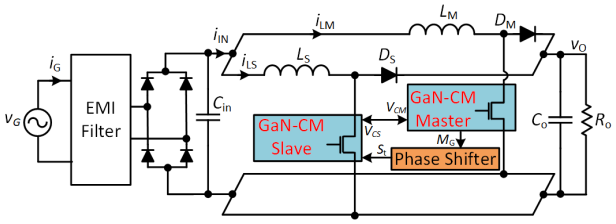

Fig. 2. Proposed interleaved PFC based on GaN-CM.

In low-power applications, CRM with the voltage-mode controller is preferred since it does not need current sensing and a fast diode [2]. CRM has an inherent variable switching frequency in a parabolic form with its minimum switching frequency at peak of input voltage and its maximum switching frequency at near zero crossing of input voltage. The ratio between the maximum and minimum switching frequencies varies from 1.5 at low-line input voltage 90 Vac to 33 at high-line input voltage 265 Vac [3]. Therefore, to achieve acceptable efficiency in CRM, the minimum switching frequency should be limited to avoid high switching loss near the zero crossing. On the other hand, the minimum switching frequency determines the boost inductance to maintain CRM. As a result, the compromise between efficiency and boost

inductor size restricts the size reduction of the boost inductor in CRM. To suppress the large variation of the conventional CRM switching frequency, the switching frequency limit technique is applied [3]. However, this method leads to a distorted input current. Alternatively, switching frequency can be kept constant by applying the variable ON-time technique [4]. Although the method overcomes the large variation of switching frequency and improves the efficiency, peak current, and output voltage ripple, the boost inductance is required to vary depending on the input voltage. Moreover, power factor (PF) drops significantly. Therefore, fixed switching frequency in CRM does not seem a practical solution. Instead of either suppressing switching frequency or keeping it constant, an optimal switching frequency variation range is derived in which the switching frequency variation is minimized [5]. The method achieves a quasi-constant switching frequency with higher PF compared to the fixed frequency in [4] with low PF. Nevertheless, the quasi-constant switching frequency needs to be implemented by a digital signal processor (DSP) which increases converter costs for low-power applications.

On the contrary, DCM operates inherently at a fixed switching frequency and duty cycle. Therefore, inductor size is smaller at the cost of high inductor peak current with large turn-off loss which leads to low efficiency, especially with Silicon (Si) MOSFET. Moreover, distorted input current and low PF at high-line voltages are other disadvantages of DCM with fixed switching frequency and duty cycle. To increase PF to unity, variable duty cycle is used [6] which is approximated by Taylor's expansion. However, the approximation error increases with the increase of the input voltage which leads to high distortion of input current and low PF. To reduce the high inductor peak current, third and fifth-order harmonics are injected into duty cycle to increase the boundary inductance [7]. Therefore, larger inductance can be used while maintaining DCM operation. The method could decrease the inductor peak current, but it is computationally heavy and needs to be implemented by a DSP. Alternatively, DCM can be applied with wide-bandgap (WBG) semiconductors like Gallium Nitride (GaN) to reduce the switching loss; however, gate driver and PCB design are challenging with GaN transistors due to high current and voltage slew rate.

Given pros and cons, DCM and CRM have been manufactured in commercial integrated circuits [8]–[10]. Among them, a GaN Controller Module (GaN-CM), i.e., HiperPFS-5, offers a DCM boost PFC with high efficiency and small inductor size [10]. In fact, GaN-CM uses two novel methods to overcome low efficiency and large inductor size of conventional DCM PFC. Firstly, it utilizes a 750V GaN transistor to minimize the switching turn-off loss as well as ON resistance. GaN transistor is integrated into a small package which includes a gate driver, a controller, and sensing circuits. This integration minimizes the effects of parasitic inductance and capacitance, eliminates the need for a heatsink, and enables straightforward PCB design. Secondly, it uses a novel control methodology with a variable switching frequency which gives the maximum and minimum switching frequencies at peak and near zero crossing of input voltage, respectively. Therefore, increasing switching frequency does not lead to high switching frequency near the zero crossing, unlike CRM PFC. However, the power rating of GaN-CM is up to 240W with a single module operation. Thus, the power rating of GaN-CM can be increased by current sharing techniques like interleaving. Nonetheless, GaN-CM interleaving is challenging since it has variable ON-time and OFF-time. Therefore, if there is a phase shift error between interleaved GaN-CMs, one of the inductor current will be unstable due to violating the volt-second balance. Moreover, GaN-CM is highly integrated and most of the control signals are neither accessible nor can be manipulated.

This paper studies GaN-CM controller to illustrate how utilizing a GaN transistor in DCM PFC leads to enhanced efficiency and small inductor size when compared to CRM PFC. The study involves deducing and evaluating the operational principles and steady-state characteristics of GaN-CM, providing insights beyond those offered by the manufacturer. Additionally, the paper delves into loss analysis and inductor optimization for GaN-CM. Furthermore, an interleaving method, shown in Fig. 2, is proposed to increase the power rating of GaN-CM. The proposed method employs a conventional phase shifter along with an internal controller of GaN-CM to overcome unstable inductor current. Therefore, stable inductor currents are guaranteed. Moreover, the proposed interleaved PFC leads to balanced current sharing between interleaved GaN-CMs by averaging the outputs of the voltage loop controller. The averaging is done by a simple external connection without needing to change internal circuits. The proposed interleaved PFC is verified by a 400W prototype.

The contributions of this paper are summarized as follows:

- Elaboration on the operational principles of GaN-CM
- Comprehensive derivation of the steady-state characteristics of GaN-CM
- Optimization of GaN-CM inductor to enhance efficiency
- Proposing an interleaving method to increase the power rating of GaN-CM

II. Steady-state Characteristic

A. GaN-Controller Module

GaN-CM, illustrated in Fig. 1, utilizes two control rules: constant amp-second ON-time and constant volt-second OFF-time. By integrating the switch current and controlling it to maintain a constant product of amp-seconds throughout the ON-time of the switch, the average inductor current $\bar{i}_L$ can effectively follow the input voltage v_{IN}. Additionally, integrating the difference between the output and input voltages ensures a consistent volt-second equilibrium determined by the electromagnetic characteristics of the boost inductor. Consequently, this control rule regulates both the output voltage and power. In the subsequent equations, the average variables are assumed to remain constant over a few switching cycles while being time-varying within a line cycle. The constant amp-second ON-time and constant volt-second OFF-time rules are defined as follows, respectively:

$$\bar{i}_L \times t_{ON} \approx K_2. \tag{1}$$

$$(V_O - v_{IN}) \times t_{OFF} = K_1, \tag{2}$$

where K_1 and K_2 are constants, V_O is DC output voltage, v_{IN} is the rectified input voltage, and t_{ON} and t_{OFF} are ON-time and OFF-time periods, respectively. To maintain the volt-second equity during ON-time and OFF-time, the ON-time is controlled such that:

$$v_{IN} \times t_{ON} = K_1 \tag{3}$$

Substituting t_{ON} from (3) into (1) gives:

$$\bar{i}_L = \frac{K_2}{K_1} \times v_{IN}, \tag{4}$$

The relationship of (4) demonstrates that by controlling the constant amp-second ON-time and constant volt-second OFF-time, the average inductor current $\bar{i}_L$, which is equal to the rectified grid current, is proportional to input voltage v_{IN}, satisfying the fundamental requirement for PFC.

At the end of volt-second integration for the OFF-time, the controller waits for the valley of Drain voltage, and turns on the switch at the valley. This is achieved by the valley detection block, shown in Fig. 1, to minimize turn-ON loss associated with C_{oss}, parasitic capacitance of the boost switch. In order to compensate for this delay, GaN-CM measures the difference between desired OFF-time ($t_{OFF,d}$) and real OFF-time ($t_{OFF,r}$), shown in Fig. 3. The controller then adjusts the next ON-time period to account for this difference. This ON-time correction ensures the same average current in each switching cycle. Switch current i_s which is equal to the inductor current i_L during ON-time is obtained by:

$$i_s(t) = \frac{v_{IN}}{k_{in}L} t. \tag{5}$$

where k_{in} is the resistor divider gain of the input voltage, and L is the boost inductor. Integration of the switch current during ON-time is expressed by

$$M_{ON} \int_0^{t_{ON}} i_s(t)\, dt = M_{ON} \frac{v_{IN}}{2Lk_{in}} t_{ON}^2 = V_C. \tag{6}$$

where M_{ON} is a current-sense gain and V_C is the output voltage of the operational transconductance amplifier (OTA), shown in Fig. 1. By simplifying (6), t_{ON} is derived as

$$t_{ON} = \sqrt{\frac{2Lk_{in}V_C}{M_{ON}v_{IN}}}. \tag{7}$$

Integration of the difference between output and input voltages is described by

$$M_{OFF} \int_0^t (\frac{V_O}{k_o} - \frac{v_{IN}}{k_{in}})\, dt = M_{OFF}(\frac{V_O}{k_o} - \frac{v_{IN}}{k_{in}})t, \tag{8}$$

where k_o is the resistor divider gain of the output voltage, and M_{OFF} is a scaling factor. The integration in (8) resets to zero when it reaches V_{OFF}, corresponding to $t_{OFF,d}$ according to Fig. 3. Therefore, $t_{OFF,d}$ is obtained from (8)

$$t_{OFF,d} = \frac{V_{OFF}}{M_{OFF}(\frac{V_O}{k_o} - \frac{v_{IN}}{k_{in}})}. \tag{9}$$

Since the controller waits for the valley of Drain voltage, $t_{OFF,d}$ may not describe the real OFF-time. Therefore, $t_{OFF,r}$ is given by

$$t_{OFF,r} = t_z + t_v, \tag{10}$$

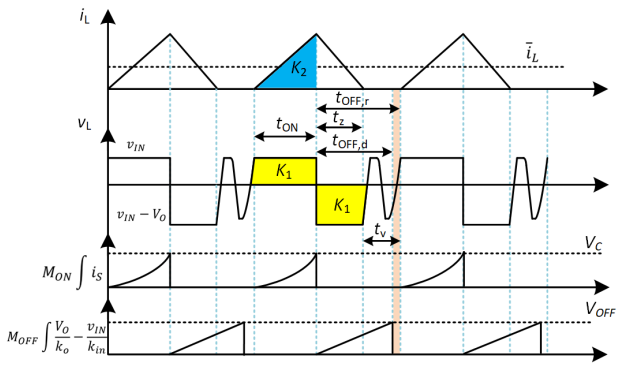

Fig. 3. GaN-CM key waveforms.

where t_z is the time that inductor current takes to reach zero and is defined as

$$t_z = \frac{i_{L,peak}L}{V_O - v_{IN}}, \tag{11}$$

and t_v is the valley time which can either be estimated [11] or measured in simulation software. Using (7) and (10), switching frequency is defined as

$$f_{sw} = \frac{1}{t_{ON} + t_{OFF,r}}. \tag{12}$$

Moreover, duty cycle is obtained by

$$D = \frac{t_{ON}}{T_{sw}}. \tag{13}$$

By knowing t_{ON} in (7), inductor peak current is expressed by

$$i_{L,peak} = \frac{v_{IN}t_{ON}}{L}. \tag{14}$$

The boost inductor is designed in a way that achieves CRM operation at full load and low-line voltage with a phase angle of $\omega t = \pi/2$. Therefore, the boundary boost inductance is given by

$$L = \frac{V_m^2}{4P_O f_{sw,\omega t=\pi/2}} D_{min}. \tag{15}$$

where V_m is the peak of input voltage, P_O is the output power, and D_{min} is the minimum value of duty cycle determined by (13).

B. Conventional CRM

The steady-state characteristics of the conventional CRM are well studied and expressed in the literature [4], and here key relationships are mentioned. The conventional CRM with voltage-mode control has constant ON-time which is defined in the following

$$t_{ON} = \frac{4LP_O}{V_m^2}. \tag{16}$$

Moreover, duty cycle and switching frequency are expressed as, respectively,

$$D(t) = 1 - \frac{v_{IN}(t)}{V_O}, \tag{17}$$

$$f_{sw}(t) = \frac{D(t)}{t_{ON}} = \frac{V_m^2}{4LP_O}(1 - \frac{V_m}{V_O} sin(\omega t)), \tag{18}$$

TABLE I
POSSIBLE OPERATING POINTS FOR CRM AND DCM

Operating points	L (μH)	$f_{\min}$ (kHz)	$f_{\max}$(kHz)	f_{avg} (kHz)
Opt1-CRM	458	30	44.2	35.1
Opt2-CRM	343	40	58.9	46.9
Opt3-CRM	275	50	73.5	58.6
Opt4-CRM	229	60	88.3	70.3
Opt1-DCM	140	22	77.8	82
Opt2-DCM	100	22	78.3	67.9

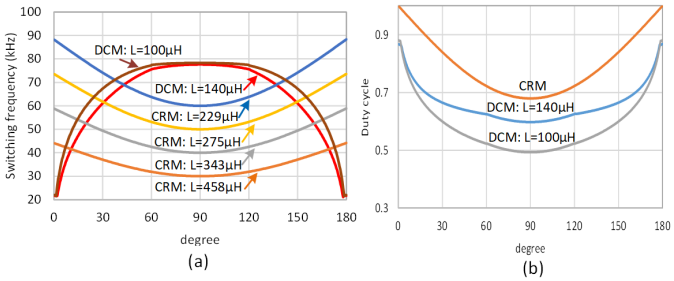

Fig. 4. Steady-state characteristic evaluation: (a) switching frequency (b) duty cycle.

C. Steady-state Characteristic Evaluation

Various possible operating points in CRM and DCM, listed in Table I, are selected based on the steady-state characteristics and system specifications listed in Table II. The switching frequencies of the operating points listed in Table I are depicted in Fig. 4(a). According to Fig. 4(a), CRM and DCM have opposite switching frequency trends in which DCM has its maximum switching frequency at 90° while CRM has its minimum switching frequency at 90°. Increasing the minimum switching frequency in CRM leads to a smaller inductor, according to (15); however, it also increases switching loss near zero crossing of the input voltage. On the contrary, the DCM has the opposite trend in which switching frequency decreases from 90° up to the zero crossing of the input voltage. DCM achieves almost the same switching frequency at 90° for two different inductor values. However, it is expected that the smaller inductor leads to a higher switching frequency at 90° since a smaller inductor leads to smaller t_{ON} (7) and t_{z} (11). Nevertheless, switching frequency in DCM is not only determined by t_{ON} and t_{z}, and t_{v} also affects switching frequency, shown in Fig. 3. In this case, t_{v} of the smaller inductor is longer than t_{v} of the larger inductor. Therefore, the smaller t_{ON} and t_{z} are offset by longer t_{v}. Thus, t_{v} is not fixed, and it changes to ensure that the switch turns ON at the valley of Drain voltage. Duty cycle of both CRM and DCM are shown in Fig. 4(b). It shows that all of the CRM operating points have the same duty cycle curve since it is determined by (17) which is only the function of the input voltage. However, DCM duty cycle curve changes for different operating points since it is based on variable t_{ON}.

III. LOSS MODEL

A. Semiconductor Loss Breakdown

In the boost PFC topology, the semiconductor loss breakdown includes switching loss, boost diode loss, and diode bridge loss [12]. The switching loss accounts for conduction loss and turn-OFF loss which are expressed in the following, respectively,

$$P_{con,s} = i_{S,RMS}^2 R_{ds,on}, \tag{19}$$

$$P_{off} = \frac{1}{n}\sum_{i=1}^{n} E_{off}(i_{L,peak}(n)) f_{sw,avg}, \tag{20}$$

where $i_{\text{S,RMS}}$ is the switch RMS current, $R_{\text{ds,on}}$ is the *ON*-state resistance of the switch, n is the sampling points during half line cycle, E_{off} is energy loss during switch turn OFF, and $f_{\text{sw,avg}}$ is the average switching frequency. Moreover, the conduction loss of the boost diode is described as

$$P_{con,d} = i_{D,RMS}^2 R_f + i_{D,avg} V_f, \tag{21}$$

where $i_{\text{D,RMS}}$, $i_{\text{D,avg}}$, R_{f}, and V_{f} are diode RMS current, diode average current, diode forward resistance, and diode forward voltage drop, respectively. Finally, the diode bridge loss is obtained by

$$P_{bridge} = 2(i_{IN,RMS}^2 R_f + i_{IN,avg} V_f), \tag{22}$$

where $i_{\text{IN,RMS}}$ is RMS value of input current ripple, and $i_{\text{IN,avg}}$ is average value of input current. Thus, total semiconductor loss is

$$P_{ts} = P_{con,s} + P_{con,d} + P_{off} + P_{bridge}. \tag{23}$$

B. Inductor Loss Breakdown

Inductor losses include copper loss and core loss [1]. The copper loss is contributed by DC and AC components of the inductor current. Due to the proximity and skin effects, DC and AC components of the inductor current see different resistances which are characterized by R_{DC} and R_{AC} [13], respectively. Therefore, the copper loss is expressed as

$$P_{copper} = i_{L,DC}^2 R_{DC} + i_{L,RMS}^2 R_{AC}, \tag{24}$$

where $i_{\text{L,DC}}$ is DC component of the inductor current and $i_{\text{L,RMS}}$ is RMS value of AC component of the inductor current.

The core loss is expressed as

$$P_{core} = a f_{sw}{}^b B_{ac}{}^c V_e, \tag{25}$$

where B_{ac} is the flux density and V_{e} is the core volume. Total inductor loss is

$$P_{tm} = P_{copper} + P_{core}. \tag{26}$$

TABLE II
SYSTEM SPECIFICATIONS FOR A SINGLE MODULE

Parameters	Values	Parameters	Values
P_{o}	200 W	V_{in}	90 Vrms
V_{o}	397 V	f_{grid}	50 Hz

IV. OPTIMUM OPERATING POINT SELECTION

To determine the optimum operating points in Table I, inductor design optimization and loss analysis are conducted in the following. Finally, optimum operating points in CRM and DCM are compared to determine which one achieves a smaller inductor size and higher efficiency.

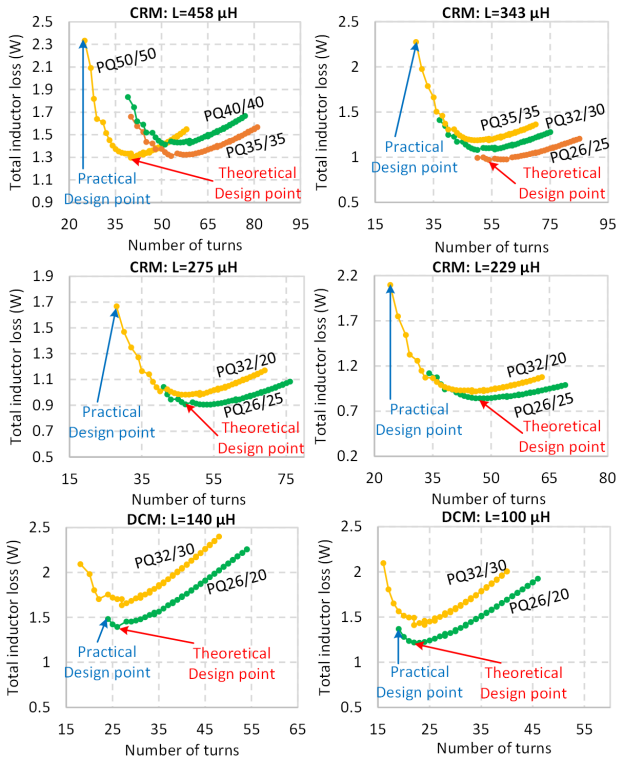

Fig. 5. Inductor design curves.

TABLE III
PARAMETERS OF THE PRACTICAL INDUCTOR DESIGN POINTS

Operating points	L (μH)	Core	air gap (mm)	N	P_{tm}
Opt1-CRM	458	PQ50/50	0.6	25	2.33
Opt2-CRM	343	PQ35/35	0.6	29	2.27
Opt3-CRM	275	PQ32/20	0.6	28	1.66
Opt4-CRM	229	PQ32/20	0.5	24	2.09
Opt1-DCM	140	PQ26/20	0.7	24	1.48
Opt2-DCM	100	PQ26/20	0.6	19	1.37

A. Inductor Design Optimization

Each operating point, listed in Table I, has a different inductance value. Therefore, inductor design optimization is required for all the operating points. To this end, Ferrite core with PQ shape and PC95 material from TDK are used. The cores offer high flux density saturation of 0.41 T at 100 °C. Also, its round pole shape helps to reduce the wire length and copper loss. The number of turns is determined by

$$N = \sqrt{\frac{L}{A_L(l_g)}} \tag{27}$$

where A_L is the nominal inductance and function of air gap length l_g. Therefore, different values of air gap result in different values of N. Hence, air gap is a control parameter to achieve a compromise between number of turns and total inductor loss P_{tm}. To this end, various cores with different air gaps are evaluated for each operating point, and the results are shown in Fig. 5. According to the results, there are two design points, i.e., theoretical design point and practical design point. The theoretical design point gives the lowest P_{tm}; however, it may lead to a large air gap which generates extra power losses and a rise in the conductor temperature due to the air gap fringing flux [14]. Therefore, the practical design point is used which gives the shortest air gap and the minimum number of turns and may not lead to the lowest P_{tm}. The parameters of the practical design points are summarized in Table III. It shows that DCM operating points achieve a smaller core and the lowest P_{tm} compared to CRM operating points.

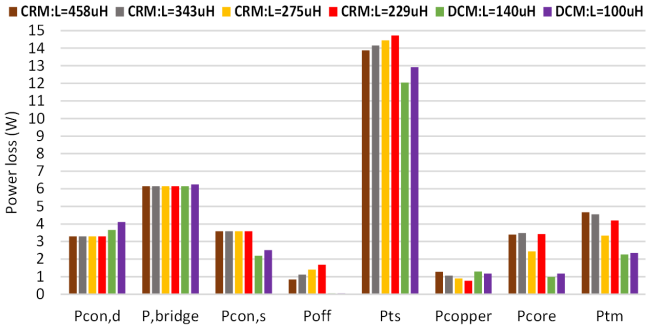

Fig. 6. Loss breakdown analysis of the proposed PFC (DCM) and CRM PFC at 90Vac-400W.

B. Loss Breakdown Analysis

The loss breakdown analysis, including semiconductor loss and inductor loss, is conducted at 90Vac-400W for CRM with Si MOSFET and DCM with GaN transistor, shown in Fig. 6. Moreover, the semiconductors used in the analysis are mentioned in Table IV. The boost diode conduction loss $P_{con,d}$ is determined by diode average and RMS currents. The diode average current is the same for both CRM and DCM while DCM has higher diode RMS current. Therefore, $P_{con,d}$ is higher in DCM around 0.8 W in the worst case. Although DCM has higher switch RMS current, its lower $R_{ds,on}$ leads to lower $P_{con,s}$ compared to CRM. Diode bridge loss is mainly affected by the average of the input current since the effect of the input current ripple is negligible, due to ripple cancellation achieved by the interleaving. Therefore, the diode bridge loss is almost the same for CRM and DCM. Turn-OFF loss is affected by inductor peak current and average switching frequency according to (20). The turn-OFF loss increases in CRM as the inductance decreases since average switching frequency is increasing while inductor peak current is kept constant. In DCM, turn-OFF loss is assumed to be zero due to utilizing GaN transistor. According to Fig. 6, DCM with GaN transistor achieved lower total semiconductor loss P_{ts} compared to CRM with Si MOSFET. The other important loss contributor is the inductor loss consisting of the copper loss and the core loss. The copper loss is determined by both DC and AC components of the inductor current. DC component is the same for both CRM and DCM while DCM has higher $i_{L,RMS}$. However, higher value of $i_{L,RMS}$ in DCM does not necessarily lead to higher P_{copper}. For instance, DCM with L=140 μH has the same P_{copper} as CRM with L=458 μH. The reason is that CRM with L=458 μH has a higher number of turns and a biger core resulting in higher mean turn length (MTL) of wire. Consequently, R_{DC} increases and offsets lower $i_{L,RMS}$ in CRM, leading to the same P_{copper} as

TABLE IV
SEMICONDUCTOR USED FOR LOSS ANALYSIS

Diode bridge	Boost Diode	Si MOSFET	GaN transistor
GBU8kK-BP	STTH3R04S	SPW20N60C3 $R_{ds,on}$=0.375Ω	PowiGaN $R_{ds,on}$=0.18Ω

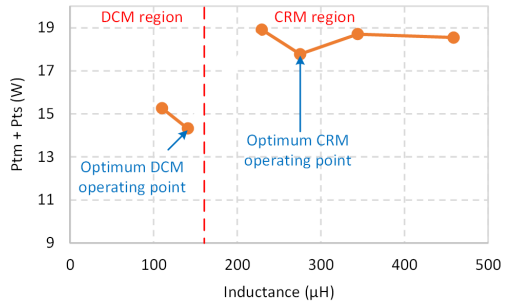

Fig. 7. Optimum operating point selection curve.

of DCM. Furthermore, DCM shows significantly lower core loss compared to CRM which mainly stems from the fact that DCM requires smaller core, according to Table III. As expected, DCM achieved lower total inductor loss compared to CRM.

C. Operting Points Optimization

By conducting the inductor optimization and the loss breakdown analysis, the optimum operating point which gives the smallest core and the lowest loss can be determined. To this end, total power loss which is the sum of the total inductor loss and the total semiconductor loss is plotted versus inductance values, shown in Fig. 7. Based on the inductance values, the graph is divided into DCM and CRM regions. In CRM region, the optimum operating point is Opt3-CRM with L=275 μH, shown in Table III. In DCM region, the optimum operating point is OPt1-DCM with L=140 μH, shown in Table III. Therefore, the optimum DCM operating point achieves not only a smaller inductor but also lower power loss.

V. PROPOSED INTERLEAVED PFC

The superiority of GaN-CM over the conventional CRM has already been proved by analytical analyses. GaN-CM uses a smaller inductor and has lower power loss. However, the power rating of GaN-CM is up to 240 W with a single module operation. Therefore, two GaN-CM are interleaved as Master and Slave modules according to the block diagram shown in Fig. 2 where L_M=L_S=140μH and C_{in}=1μF. There are two challenges with GaN-CM interleaving. Firstly, GaN-CM is highly integrated, and most of the internal control signals either are not accessible or cannot be manipulated. For instance, there are two OTAs in parallel when two GaN-CMs are interleaved, shown in Fig. 8. Since OTAs do not have exactly equal gains, one of them is faster than the other. Therefore, the faster OTA leads to higher current sharing in the corresponding module, and unbalanced current sharing will happen between Master and Slave modules. OTAs output cannot be disconnected internally to only have one OTA.

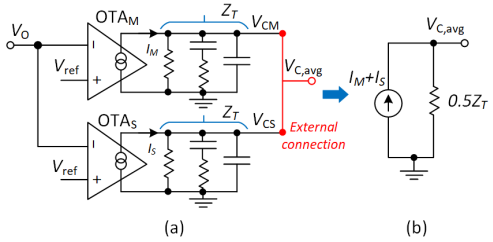

Fig. 8. Paralleled OTAs: (a) actual model (b) simplified model.

However, OTAs outputs are accessible externally. Therefore, if they are connected externally, as shown in Fig. 8(a), OTAs outputs are averaged (28), as shown in the simplified model in Fig. 8(b). Thus, the average value of OTAs outputs leads to balanced current sharing between Master and Slave modules.

$$V_{C,avg} = \frac{V_{CM} + V_{CS}}{2} = \frac{I_M + I_S}{2} Z_T, \tag{28}$$

where

$$V_{CM} = I_M Z_T, V_{CS} = I_S Z_T. \tag{29}$$

The second consideration is how to connect the phase shifter between Master and Slave modules. Master module works stand-alone while Slave module is shifted in phase by 180°. The input of the phase shifter is Master gate signal, and its output should either be connected to Reset or Set of the slave latch. The former and the latter require disabling the ON-time and OFF-time controllers, respectively, shown in Fig. 1. ON-time controller includes ON-time correction, explained in Section II.A, to maintain average current. Therefore, the ON-time correction will be canceled if ON-time controller is disabled. The lack of ON-time correction will lead to an unstable inductor current. Thus, disabling ON-time controller is not a practical solution for GaN-CM interleaving. As a result, the only option in GaN-CM interleaving is to disable OFF-time controller to keep ON-time correction. Therefore, the stable operation of the GaN-CM interleaving is guaranteed. The phase shifter is implemented according to Fig. 9(a). It employs two edge detectors to create short pulses on the rising edges of Master gate signal M_G and output of the comparator *CMP*. A current source charges a capacitor to form a ramp signal which is locked on M_G, shown in Fig. 9(b). A sample-and-hold is used to save the peak value of the ramp signal which corresponds to Master switching period, and its half value V_S corresponds to 180°. Therefore, a resistor divider along with a comparator is used to obtain 180° phase shift. Finally, S_t signal obtained from the rising edge of *CMP* turns ON Slave module at 180° phase shift with respect to Master module. The input current ripple Δi_{IN} for two interleaved GaN-CMs is shown in Fig. 10. Since t_{ON} is variable, Δi_{IN} is derived based on t_{ON} relation with T_{sw}/2. Therefore, the upper and lower boundaries of Δi_{IN} are described as

$$i_{IN}{}^{+} = \begin{cases} i_{L,peak} + i_{L,r}(t_x) & t_{ON} \geq T_{sw}/2 \\ i_{L,peak} & t_{ON} < T_{sw}/2 \ \& \ t_{ON}+t_z \geq T_{sw}/2 \\ i_{L,peak} & t_{ON}+t_z < T_{sw}/2 \end{cases} \tag{30}$$

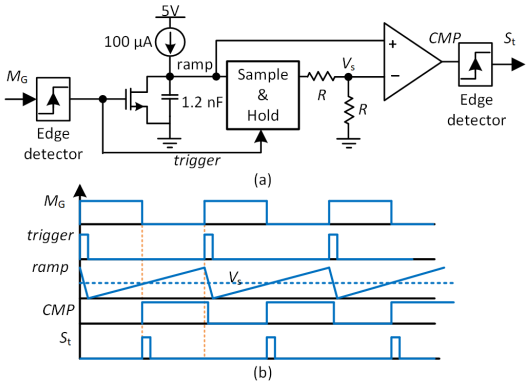

Fig. 9. Phase shifter: (a) block diagram (b) key waveforms.

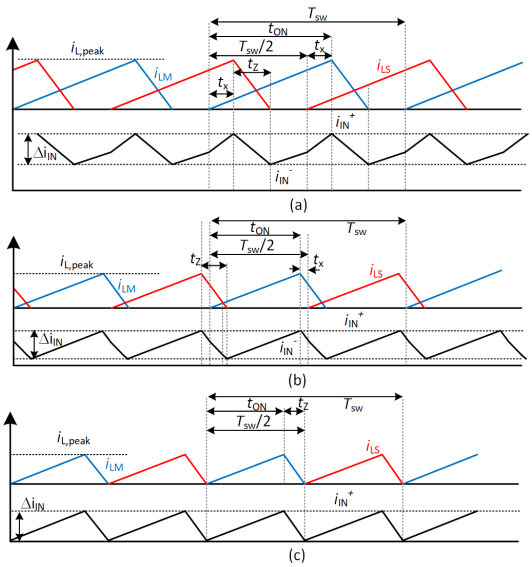

Fig. 10. Input current ripple of the proposed interleaved PFC: (a) $t_{ON} \geq T_{sw}/2$, (b) $t_{ON} < T_{sw}/2$ and $t_{ON}+t_z \geq T_{sw}/2$, (c) $t_{ON}+t_z < T_{sw}/2$.

$$i_{IN}{}^{-} = \begin{cases} i_{L,r}(t_z + t_x) & t_{ON} \geq T_{sw}/2 \\ i_{L,r}(t_z + t_x) & t_{ON} < T_{sw}/2 \ \& \ t_{ON}+t_z \geq T_{sw}/2 \\ 0 & t_{ON}+t_z < T_{sw}/2 \end{cases} \quad (31)$$

where $i_{L,r}$ is the rising inductor current expressed by

$$i_{L,r}(t) = \frac{i_{L,peak}}{DT_{sw}}(t), \quad (32)$$

and t_x is

$$t_x = t_{ON} - \frac{T_{sw}}{2}. \quad (33)$$

Finally, the input current ripple is expressed as

$$\Delta i_{IN} = i_{IN}^{+} - i_{IN}^{-}. \quad (34)$$

VI. Experimental Verification and Comparison

Experimental results are provided to verify the proposed interleaved PFC. To this end, a 400 W prototype is built, shown in Fig. 11, with specifications listed in Table II. Moreover, a commercial Electromagnetic Interference (EMI) filter, shown in Fig. 12, is connected to the proposed interleaved PFC. The

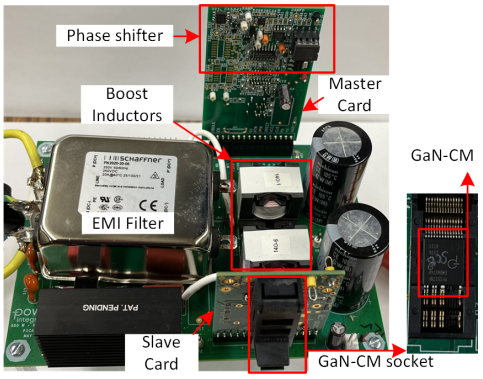

Fig. 11. Experimental setup of the proposed interleaved PFC.

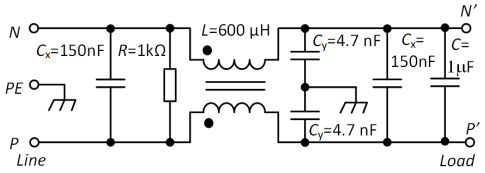

Fig. 12. EMI filter FN2020-20-06 applied to the proposed PFC.

low-line 90Vac and high-line 230Vac results are shown in Fig. 13 and Fig. 14. The experimental results are evaluated to see if the challenges, mentioned in Section V, with GaN-CM interleaving are addressed. The results show that the balanced current sharing is achieved in both low-line and high-line voltages by connecting the output of OTAs externally. Moreover, disabling OFF-time controller of the Slave module leads to stable inductor current in both low-line and high-line voltages. Furthermore, the interleaving performance can closely be evaluated from the zoomed figures in Fig. 13 and Fig. 14 which shows that interleaving is achieved in all the experiments since Δi_{IN} frequency is doubled. However, Δi_{IN} frequency is not always doubled in 90Vac-400W, Fig. 13(b), and it has an irregular shape which does not agree with Fig. 10(a). To further investigate the interleaving performance, Δi_{IN} amplitude at 90° is measured and compared with the theoretical values, shown in Fig. 15(b). The comparison shows that measured Δi_{IN} amplitude does not follow the theoretical values. The reason is that once the OFF-time controller of Slave module is disabled, the phase shifter output (S_t) is connected to the input of the valley detection block not directly to Set of the Slave latch, shown in Fig. 1. Therefore, valley detection does not turn on Slave upon receiving S_t, and it delays turning ON until the valley of Drain voltage arrives. This delay increases the phase shift between Master and Slave to more than 180°. Therefore, the ripple cancellation is not maximized. In other words, the ripple cancellation is mitigated to achieve higher efficiency. The grid current quality of the proposed PFC is evaluated by THD measurements and comparison with THD limits specified by IEEE 519 [15]. The THD limit defined by IEEE 519 is varying based on the maximum demand current and grid stiffness. In the context of this paper, the THD limits of IEEE 519 are determined 20% and 15% for 200W and 400W, respectively. According to the measured THD shown in Fig.

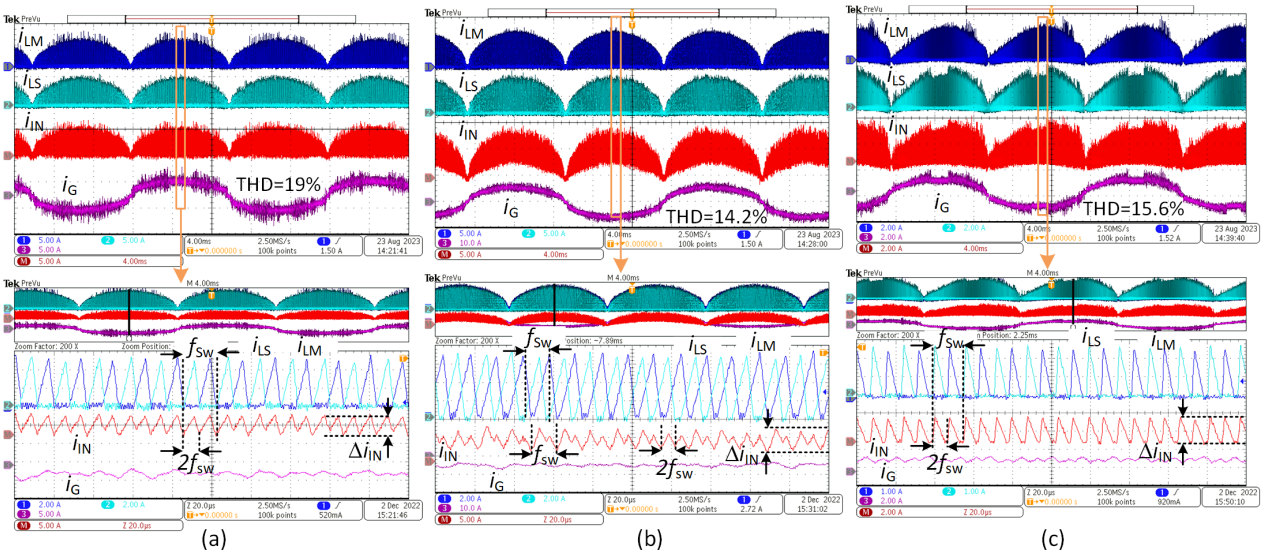

Fig. 13. Experimental results of the proposed PFC at (a) 90Vac-200W (b) 90Vac-400W (c) 230Vac-200W.

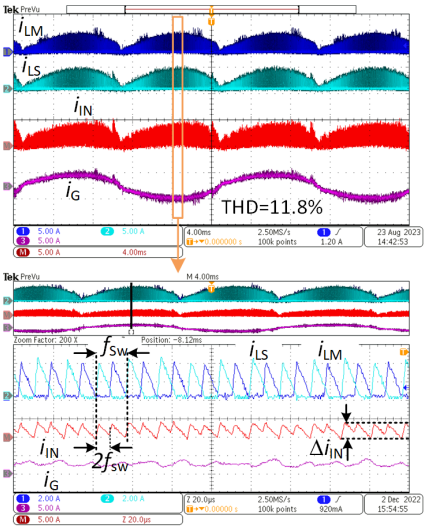

Fig. 14. Experimental results of the proposed PFC at 230Vac-400W.

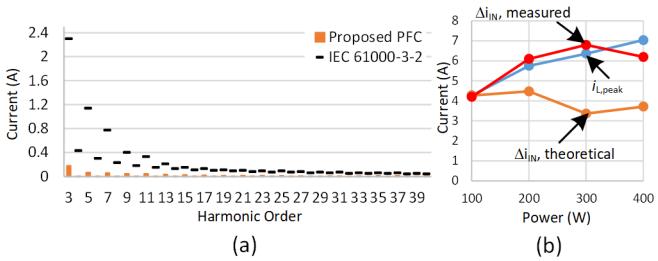

Fig. 15. (a) Grid current harmonic measurements at 230Vac-400W (b) input current ripple Δi_{IN} and inductor peak current of the proposed interleaved PFC.

13 and Fig. 14, the proposed PFC complies with IEEE 519. Furthermore, the proposed PFC is tested for IEC61000-3-2 [16] which specifies harmonic limits. Harmonic measurements in Fig. 15(a) show the compliance of the proposed PFC with IEC61000-3-2. The proposed interleaved PFC is compared with other methods in the literature, as listed in Table V. These selected methods closely match the power rating of the proposed method. The interleaved SEPIC PFC utilizes two Si MOSFETs, switching at 150 kHz with DCM operation [17]. It necessitates four large inductors, each 400 μH, and operates within a limited grid voltage (V_G) range of 85-135 Vac, as well as a low output voltage range of 50-200 V. All components are discrete, and the controller is implemented using a DSP, contributing to higher converter costs at this power level. This method achieves the peak efficiency of 96%. The Dual SEPIC employs four GaN transistors with variable switching frequencies ranging from 400-1000 kHz, operating in CRM [18]. Consequently, the number of inductors is reduced, and they are integrated into a single coupled inductor. However, this method is optimized for V_G=220 Vac, with a low output voltage of 100V. Despite increasing the peak efficiency to 97% compared to [18], it still shares the disadvantages of relying on a DSP and discrete components, leading to increased converter costs. The Totem-Pole PFC uses two GaN transistors with variable switching frequencies in the range of 100-800 kHz, functioning in both DCM and CRM [19]. This method requires a smaller inductor of 55 μH, resulting in the peak efficiency of 98%. However, it is limited to V_G=220 Vac and still requires a DSP and discrete components. Moreover, small inductance achieved by the methods in [18] and [19] is due to high switching frequency which requires proper thermal management of GaN transistors and isolated high-side/low-side gate drivers, further increasing converter costs and design complexity. Furthermore, [18] and [19] lack EMI evaluation to show increasing switching frequency will not lead to a larger EMI filter size. The interleaved CRM PFC eliminates the need for a DSP and discrete components, except the main switches, by integrating gate drivers and controllers into an Integrated Circuit (IC) [9]. This method employs two Si MOSFETs with variable switching frequencies ranging from

TABLE V
PERFORMANCE COMPARISON

Topology	Power	Mode	Main switches	Integrated components				Inductor	f_{sw} (kHz)	V_G (RMS)	V_O (V)	Peak Effi. %
				Main switches	Gate driver	Controller	Current sensor					
Interleaved SEPIC PFC [17]	500W	DCM	2×Si	✘	✘	✘ DSP	✘	4×400μH Coupled	150	85 - 135	50 - 200	96
Dual SEPIC [18]	300W	CRM	4×GaN	✘	✘	✘ DSP	N/A	140+5.8+5.6μH Coupled	400 - 1000	220	100	97
Totem-Pole PFC [19]	400W	DCM +CRM	2×GaN	✘	✘	✘ DSP	✘	1×55μH	100 - 800	220	400	98
Interleaved CRM PFC [9]	300W	CRM	2×Si	✘	✔	✔	N/A	2×340μH	30 - 220	85 - 265	390	97
Proposed	400W	DCM	2×GaN	✔	✔	✔	✔	2×140μH	22 - 150	85 - 265	397	98.41

TABLE VI
EMI COMPARISON DETAILS

	Boost inductance	EMI inductance	EMI noise peak
CRM-PFC [9]	2×340μH	600μH	LF=95 dB HF=71 dB
Proposed	2×140μH	600μH	LF=96 dB HF=44 dB

30-220 kHz, utilizing CRM operation. It demands two boost inductors of 340 μH, achieving the peak efficiency of 97%. Unlike the previous methods, it covers a broad input voltage range of 85-265 Vac and provides a high output voltage of 390 V. In comparison, the proposed method benefits from the high level of integration of GaN-CM, potentially reducing converter costs and simplifying PCB design. It covers a wide input voltage range and achieves a high output voltage of 397V, resulting in the highest peak efficiency of 98.418% compared to the other methods surveyed in Table V. Moreover, GaN-CM eliminates the need for the heatsink, potentially increasing the power density. It should be noted that the integrated components section in Table V reflects the status of the previous works in the literature and does not imply that these methods cannot be developed to integrate more components like GaN-CM. Among the surveyed methods, the interleaved CRM PFC [9] closely matches the proposed topology in terms of covering a wide input voltage range, achieving high output voltage, and eliminating the need for a DSP, and integration, except the main switches. Due to these reasons, the interleaved CRM PFC [9] is subject to a closer comparison with the proposed topology. To this end, the efficiency and PF of the proposed interleaved PFC are measured and compared with an interleaved CRM PFC. The comparison in Fig. 16(a) shows that the proposed interleaved PFC achieves higher efficiency in both low-line and high-line voltages compared to the interleaved CRM PFC, which agrees with loss analysis in Section IV.B. Moreover, the PF comparison in Fig. 16(b) shows that both DCM and CRM achieved PF higher than 0.94.

To ensure the magnetic component size reduction in the proposed PFC is not offset by requiring a larger EMI filter, EMI compression is conducted between the proposed PFC and CRM PFC, both employing the same EMI filter shown in Fig. 12. The EMI results are shown in Fig. 17, and the

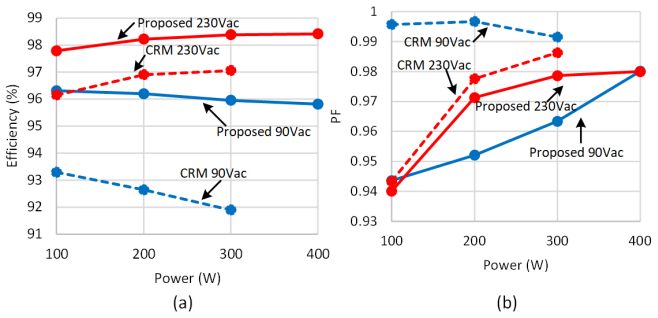

Fig. 16. Experimental comparison: (a) efficiency (b) power factor.

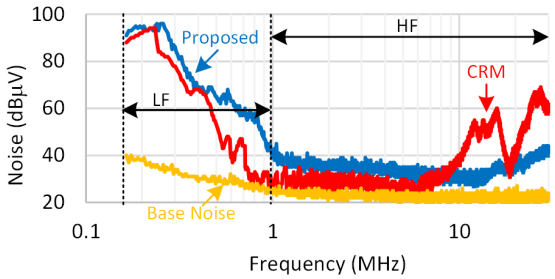

Fig. 17. EMI comparison between the proposed and CRM PFCs.

noise peaks are summarized in Table VI, indicating that at low frequency (LF) the proposed and CRM PFCs have almost the same noise peak with only 1 dB difference while at high frequency (HF), the proposed PFC outperforms the CRM PFC by a great margin. Thus, it can be concluded that the proposed PFC does not require a larger EMI filter.

VII. CONCLUSION

Reducing magnetic component size can significantly lead to overall PFC converter size and cost reduction and efficiency increase. To this end, choosing the right operation mode along with a novel control algorithm is important. In this paper, it was proved that employing DCM with variable ON-time and OFF-time can reduce the boost inductance around 50 % compared to CRM with constant ON-time. The controller is implemented with GaN-CM which is highly integrated, and its power rating is up to 240W with a single module operation. To benefit from small inductor size and high efficiency of

GaN-CM in high-power applications, GaN-CM interleaving is proposed. The challenges with GaN-CM interleaving like its highly integrated package, stable and balanced current sharing, and the trade-off between efficiency and phase shift accuracy were discussed and addressed. The experimental results prove that the proposed interleaved PFC meets the regulatory standards with high efficiency compared to CRM interleaved PFC.

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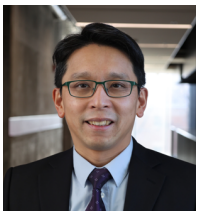

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