Three-phase Transformerless PV Inverter with Reconfigurable *LCL* Filter and Reactive Power Capability

Jalal Dadkhah, *Student Member, IEEE,* Carl Ngai Man Ho, *Senior Member, IEEE,*
Ken King-Man Siu, *Senior Member, IEEE*

***Abstract*—Constructing *LCL* filter with only three inductors is made possible by a topology called the reconfigurable filter in three-phase converters, in which the filter is reconfigured six times during the AC line cycle. While the existing reconfigurable filter reduces the magnetic components by half, it cannot be installed as an add-on filter to existing converters due to requiring a DC link connection. In this paper, a novel reconfigurable *LCL* filter applied in Photovoltaic (PV) transformerless inverters is proposed, which not only inherits the merits of the existing reconfigurable filter but also eliminates the need for a DC link connection, enabling easy installation in existing converters. Additionally, the proposed reconfigurable filter effectively clamps the common-mode (CM) voltage to Neutral at high frequencies, resulting in the reduction of leakage current. Therefore, the proposed topology offers several advantages with one solution, including injecting high-quality grid current, magnetic component reduction, leakage current reduction, compatibility with add-on installations, and reactive power support. Comprehensive equivalent circuits, modeling, and analysis are provided to study the operation modes, leakage current capability, and loss breakdown of the proposed topology. The proposed topology is verified and compared with the existing reconfigurable filter by a 1-kW experimental prototype. All the experimental results agree with the theoretical concepts.**

***Index Terms*—Inverter, *LCL* filter, Photovoltaic, magnetic component, leakage current, three-phase converter.**

I. Introduction

POWER conversion in Photovoltaic (PV) systems is realized by PV inverters which can be classified as either isolated or non-isolated. Isolated PV inverters employ either a high-frequency (HF) transformer or a low-frequency transformer to establish galvanic isolation. In contrast, non-isolated PV inverters, commonly known as transformerless inverters, are directly connected to the grid. Therefore, transformerless PV inverters have the advantage of lower cost, smaller size, and higher efficiency. Both types of PV inverters have to satisfy high-quality current injection to the grid in compliance with grid codes like IEC 61000-3-2-1 and IEEE 519 [3], [4].

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J. Dadkhah and Carl N. M. Ho are with RIGA Lab, the Department of Electrical and Computer Engineering, University of Manitoba, Winnipeg, MB R3T5V6, Canada (e-mail: dadkhahj@myumanitoba.ca; carl.ho@umanitoba.ca).

K. K. M. Siu is with the Department of Electrical Engineering, University of North Texas, United States (e-mail: kingman.siu@unt.edu).

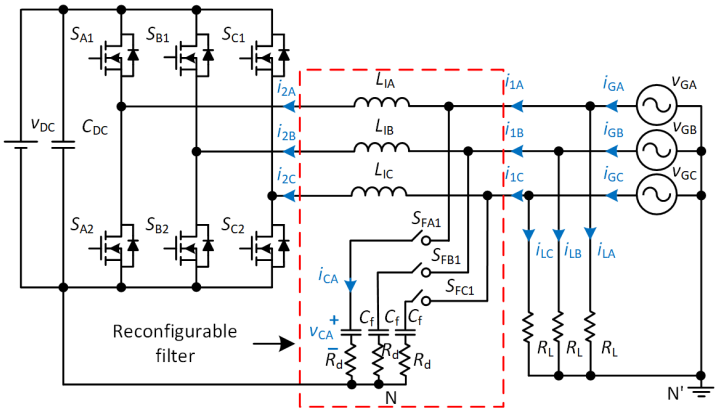

Fig. 1. 4wire-Re topology applied in PV application [2].

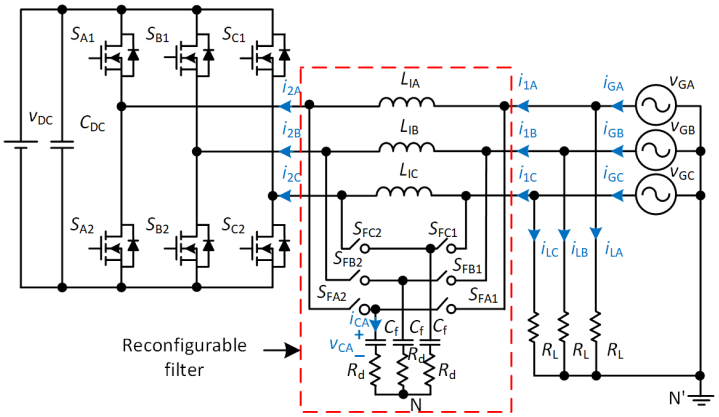

Fig. 2. The proposed 3wire-Re topology.

However, transformerless PV inverters have an additional requirement: the suppression of leakage current. This arises due to HF components in the common-mode (CM) voltage, which are imposed on the parasitic capacitor formed between the PV panel and the system ground. Leakage current can result in electromagnetic interference (EMI) issues, potential safety risks for maintenance personnel, increased system losses, and higher total harmonic distortion (THD) in the current injected into the grid. To address these concerns, international standards such as IEC 62109-2 [5] impose strict limitations on the RMS value of the leakage current, limiting it to 300 mA. Besides,

power networks with high penetration of PV systems may suffer from voltage fluctuations. For instance, reverse power flow from load buses to the substation increases the voltage along low-voltage feeders. Similarly, significant voltage drops may occur during high-load consumption periods. Therefore, PV inverters should contribute to voltage regulation by injecting or absorbing reactive power [6]. The required reactive power injection or absorption is 48% of rated active power, corresponding to Power Factor (PF)=0.9 [7], [8].

To achieve high-quality current injection into the grid, utilizing high-order *LCL* filters is a widely adopted approach in PV inverters [9]. While *LCL* filters effectively ensure high-quality current injection, it suffers from the drawback of requiring a high number of inductors in three-phase PV inverters. To address this issue, high-order filters have been developed with the objective of reducing the size of filter components while maintaining a high filtering capability. For instance, *LLCL* filter is formed by introducing an additional inductor in series with the capacitor of the conventional *LCL* filter [10], while *LCCL* filter incorporates a capacitor in parallel with the grid-side inductor of the conventional *LCL* filter [11]. These modifications aim to reduce filter inductance value while eliminating switching frequency harmonics. However, it should be noted that the harmonic attenuation rate of these modified filters decreases from -60 dB/decade to -20 dB/decade in the HF band. Consequently, more passive components are added to *LLCL* and *LCCL* filters to enhance the harmonic attenuation rate [12]–[15]. Additionally, more complex filters, such as Trap filters, which consist of several *LC* branches, have been proposed in the literature [16], [17]. While these high-order filters showcased good filtering performance, they also introduced challenges such as increased passive components, design complexity, and resonance issues.

In addition to employing high-order filters for achieving high-quality current injection, various methods have been employed to suppress the leakage current in three-phase three-wire (3p3w) transformerless PV inverters. An approach to reduce the leakage current is through modified modulation techniques. One example is the active-zero-state pulse width modulation (AZSPWM) technique, which utilizes only active vectors to construct the reference inverter voltage [18], [19]. Another example is vector-split PWM (VSPWM), in which two boundary vectors, namely leading and lagging vectors, are employed to avoid zero vectors when constructing the reference vector [20]. While these modified modulation techniques can reduce CM voltage, they often result in higher switching losses and limited modulation index.

DC-bypass topologies are another technique to address leakage current. One particular topology, known as H7, employs an additional switch to disconnect the PV array from the inverter during zero voltage vectors [21], [22]. To deal with oscillations in CM voltage caused by junction capacitors, a clamp branch is added to H7 topology [23]. H8 topology was introduced to reduce CM voltage and improve either efficiency or THD depending on the PWM method [24]. However, a significant drawback of these topologies is the increased number of switches that operate at HF switching and rated current and voltage, leading to lower system efficiency. Another method to suppress the leakage current is Virtual Ground (VG) [25], [26]. In this method, the voltage between the filter star point and the system ground is controlled to be zero. However, the voltage balancing of the split capacitors of the DC link is necessary. To deal with both requirements of transformerless PV inverters simultaneously, i.e., injecting high-quality current with reduced leakage current, Active Virtual Ground (AVG) technique was introduced. In this technique, which was applied in various single-phase topologies [27]–[29], inductors are fully utilized so that a high-order filter is formed with the minimum number of inductors. Moreover, the DC link is virtually connected to the system ground at HF, which reduces leakage current. AVG has been developed for a three-phase power factor correction (PFC) converter called the reconfigurable filter, which builds an *LCL* filter with only three inductors, reducing the number of inductors by half in the three-phase PFC converter [2]. The reconfigurable filter is shown in Fig. 1, applied in a PV system. In this paper, the reconfigurable filter in [2] is named 4wire reconfigurable (4wire-Re) filter due to having four connections to the filter, i.e., three connections from the grid side and one connection from the DC link. 4wire-Re topology achieved a comparable THD compared to the conventional *LCL* filter. The concept of the reconfigurable filter is a promising substitute for existing converters utilizing conventional *LCL* filters. The substitution not only reduces the number of inductors by half but also can suppress the leakage current. However, its installation is not a simple add-on process. In fact, the reconfigurable filter in [2] requires a DC link connection. Nevertheless, the DC link in high-power PV inverters may not be easily accessible due to safety and design considerations. The DC voltage levels can be quite high, typically hundreds of volts or even higher, and can pose significant electrical hazards if not handled properly. To ensure safety and compliance with regulations, DC input terminals are typically located far from AC terminals. Therefore, it is hard to treat 4wire-Re topology as an add-on filter.

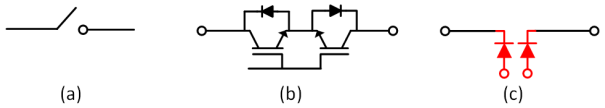

Fig. 3. Bidirectional switch implementation: (a) ideal bidirectional switch (b) two IGBTs back-to-back in series (c) Monolithic Bidirectional Power transistor.

In this paper, a novel reconfigurable filter is proposed that does not need a DC link connection and can be used as the add-on filter to existing converters utilizing conventional *LCL* filters. The proposed topology is called 3wire reconfigurable (3wire-Re) filter, shown in Fig. 2. The name signifies its three connections from the grid side and no connection to the DC link. The proposed topology fully utilizes the converter-side inductor so that an *LCL* filter is constructed with only three inductors. Moreover, CM voltage is connected to the system ground through a low-impedance path at HF. Therefore, the leakage current is mitigated. Furthermore, the proposed topology is able to inject and absorb reactive power to meet the related standards [7], [8].

TABLE I
LITERATURE REVIEW SUMMARY

	High-order filter	Leakage current reduction	Inductor reduction	DC link-less
Filter topologies [9]–[17]	X	7	7	X
Modulation techniques [18], [20]	7	X	7	X
DC-bypass [21]–[24]	7	X	7	X
VG [25], [26]	X	X	7	7
4wire-Re [2]	X	X	X	7
Proposed 3wire-Re	X	X	X	X

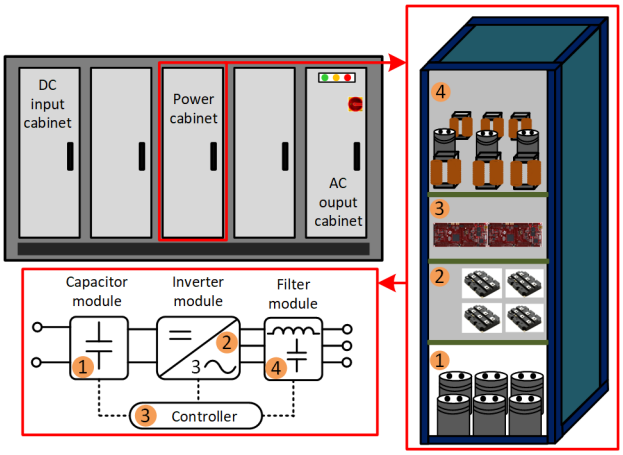

Fig. 4. Typical example of a high-power central PV inverter.

The key components of 3wire-Re topology are a set of bidirectional switches, shown in Fig. 3, which are used to change the role of the inductors from the grid side to the converter side and vice versa. The bidirectional switches are switching at low frequency, twice the line frequency, e.g., 120 Hz. Therefore, their switching loss is negligible. However, it may raise concerns regarding the high number of switches required to construct the reconfigurable filter. Nevertheless, the proposed topology and the prototype used in this paper serve the purpose of validating the concept. Looking ahead to future development and commercialization, several factors should be considered regarding the proposed topology. Firstly, the semiconductor industry is continuously advancing, leading to more affordable and integrated semiconductor solutions. This means that all the bidirectional switches and gate drivers can be integrated into a compact package. On the other hand, inductors made from rare earth materials are becoming more expensive. As a result, using additional semiconductors to reduce the dependence on inductors becomes justifiable. Secondly, a new generation of semiconductors is emerging, which reduces the number of components required for building bidirectional switches. A recent breakthrough in this regard is the development of Monolithic Bidirectional power transistors, as illustrated in Fig. 3(c) [30], [31]. These advancements in semiconductor technology provide opportunities for improving the efficiency and compactness of the proposed topology.

The summarized literature review in Table I emphasizes the distinctive contributions of the proposed topology to PV systems when compared to the existing solutions. The proposed topology offers a comprehensive solution that combines high-order filtering capability, leakage current reduction, inductor reduction, and DC link-less connection. Table I clearly demonstrates that no other existing method can offer all these features simultaneously.

It is worth mentioning that the proposed topology was briefly introduced in [1]. However, in this paper, a more comprehensive analysis and details are provided as follows:

- Expressing detailed switching schemes with reactive power support
- Introducing AVG technique in three-phase converters
- Developing leakage current models for both 3wire-Re and 4wire-Re topologies
- Expressing a detailed frequency response and loss analysis
- Verifying the proposed topology with extensive experimental results
- Verifying reactive power injection and absorption capabilities
- Comparing the proposed topology with 4wire-Re topology as the benchmark

II. COMPACT AND MODULAR FILTERING SOLUTION

The proposed topology offers DC link-less connection, which is advantageous in the context of high-power converters where the components have modular configuration. To clarify, a typical high-power central PV inverter is shown in Fig. 4. These central inverters are often composed of separate DC input, AC output, and power cabinets, with each power cabinet rated at 350 kW and 1 kV DC [32]. The power cabinets are comprised of various modules, including capacitor modules, inverter modules, controllers, and filter modules, all designed with plug-and-play configurations for easy maintenance and replacement. When it comes to integrating a new filter solution into such central inverters, the DC link-less connection of the proposed 3wire-Re topology is advantageous. This is because 3wire-Re topology can be seamlessly integrated as a plug-and-play module by replacing the existing filter module. The absence of a DC link connection simplifies the installation process, making it much more straightforward. In contrast, incorporating 4wire-Re topology, which requires a DC link connection, would not be as straightforward. Establishing a DC link connection involves working with high voltages, and it is a more complex process. It often necessitates discharging DC link capacitors and should be carried out by trained personnel, which adds complexity and safety considerations to the installation process. Therefore, the DC link-less feature of the proposed 3wire-Re topology makes it a more practical and user-friendly solution, particularly when retrofitting existing central PV inverters like the one shown in Fig. 4. The reduction in inductor count, as accomplished by the proposed

Fig. 5. Filter volume comparison: (a) conventional LCL filter [2] (b) the proposed 3wire-Re topology.

TABLE II
FILTER VOLUME AND COST COMPARISON

	Conventional LCL filter	Proposed LCL filter
Width	13 cm	7.5 cm
Lenght	13.5 cm	13.5 cm
Hight	2.7 cm	3.4 cm
Volume	473.85cm^3	344.25cm^3
Cost	143 USD	117 USD

Fig. 6. Semiconductor and inductor price trends based on the producer price index [33], [34].

topology, results in substantial savings both in terms of volume and cost. To accurately gauge the volume benefits offered by the proposed topology, filter boards for both the proposed topology and the conventional LCL filter [2] are designed, as presented in Fig. 5. A breakdown of the filter dimensions is provided in Table II. Notably, the proposed topology achieves a remarkable 27% reduction in filter volume when compared to the conventional filter. As a direct consequence, the filter cost is notably diminished, with an estimated cost reduction of approximately 18%. It is essential to note that this cost reduction calculation is based on the current market price and a single prototype. Considering the price trend of inductors and semiconductors provides a more realistic perspective on how reducing magnetic components by employing semiconductors will decrease costs in the future. The producer price index in Fig. 6 illustrates the price change of inductors and semiconductors relative to their base year. Inductor prices have increased by more than 51%, while semiconductor prices have decreased by 69%, relative to their respective base years. As a result, it can be predicted that the cost reduction achieved

Fig. 7. The switching scheme of the proposed topology in the inductive reactive power mode.

Fig. 8. The switching scheme of the proposed topology in the capacitive reactive power mode.

Fig. 9. Equivalent circuits of the proposed topology in the inductive mode.

Fig. 10. Simpli ed equivalent circuits of the proposed topology in the inductive mode.

by the proposed topology will be even more signi cant in the future than reported in Table II.

III. Principle of Operation

The proposed topology is designed for a 3p3w system, which inherently allows the sum of inverter output currents to be zero. Therefore, the output current is formed by only two phases under control. Discontinuous pulse width modulation (DPWM) techniques were used to utilize this feature of 3p3w systems. If the proposed topology is used along with DPWM, an LCL lter is built with only three inductors, reducing the number of inductors signi cantly. The switching scheme of the proposed topology is depicted for inductive and capacitive reactive power support, Fig. 7 and Fig. 8, respectively. Both switching schemes consist of six main operation modes, and each main operation mode has two sub-modes. In fact, the current polarity of one phase changes in the main mode if there is reactive power support, either capacitive mode or inductive mode. Therefore, sub-modes differentiate the current polarity in the main mode; otherwise, there is no sub-mode since there is no change in the current polarity. The capacitive and inductive operation modes have the same equivalent circuits, except their current polarity is different. Therefore, the equivalent circuits are only derived for the inductive mode, shown in Fig. 9 and Fig. 10; the same principle can be applied to derive the capacitive one. Taking Mode I in Fig. 9 as an example, leg A is inactive, and legs B and C are active, operating at HF. In this case, the recon gurable lter places the inductor associated with the inactive phase, L_{IA}, on the grid side by turning S_{FA1} = OFF and turning S_{FA2} = ON. Simultaneously, inductors of the active phases, L_{IB} and L_{IC}, are placed at the converter side by turning S_{FB1}, S_{FC1} = ON and turning S_{FB2}, S_{FC2} = OFF. In this mode, the current direction of phase C changes based on sub-modes, I_1 and I_2. Finally, the LCL lter is formed by only three inductors. The same principle is applied to the other operation modes, such as Mode II, where L_{IB} remains on the converter side while L_{IA} is transferred to the converter side and L_{IC} to the grid side. The simpli ed equivalent circuits in Fig. 10 demonstrate that the LCL lter is effectively constructed in all the operation modes using only three inductors. It has to be mentioned that the damping resistors (R_d) are omitted in Fig. 9 and Fig. 10 for the purpose of simpli ed illustration.

IV. Leakage Current and Active Virtual Ground

Transformerless PV inverters are susceptible to leakage current, which stems from the HF content of CM voltage, (v_{CM}). Therefore, v_{CM} mitigation is important in PV inverters. To investigate v_{CM} mitigation in 3wire-Re and 4wire-Re topologies, their equivalent circuits in Mode I are shown and compared in Fig. 11. Both topologies are able to clamp v_{CM} to Neutral of the grid through an HF path called AVG. In fact, AVG is a low impedance path that is formed at HF through capacitors and provides a virtual ground for v_{CM}. Therefore, there is no physical connection between the DC link and the system ground, and v_{CM} is mitigated intrinsically. The recon gurable lter topologies are compatible with DPWM, which can be modeled by a 3rd-order harmonic injection, V_{3rd},

Fig. 11. AVG in (a) 3wire-Re topology (b) 4wire-Re topology.

Fig. 12. Conceptual waveforms of leakage current and CM voltage: (a) 3wire-Re topology (b) 4wire-Re topology.

as shown in Fig. 11. In 4wire-Re topology, v_{cf} is affected by V_{3rd} in a way that grid voltage plus V_{3rd} are imposed on v_{cf} which makes v_{cf} non-sinusoidal, as shown in Fig. 11(b). Therefore, V_{3rd} is modi ed by modi ed DPWM (MDPWM) [35] to have a soft transition in the interval of to avoid ringing and oscillation in the output current [2]. In contrast, v_{cf} is sinusoidal and independent of V_{3rd} in 3wire-Re topology, as shown in Fig. 11(a). Moreover, v_{CM} is described by

$$v_{CM} = V_{CM} + v_{cm} \quad V_{3rd}; \qquad (1)$$

where $V_{CM} = V_{3rd}$ is the large signal, and $v_{cm}=v_{HF}$ is the small signal which is almost zero due to AVG. Therefore, V_{3rd} should also have soft transitions in 3wire-Re topology to avoid spikes on leakage current. The conceptual waveforms of i_{CM} and v_{CM} are depicted in Fig. 12. In both topologies, MDPWM is applied to make v_{CM} have soft transitions in the interval of ; however, the leakage current has different behaviors in 3wire-Re and 4wire-Re topologies. During, both topologies change to C lter, and i_{CM} is not suppressed by AVG. Nevertheless, in 4wire-Re topology, the DC link connection to the star point of the lter damps i_{CM} while in 3wire-Re topology, i_{CM} is not suppressed during . In 4wire-Re topology, =20 is chosen to achieve the lowest

Fig. 13. Leakage current model of 3wire-Re topology.

Fig. 14. Leakage current model of 4wire-Re topology.

THD [2], but in 3wire-Re topology, must be chosen to ensure i_{CM} is less than the standard limit. To this end, i_{CM} models of 3wire-Re and 4wire-Re topologies are derived in Fig. 13 and Fig. 14, respectively. According to the models, i_{CM} amplitudes in 3wire-Re and 4wire-Re topologies are expressed by, respectively,

$$i_{CM\ 1;3wire} = \frac{3Z_C Z_1}{3Z_C Z_1 + 3Z_C Z_{CM} + 2Z_{CM} Z_1} i_{HF}; \quad (2)$$

$$i_{CM;\ 4wire} = \frac{Z_C Z_1}{Z_C Z_1 + Z_C Z_{CM} + 2Z_{CM} Z_1} i_{HF}; \quad (3)$$

where

$$Z_1 = L_l s; Z_C = \frac{1}{C_f s} + R_d; Z_{CM} = \frac{1}{C_{CM} s}; i_{HF} = i_{ia} + i_{ib}: \quad (4)$$

Moreover, $i_{CM2,3wire}$ is measured in simulation and is 1.5A. The effect of on i_{CM} is explored in Fig. 15. It shows that has a direct relationship with i_{CM}. To meet i_{CM} standard, the minimum possible value of should be selected. This value is found experimentally to be 7 which gives enough margin from the standard. The value smaller than 7 leads to large spikes on i_{CM} and v_{CM}, based on experimental observations. Moreover, Fig. 15 shows that the effect of component tolerances and temperature, listed in Table III, on i_{CM} is negligible.

V. Frequency response analysis

A. Frequency response of 3wire-Re topology

The frequency response of 3wire-Re topology is derived by considering one of the equivalent circuits in Fig. 10. For

Fig. 15. Effect of on the leakage current.

Fig. 16. HF equivalent circuit of the proposed topology in Mode II.

TABLE III
Tolerances of key components affecting the leakage current

Parameters	Value
Film capacitor tolerance (C_f, C_{CM})	10%
Temperature coefficient of capacitor (C_f, C_{CM})	100ppm/°C
Inductor tolerance (L_l)	5%

instance, the HF equivalent circuit of Mode II is considered and shown in Fig. 16 in which v_G is neglected at the switching frequency, and switching actions are replaced with the source of harmonics v_{sa} and v_{sb}. Since the equivalent circuit in Fig. 16 cannot be simplified into a single-phase equivalent circuit, the superposition principle is used to derive the frequency response of 3wire-Re topology. By applying the superposition principle, two admittances are defined as

$$Y_{i_{gc}\ v_{sa}}(s) = \left.\frac{i_{gc}(s)}{v_{sa}(s)}\right|_{v_{sb}=0}; Y_{i_{gc}\ v_{sb}}(s) = \left.\frac{i_{gc}(s)}{v_{sb}(s)}\right|_{v_{sa}=0} \quad (5)$$

where

$$Y_{i_{gc}\ v_{sa}}(s) = \frac{3C_f R_d s^3}{2L_l^2 C_f s^3 + 9L_l R_d C_f s^2 + 9L_l s}: \quad (6)$$

Due to symmetry in HF equivalent circuit in Fig. 16, it is also deduced that

$$Y_{i_{gc}\ v_{sa}}(s) = Y_{i_{gc}\ v_{sb}}(s): \quad (7)$$

Finally, the complete response of i_{gc} to v_{sa} and v_{sb} is

$$i_{gc}(s) = Y_{i_{gc}\ v_{sa}}(s)v_{sa}(s) + Y_{i_{gc}\ v_{sb}}(s)v_{sb}(s): \quad (8)$$

By assuming

$$\begin{bmatrix} v_{sa}(s) \\ v_{sb}(s) \\ v_{sc}(s) \end{bmatrix} = \begin{bmatrix} 1 \\ e^{\frac{2}{3}j} \\ e^{\frac{2}{3}j} \end{bmatrix} v_{sa}(s); \quad (9)$$

the trans-admittance of the reconfigurable filter is

$$Y_{Recon\,1}(s) = \frac{i_{gc}(s)}{v_{sa}(s)} = Y_{i_{gc}\ v_{sa}}(s)(1 + e^{\frac{2}{3}j}): \quad (10)$$

Moreover, similar to Y_{Recon1}, the relationship between i_{ia} and v_{sa} is derived as

$$Y_{Recon\,2}(s) = \frac{i_{ia}(s)}{v_{sa}(s)} = Y_{i_{ia}\ v_{sa}}(s) + Y_{i_{ia}\ v_{sb}}(s)e^{\frac{2}{3}j}; \quad (11)$$

where

$$\begin{aligned} Y_{i_{ia}\ v_{sa}}(s) &= \frac{L_l C_f s^2 + 2C_f R_d s + 6}{2L_l{}^2 C_f s^3 + 9C_f R_d L_l s^2 + 9L_l s}; \\ Y_{i_{ia}\ v_{sb}}(s) &= \frac{9C_f R_d s - 9}{2L_l{}^2 C_f s^3 + 9C_f R_d L_l s^2 + 9L_l s}: \end{aligned} \quad (12)$$

By combining (10) and (11), the relationship between i_{gc} and i_{ia} is found as

$$\frac{i_{gc}(s)}{i_{ia}(s)} = \frac{Y_{Recon\,1}(s)}{Y_{Recon\,2}(s)}: \quad (13)$$

By putting $R_d = 0$ in (10), the resonant frequency of the reconfigurable filter can be obtained as

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{3}{2L_l C_f}}: \quad (14)$$

Fig. 17. Frequency responses of the conventional LCL filter and the reconfigurable filter.

Fig. 18. Conceptual waveforms of v_{CA}, i_{CA}, i_{SFA1}, and i_{SFA2}: (a) 3wire-Re (b) 4wire-Re.

B. Frequency response comparison and evaluation

A comparison is made between 3wire-Re and 4wire-Re topologies, shown in Fig. 2 and Fig. 1, respectively. To this end, first, the converter specifications are defined in Table IV, and converter parameters are designed and listed in Table V according to design guidelines provided in [2]. The bode diagram representing (10) is depicted in Fig. 17 for both 3wire-Re and 4wire-Re topologies. There are two key points that need to be highlighted in Fig. 17. Firstly, the resonant frequency of the proposed topology is higher than 4wire-Re topology, which leads to a smaller damping resistor according to (15) [9]. Secondly, the proposed topology has a higher magnitude compared to 4wire-Re at high frequencies. It implies that the proposed topology achieves lower attenuation between i_{gc} and v_{sa}. The harmonic attenuation between i_{gc} and i_{ia}, described in (13), also shows that 3wire-Re topology has lower attenuation compared to 4wire-Re, according to Table V. This point can also be explained intuitively that the proposed topology has one more capacitor than 4wire-Re topology, according to Fig. 11. The capacitor is in series with the other two ones, leading to higher impedance in the branch. Consequently, capacitors absorb smaller current ripple, which means lower harmonic attenuation. Although the proposed topology achieved lower harmonic attenuation compared to 4wire-Re, it can satisfy grid codes related to harmonic current emissions. This point is verified by experimental results in Section VII.

$$R_d = \frac{1}{3\omega_{res} C_f}: \quad (15)$$

TABLE IV
SYSTEM SPECIFICATIONS

Parameters	Value	Parameters	Value
Grid voltage	208 Vrms-ll	Power	1 kW
Grid frequency	60 Hz	V_{DC}	390 V
R_L	33	PF	0.73 - 1

TABLE V
SYSTEM PARAMETERS

Parameters	3wire-Re topology	4wire-Re topology
L_l	3 mH	3 mH
C_f	2.2 μF	2.2 μF
I_{max}	0.647 A (23%)	0.647 A (23%)
	7°	20°
f_{res}	4.16 kHz	2.4 kHz
f_{sw}	25 kHz	25 kHz
R_d	5	10
$\lvert i_{gc}(f_{sw})/i_{ia}(f_{sw})\rvert$	3.6%	1.1%

VI. LOSS ANALYSIS

The loss breakdown of 3wire-Re and 4wire-Re topologies includes switching cell loss, magnetic loss, and filter loss.

Fig. 19. Loss analysis.

Fig. 20. Simplified model of a bidirectional switch for loss analysis: (a) actual bidirectional switch (b) simplified unidirectional model.

The switching cell loss, consisting of conduction loss and switching loss, and magnetic loss, consisting of copper loss and core loss, were analyzed in detail in [2]. However, the filter loss calculation in [2] relied on simulation data, whereas this paper adopts a mathematical model. To this end, conceptual waveforms of filter capacitor voltage v_{CA} and current i_{CA} of phase A are depicted in Fig. 18. In 3wire-Re topology, i_{CA} is equal to either inductor current ripple i_{LA} when Leg A is at HF switching or 2 i_{LA}, i.e., the sum of i_{CB} and i_{CC}, when Leg A is disabled. In 4wire-Re topology, i_{CA} is equal to either i_{LA} when Leg A is at HF switching or zero when Leg A is disabled. Therefore, i_{CA} in 3wire-Re topology has a higher RMS value compared to 3wire-Re topology. On the other hand, 3wire-Re topology has a smaller R_d compared to 4wire-Re topology. By using (16), it turns out that 3wire-Re leads to slightly higher power loss in R_d even though it has a smaller R_d, shown in Fig. 19. Moreover, bidirectional switches also contribute to reconfigurable filter loss. In 3wire-Re topology, i_{CA} flows through i_{SFA1} when phase A is at HF switching and i_{SFA2} when phase A is disabled. However, in 4wire-Re topology, i_{CA} always flows through i_{SFA1}. To calculate the conduction loss of a bidirectional switch, its unidirectional loss is calculated according to Fig. 20 and (17), where the unidirectional loss is multiplied by 2 to account for the bidirectional loss. A similar procedure can be applied to find conduction loss in S_{FA2}. The switching loss of bidirectional switches is neglected because of their low switching frequency. The conduction loss of bidirectional switches can be reduced by using Wide Band Gap (WBG) semiconductors. Since 3wire-Re and 4wire-Re topologies have the same switching scheme and inductor values, their switching cell loss and magnetic loss are the same.

Fig. 21. Prototype of the proposed topology.

Fig. 22. Switching gate signals of phase A: (a) 3wire-Re (b) 4wire-Re.

$$P_{Rd} = 3R_d i^2_{CA;rms}\ ; \tag{16}$$

$$P_{R_{on}} = \underbrace{2(0.1 i^2_{SFA\ 1P;rms} + 0.5 i_{SFA\ 1P;avg})}_{\text{Switch}} + \underbrace{2(0.08 i^2_{SFA\ 1P;rms})}_{\text{Body diode}}; \tag{17}$$

where $i_{SFA1P,avg}$ and $i_{SFA1P,rms}$ are the average and RMS values of i_{SFA1P}, respectively.

VII. Experimental verification

The proposed topology is verified and compared with 4wire-Re topology by experimental results. To this end, the prototype of the proposed topology is built, shown in Fig. 21, and tested for the system specifications defined in Table IV and system parameters defined in Table V. Besides, the proposed topology and 4wire-Re topology utilize the same controller which is implemented in TI TMS320F28379D microcontroller. The switching gate signals of phase A in the proposed topology and 4wire-Re topology are explored in Fig. 22. In both topologies, phase A is disabled by turning S_{A1} ON and S_{A2} OFF or vice versa, which are Modes I and IV, respectively. In 3wire-Re and 4wire-Re topologies, the filter gate signals determine the role of the inductors to be either the grid-side inductor or the converter-side inductor. In 4wire-Re topology, there is one filter gate signal per phase. For instance in phase A, S_{FA1} OFF makes L_{IA} to be the grid-side inductor, Modes I and IV, and S_{FA1} ON makes L_{IA} to be the converter-side inductor, Modes II, III, V, and VI, shown in Fig. 22(b). However, in 3wire-Re topology, there are two filter gate signals per phase which determine the role of the inductors. For instance, in phase A, S_{FA1} OFF and S_{FA2} ON make L_{IA} to be the grid-side inductor, Modes I and IV, and S_{FA1} ON and S_{FA2} OFF make L_{IA} to be

Fig. 23. Experimental results at 1kW and PF=1: (a) 3wire-Re, output currents (b) 4wire-Re, output currents (c) 3wire-Re, converter-side currents (d) 4wire-Re, converter-side currents.

Fig. 24. Experimental results at 1kW and PF=0.73 (capacitive mode): (a) 3wire-Re, output currents (b) 4wire-Re, output currents (c) 3wire-Re, converter-side currents (d) 4wire-Re, converter-side currents.

Fig. 25. Experimental results at 1kW and PF=0.73 (inductive mode): (a) 3wire-Re, output currents (b) 4wire-Re, output currents (c) 3wire-Re, converter-side currents (d) 4wire-Re, converter-side currents.

the converter-side inductor, Modes II, III, V, and VI, shown in Fig. 22(a).

Fig. 26. THD measurement at 1kW.

Fig. 27. Harmonic measurement of output currents.

The output currents and converter-side currents for zero, capacitive, and inductive reactive power are depicted in Figs. 23, 24, and 25, respectively. The experimental results show that both topologies achieved high-quality output currents in PF range between 0.73 and 1. The output current quality is quanti ed by THD measurements shown in Fig. 26. In PF range of 0.73 and 1, THD varies from 3.5% to 4.0% in both topologies. The THD range complies with IEEE 519 standard which speci es THD limit of 5% [4]. Moreover, the harmonic measurement is shown in Fig. 27 and compared with IEC 61000-3-2 standard [3]. The results show that the proposed topology meets the standard by a great margin. Therefore, from the current quality point of view, the proposed topology achieved a comparable performance to 4wire-Re topology.

The experimental results presented in Fig. 28 validate the conceptual waveforms depicted in Fig. 18. These results demonstrate that the capacitor voltage in 4wire-Re is non-sinusoidal and remains non-conductive during phase disabling, as illustrated in Fig. 28(b). On the other hand, 3wire-Re achieves a sinusoidal capacitor voltage waveform that remains conductive throughout the operation, as shown in Fig. 28(a).

The other important veri cation of PV inverters is the leakage current. The parasitic capacitance for crystalline silicon PV modules is 50-150nF/kW [35]. Therefore, the worst parasitic capacitor, C_{CM}=150nF, is considered and connected to the converter like the one shown in Fig. 11. In 3wire-Re topology, the theoretical value of i_{CM} with $\quad$=7 is 249.6 mA-RMS, shown in Fig.15. The experimental value of i_{CM} with $\quad$=7 is between 253 - 257 mA-RMS, shown in Figs. 29 (a) and (c). Moreover, the theoretical value of i_{CM} in 4wire-Re is 90 mA-

Fig. 28. Filter capacitor voltage and current: (a) 3wire-Re (b) 4wire-Re.

Fig. 29. Leakage current and CM voltage: (a) 3wire-Re at PF=1 (b) 4wire-Re at PF=1 (c) 3wire-Re at PF=0.9 (d) 4wire-Re at PF=0.9.

Fig. 30. Ef ciency measurement at 1kW.

RMS, calculated by (3). The experimental value is between 93.3 - 94.2 mA-RMS, shown in Figs. 29(b) and (d). Therefore, the accurate modeling of the leakage current in both 4wire-Re and 3wire-Re topologies is veri ed with acceptable errors.

The ef ciency of both converters is assessed and compared, as illustrated in Fig. 30. Additionally, estimated ef ciency, calculated based on the loss analysis detailed in Section VI, is superimposed on Fig. 30. The results reveal that 3wire-Re and 4wire-Re topologies achieve peak ef ciencies of 98.176% and 98.219%, respectively, with only a marginal ef ciency difference of approximately 0.043%. Notably, the estimated ef ciency of 3wire-Re topology closely aligns with the measured ef ciency.

Furthermore, a broader comparison with other methods is provided in Table VI. The scalar PWM and AZSPWM are modulation techniques. They employed three inductors without a DC link connection; however, they have poor THD and leakage current. oH8 topology is based on DC-bypass methods and requires three more HF switches while improving the leakage current compared to modulation techniques. The conventional LCL lter showed case the worst THD and leakage current mainly due to unsuppressed CM voltage. In contrast, 4wire-Re has the lowest leakage current with only three inductors, while it needs a DC link connection. In comparison, the proposed 3wire-Re demonstrates acceptable THD and leakage current with only three inductors while eliminating the DC link connection.

TABLE VI
COMPARISON WITH OTHER METHODS

Topology/ Method	Filter Type	Number of Inductors	HF switches	Leakage current	THD	DC link-less
oH8 [23]	LC	3 5mH	8	352mA	5.07%	X
Scalar PWM [19]	L	3 4.3mH	6	460mA	4.98%	X
AZSPWM [19]	L	3 4.3mH	6	620mA	7.68%	X
Conventional lter [2]	LCL	3 3mH 3 347 H	6	1.06A	10%	X
4wire-Re [2]	LCL	3 3mH	6	93.3mA	4%	7
Proposed 3wire-Re	LCL	3 3mH	6	253mA	4%	X

VIII. CONCLUSION

The paper developed the concept of a recon gurable lter, named 3wire-Re, for PV inverter applications. The recon-gurable lter utilized a set of bidirectional switches that operated at twice the line frequency to alter the function of inductors, allowing them to switch roles between the grid side and the converter side. This recon guration of the lter presented various advantages not found in existing methods. The advantages included constructing LCL lter with a minimum number of inductors, reducing leakage current intrinsically, and easy installation capability. Although 3wire-Re had a higher leakage current compared to 4wire-Re, it met the leakage current standard. Moreover, inductor reduction led to cost savings and potentially a smaller overall size of the system. Furthermore, the proposed topology can provide inductive and capacitive reactive power. The paper provided mathematical models and analysis, equivalent circuits, and design guidelines to support the implementation of the proposed topology. Furthermore, the proposed topology was validated by experimental results which showed good compliance with grid codes such as THD and leakage current standards.

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