Parallel/Series Connected Standardized Active Switching Modules for High Power DCCBs in MVDC Networks

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***Abstract*— Solid-state DC Circuit Breakers (DCCBs) are increasingly employed across all power levels, including MVDC networks. Seamless integration of DCCBs into MVDC networks is challenging due to the diverse voltage and power levels and the varying network architectures associated with different applications. Furthermore, the limited current and voltage capability of semiconductor devices limits the full integration of solid-state DCCBs for MVDC applications. Series and parallel-connected IGBT arrays can be employed to match the current and voltage levels required. However, with passive gate drives, devices may fail due to non-homogeneous current and voltage distribution across IGBTs. Closed-loop Active Gate Drives (AGDs) provide a solution to overcome this.**

In the proposed standardized-Active Switching Module (ASM) scheme, IGBTs are equipped with AGDs with status feedback. This control method enables the IGBTs to follow a defined current/voltage trajectory during the switching rather than being guided by the inherent characteristics of the device and the circuit. Hence, with the ability to control dynamic current and voltage during switching, an additional degree of freedom is enabled to connect several ASMs in series and parallel. This allows us to match the DCCBs voltage and current capacities to that of the MVDC networks. DCCB architecture based on Standardized-ASMs is proposed as a flexible protection solution for MVDC networks. This paper describes the proposed AGD scheme, high-speed controller design, and behavioral analysis of the AGD-based ASMs. Experimental results show the dynamic voltage and current slope control capability of the proposed standardized ASMs. Finally, this paper assesses the ASM-based DCCB architecture for MVDC networks. An ASM-based DCCB prototype was developed and tested to verify the voltage and current sharing capability of modular ASMs in the proposed DCCB architecture.

***Index Terms*—Active Gate Drive, Current Balancing, DCCB, IGBTs, Voltage Balancing, MVDC**

I. Introduction

Due to their inherent advantages, MVDC networks are increasingly employed across various applications such as shipboard networks, MVDC collector grids, traction power networks, EV charging stations, and data center networks [1], [2], [3], [4]. The main advantages are better transfer capacity, improved flexibility and controllability, reduction of conversion stages, reduced cabling size, and ease of integration of renewable energy systems and energy storage systems. The MVDC voltages range from 1.5–50 kV DC and tens of MW across various applications [3], [4]. This enables the use of varying technologies at lower and high voltage ranges, giving flexibility in choosing the required topology. Furthermore, MVDC networks are mostly multi-terminal and meshed, improving the system's stability and reliability.

Reliable DC current breaking across a wide range of voltage and power levels remains challenging. Although several DC breaker topologies have been suggested in the literature, they lack the scalability and flexibility to serve across various applications involving different voltage and power levels.

DC Circuit Breakers (DCCBs) in MVDC applications are requisite to handle currents of up to several hundred amperes and voltages of several hundred kV, which exceeds the ratings of single IGBTs available [5], [6]. Furthermore, IGBTs employed in DCCBs undergo high fault current and Transient Interrupt Voltage (TIV) [7], [8]. Therefore, it is necessary to arrange multiple IGBT units in a combination of series and parallel configurations to accommodate the desired current and voltage ratings of MVDC networks [9], [10], [11]. Compared to the costly and bulky high-power IGBTs, multiple low-power IGBTs are more cost-effective and require less physical space [12]. A standardized-Active Switching Module (ASM) for parallel/Series connection in DCCBs to match the MVDC network requirements presents a protection solution to overcome these challenges.

Matched devices and gate drivers do not ensure dynamic current and voltage sharing between IGBTs in parallel/series connection. Passive snubber devices and Metal Oxide Varistor (MOV) arrangements are primarily employed in these stacked IGBT arrays to achieve voltage sharing between IGBTs and to dissipate the excess energy during transient interruption [8], [9], [12] The short circuit current during a fault is several times the rated current. Interrupting such high currents can result in high TIV [13], [14], [15]. The snubber capacitor value required is proportional to the square of device currents; Hence, the required capacitor has to be several times larger than during regular operation. The high-capacity, high-voltage snubbers are large and expensive, making them unviable for high-power IGBT-based DCCBs [13], [16]. Furthermore, snubber performance may deteriorate, leading to poor voltage sharing between series-connected IGBTs [17], [18].

MOVs are commonly used in DCCBs to dissipate energy during IGBT current interruption [8], [9], [10], [12]. However, MOVs are known to age due to repeated surge events and constant exposure to heat and humidity [8]. MOVs with voltage and surge ratings exceeding the normal operating voltage are specified to prevent failure, resulting in larger and more expensive components. [19]. Furthermore, IGBTs in DCCBs

are derated significantly to account for their non-homogenous voltage and current sharing. Ensuring homogenous voltage and current sharing is vital to advancing the development of DCCBs. This promotes the optimal use of IGBTs with minimal derating and increased ruggedness.

Closed-loop Active Gate Drive (AGD) techniques can compensate for non-linearities, temperature dependencies, and varying operating points of the IGBTs [20], [21]. Previous studies on AGDs focus on minimizing switching losses by minimizing the dead time and balancing the current distribution among IGBTs connected in parallel, which are primarily intended for high-frequency switching applications [20], [22], [23]. These AGD-based switching applications address the current unbalance over multiple switching cycles. This corrective process spans several switching cycles, during which the IGBTs may operate with notable unbalances. Consequently, the IGBTs need to be derated to accommodate these temporary unbalances. This approach does not apply to DCCBs.

Furthermore, prior to this study, no previous study has reported investigating the AGD techniques to balance both current and voltage among IGBTs in a modular array [10], [12], [23], [24], [25]. A summary of previous studies on AGDs and their target application is provided in *Appendix A*. Due to the delays of switching pulses caused by delay skews in the gate drive ICs and non-linearities in the IGBT devices, previous AGD schemes fall short when achieving both current and voltage balancing among IGBTs in DCCBs. Furthermore, unlike switching applications, delay time information between IGBTs is not available from previous switching cycles. The critical nature of DCCB requires immediate homogeneity of IGBT current and voltage. Unsynchronized switching, even by few ns, could result in cascaded failure of the IGBTs in the DCCB.

AGD scheme designed to achieve dynamic collector current (i_C) and collector-emitter voltage (v_{CE}) balance among IGBT arrays is required, with slowed down rate of change of collector current (di_C/dt) and rate of change of collector-emitter voltage (dv_{CE}/dt) to allow the synchronization of current and voltage slopes.

Specifically, the main contributions of this paper are as follows:

1. Closed-loop AGD is developed for dynamic di_C/dt and dv_{CE}/dt control during IGBT switching. A predefined di_C/dt and dv_{CE}/dt slopes are used to compensate for the gate drive delays and IGBT non-linearities.
2. Introduction of standardized ASM module with a scalable and reconfigurable DCCB architecture. These Standardized ASM modules can be connected in parallel/series to match the current and voltage levels of different MVDC networks.
3. The proposed DCCB architecture is evaluated using an ASM-DCCB prototype, demonstrating enhanced flexibility and seamless adaptation to diverse MVDC network requirements.

These enhancements offer greater flexibility to the DCCB architecture, facilitating seamless integration with various MVDC networks.

II. Proposed AGD Scheme

Control of the gate current to actively adjust the di_C/dt and dv_{CE}/dt during IGBT switching requires high-speed control action by the AGD. The designed AGD is implemented with high Bandwidth (BW) Op-Amps to achieve high control speed. Signal isolation stages are avoided in the proposed AGD scheme to prevent measurement delays.

The dynamic switching period must be extended to allow the current and voltage slopes to synchronize and compensate for the non-linearities and delay skews during IGBT switching. IGBT parasitic miller capacitance ($C_{GC,int}$) and gate-to-emitter capacitance ($C_{GE,int}$) are non-linear and voltage-dependent. In the proposed AGD scheme, an external gate-emitter capacitor ($C_{GE,ext}$), and an external miller capacitor ($C_{GC,ext}$) are connected across each IGBT, as shown in Fig. 1. $C_{GE,ext}$ adds to the gate-to-emitter capacitance and slows down di_C/dt without significantly affecting dv_{CE}/dt [26]. A damping resistor (R_D) is added to avoid oscillations between $C_{GE,ext}$ and $C_{GE,int}$. $C_{GC,ext}$ reduces the speed of dv_{CE}/dt without affecting the di_C/dt. External capacitances behave linearly over the voltage range and assist in more accurate di_C/dt and dv_{CE}/dt control. This increases the dynamic di_C/dt and dv_{CE}/dt control capability to achieve more homogeneous current and voltage profiles across the ASMs.

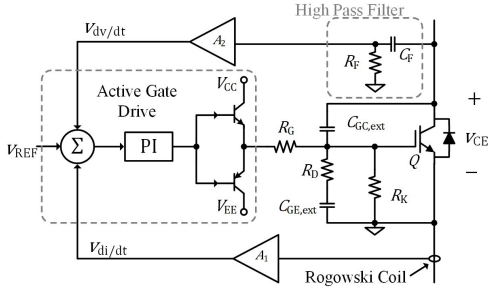


Fig. 1. Developed closed-loop Active Gate Drive (AGD).

$C_{GC,ext,}$ and $C_{GE,ext}$ increase total gate charge and switching losses [21], [26]. Nonetheless, this is not a drawback for DCCB applications. In DCCBs, the primary role of IGBTs is to operate during breaker turning ON/OFF, where they absorb the transient inrush current and TIV [8], [10], [27]. As with switching power applications, IGBTs are not expected to be continuously switched.

A. di_C/dt and dv_{CE}/dt sensing circuitry

An RC High Pass Filter (HPF) circuit measures the dv_{CE}/dt across the IGBT during IGBT switching. Using an RC passive circuit eliminates the requirement for additional high-speed voltage measurement and differentiator circuits. Filter resistance (R_F) and capacitance (C_F) are selected to achieve the required measurement BW.

When R_FC_F is small, the output voltage of HPF can be written as;

$$v_{HPF}(t) \approx R_F C_F \frac{dv_{CE}(t)}{dt} \tag{1}$$

Op-Amp Gain (A_1) amplifies the induced voltage.

$$v_{dv/dt} = -A_1 R_F C_F \frac{dv_{CE}(t)}{dt} \tag{2}$$

Previous studies on AGDs suggest using IGBT bond wire

inductance to measure the di_C/dt of IGBT [14], [21]. However, the bond wire inductance is contingent on the internal construction of the IGBT. Furthermore, high-power IGBTs are frequently packaged in multiple IGBTs, and the bond wire inductances can vary within the same package, which could lead to measurement errors. This study employs a PCB Rogowski coil to measure the di_C/dt through IGBT [28]. The induced voltage in the Rogowski coil terminal v_{ROG} is;

$$v_{\mathrm{ROG}} = -M\,\frac{di}{dt} \tag{3}$$

Here, M is the mutual inductance of the coil. Apart from mutual inductance, each coil turn has a parasitic capacitance between turns of the coil, resulting in many resonance points [28]. In regular operation, the Rogowski coil is only used at frequencies below the first resonance frequency. In this study, the Rogowski coil is designed to have a measurement BW of 20 MHz to capture sharp current changes during IGBT switching. High BW Op-Amp of gain (A_2) amplifies the induced voltage.

$$v_{\mathrm{di/dt}} = -A_2 M\,\frac{di}{dt} \tag{4}$$

B. Operating principle of the AGD

An AGD concept with automatic transitioning between di_C/dt and dv_{CE}/dt control is proposed in [21]. The AGD scheme proposed in this study employs a comparable automatic transition technique. dv_{CE}/dt and di_C/dt periods during IGBT switching appear in sequence without overlap [26]. i.e., di_C/dt is zero during the v_{CE} change period, and dv_{CE}/dt is zero during the i_C change period. Hence, combined di_C/dt and dv_{CE}/dt control loops can be implemented without actively selecting the control parameter. A combined control loop eliminates the complex circuitry requirement for the IGBT switching phase detection and high-speed signal multiplexing.

The implemented PI controller controls di_C/dt and dv_{CE}/dt during turning ON and OFF. Before the start of the switching cycle, the reference voltage, V_{REF} establishes the di_C/dt and dv_{CE}/dt. V_{REF}, combined with A_1, A_2, M, R_F, and C_F, defines the reference values for di_C/dt and dv_{CE}/dt control as in (5) and (6).

$$\left(\frac{di}{dt}\right)_{\mathrm{REF}} = -\frac{V_{\mathrm{REF}}}{A_2.M} \tag{5}$$

$$\left(\frac{dv}{dt}\right)_{\mathrm{REF}} = -\frac{V_{\mathrm{REF}}}{A_1 R_F.C_F} \tag{6}$$

According to (5) and (6), a positive value for V_{REF} initiates the turning ON of the IGBT (i.e., positive slope for i_C and negative slope for v_{CE}). Likewise, a negative value for V_{REF} initiates the IGBT turning OFF.

The proposed controller is only active during the dynamic voltage and current slope period. Hence, without di_C/dt and dv_{CE}/dt feedback, the AGD operates as a resistive GD during the steady state.

III. Hardware Prototype of ASMs and Test Setup

The proposed closed-loop AGD was implemented as an analog controller using high BW Op-Amps to achieve high control BW. AGD unit is referenced to the emitter of the IGBT. Standardized-ASM consists of IGBT, measurement circuits, and AGD as shown in Fig. 2. The ASM is isolated from the control unit using an isolated gate drive, and each ASM necessitates a dedicated isolated power supply for the AGD. V_{REF} for each ASM is set at the start of the switching cycle to achieve dynamic current and voltage balance Between ASMs.

A double pulse test setup (rated up to 560V and 60A) with an inductive load of 2.5mH is used for testing the AGD. Fig. 2 shows the schematic of the evaluating platform for the AGD.

Tests are carried out with ASMs connected in parallel and series arrays to test the independent voltage and current balancing capability of individual ASMs.

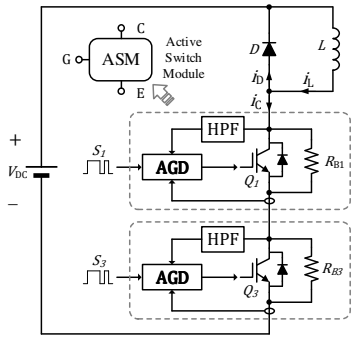


Fig. 2. Double pulse test setup for evaluating the AGD.

IV. Switching Behavior of ASMs

The switching behavior of the ASM is examined in this section. Different periods of IGBT switching are distinguished during IGBT turning ON and OFF for this analysis. Fig. 3 (a) and (b) show the voltage and current waveform trend during IGBT turning ON and OFF, respectively. Fig. 4 illustrates an equivalent circuit of the IGBT operating in the active region. During ASM turning ON and OFF, the progress of the IGBT operating point along the IGBT output characteristics and transfer characteristics is shown in Fig. 5 (a) and (b).

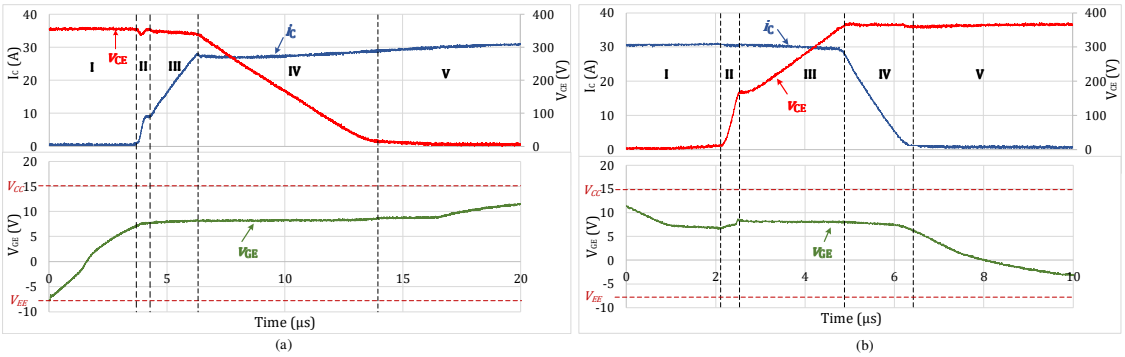


Fig. 3. Transient voltage and current waveforms during (a) ASM turning ON (b) ASM turning OFF.

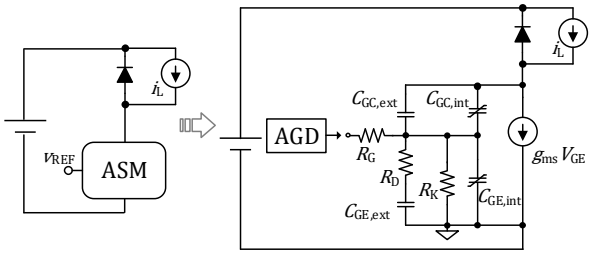


Fig. 4. Equivalent circuit of an IGBT operating in the active region during ASM switching.

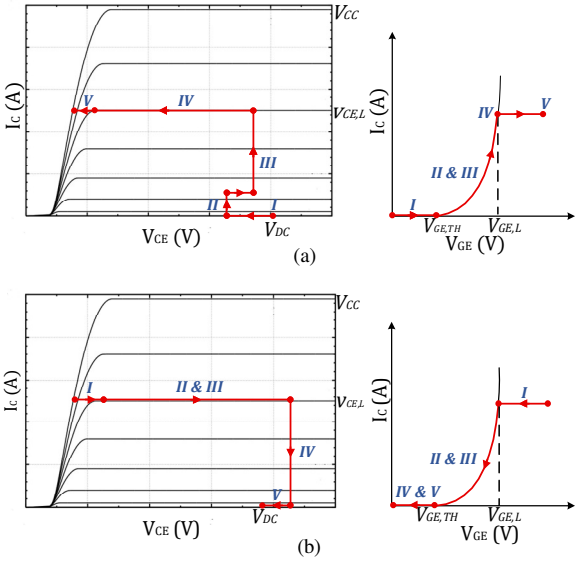


Fig. 5. Progress of operating point in IGBT output and transfer characteristics during (a) ASM turning ON, (b) ASM turning OFF.

As shown in Fig. 3 (a), ASM turning ON can be characterized into five stages for analysis. *Stages III* and *IV* are the IGBT's active current and voltage slope control periods. Similarly, ASM turning OFF can be identified into five stages, as shown in Fig. 3 (b). In *stages III* and *IV*, the AGD controls the voltage and current slopes, as determined by the voltage slope reference, $(dv/dt)_{REF}$, and current slope reference, $(di/dt)_{REF}$, respectively.

A comprehensive behavioral analysis of ASM during its switching ON and OFF, along with the equations that govern the switching of ASM, can be found in *Appendix B*.

A. Control of di_C/dt and dv_{CE}/dt

The first series of experiments examines the independent di_C/dt and dv_{CE}/dt control capability of AGD with different $(di/dt)_{REF}$ and $(dv/dt)_{REF}$ values. Different $(di/dt)_{REF}$ and $(dv/dt)_{REF}$ settings were applied by adjusting V_{REF}. Fig. 6 (a) and (b) show the measurements for ASM turning ON and OFF with different V_{REF} values.

The measured results demonstrate the capability of AGD to independently adjust the di_C/dt and dv_{CE}/dt during IGBT switching. It can also be observed that the current overshoots occur when the IGBT turn ON before the controller achieves the desired di_C/dt, and the overshoot increases with the increasing $(di/dt)_{REF}$. Similarly, voltage overshoot can be observed during IGBT turn-off before the AGD achieves the desired voltage slope defined by the $(dv/dt)_{REF}$. Hence, selecting $(di/dt)_{REF}$ and $(dv/dt)_{REF}$ values results in minimal current and voltage overshoot, especially when multiple ASMs are arranged in an array.

B. Voltage and current slope control limits

Voltage and current slope magnitude depend on how fast the gate and miller capacitors are charged and discharged during IGBT switching. IGBTs incur high switching loss in the active region and undergo high stress. It may easily lead to hot-spotting and current hogging within the die, leading to the IGBT's linear mode failure [29]. Hence, Forward Safe Operating Area (FSOA) limits provided by the manufacturers must be adhered. Power IGBTs can operate in the active region from several hundred µs to a few ms below its rated current and voltage [20], [21], [29]. FSOA of the IGBT is essential in determining the minimum di_C/dt and dv_{CE}/dt limit of the IGBT.

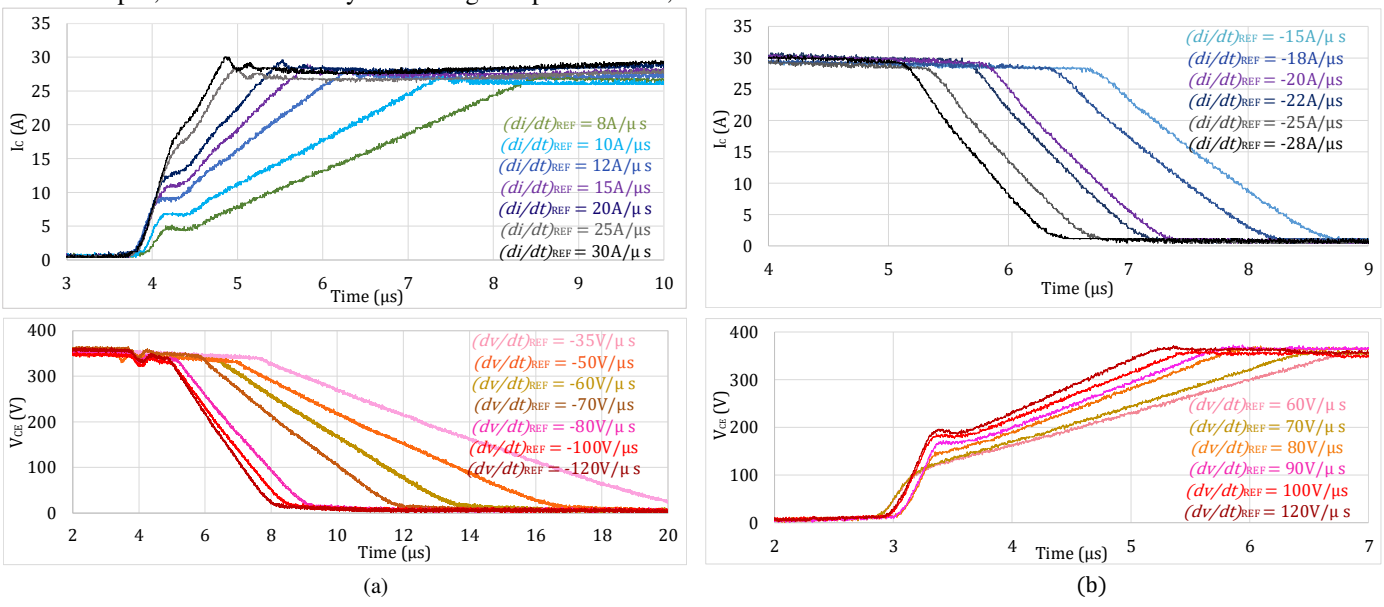


Fig. 6. Collector current (i_C) and collector-emitter voltage (v_{CE}) with different V_{REF} during (a) IGBT turning ON, (b) IGBT turning OFF.

C. Controller modeling and the bandwidth of the PI controller.

The PI controller of the proposed AGD is designed using high BW, high slew rate Op-Amp with rail-rail voltage of ±15V, followed by a high-speed amplifier stage to drive the IGBT gate. From the control perspective, the transfer function of the IGBT in the active region operation varies depending on the switching stage. Fig. 7 shows the block diagram for the closed loop transfer function for voltage slope and current slope control. $G_{dv/dt}(s)$ and $G_{di/dt}(s)$ correspond to the small signal transfer functions of the IGBT and external gate capacitors during periods of voltage and current slope of the IGBT. A small signal model valid for active region operation is extensively discussed in previous literature [24], [30], [31] and can be used to derive the transfer function $G_{dv/dt}(s)$ and $G_{di/dt}(s)$. $H_{di/dt}(s)$ and $H_{dv/dt}(s)$ are feedback gains for *di/dt* and *dv/dt* measurement. $G_C(s)$ and $G_A(s)$ are the transfer functions of the controller and amplification stage, respectively.

The Bode diagram of the PI controller and amplifier frequency response is shown in Fig. 8. The designed PI controller and amplifier stage have a control BW of 4 MHz.

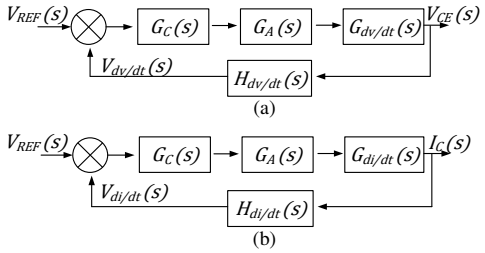


Fig. 7. Block diagram for closed-loop transfer function for (a) voltage slope and (b) current slope control.

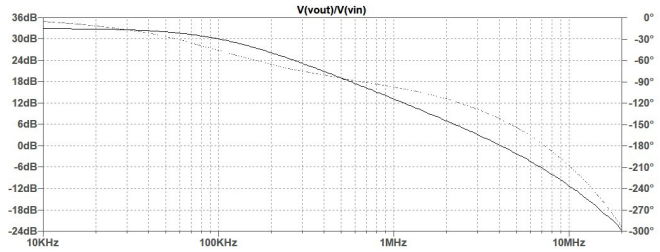


Fig. 8. Bode diagram of the PI controller and Amplifier frequency response.

V. Voltage and Current Balancing in ASMs

The AGD regulates the di_C/dt and dv_{CE}/dt during IGBT switching, facilitating dynamic voltage and current balance between ASMs. This eliminates the dependence on non-linearities and differences in the operating points of the IGBTS and allows for compensating gate drive delays between ASM modules.

A. Voltage balancing in series ASMs

The limited voltage ratings of IGBTs require connecting several ASMs in series for MV DCCBs. Equal voltage between series-connected ASMs in dynamic and steady state is vital for the safe operation of the proposed DCCB architecture. Voltage balance in a steady state can be achieved using static voltage balancing resistors (R_B), (See Fig. 2). Differences in internal parameters such as C_{GE}, C_{GC}, C_{CE}, and R_g result in voltage unbalance between IGBTs connected in series during switching. Other factors that affect uneven voltage sharing include delay skew between gate drives and differences in stray inductance and capacitance in the circuit.

Conventional passive snubber circuits cannot achieve homogenous voltages between IGBTs, requiring a significant derating of the IGBTs. Active gate clamping circuits are widely proposed to suppress overvoltage and ensure voltage balance between series devices [15], [32]. Active clamping utilizes an avalanche-based semiconductor device to provide direct feedback of collector voltage to IGBT gates. Due to the direct feedback of the collector voltage to the gate, bypassing control circuits and gate drives, active clamping circuits may lead to high voltage overshoots, unbalances, and device failures.

In previous AGD switching applications, desired voltage slope control is often achieved using iterative approaches over several switching cycles [25], [30], [33]. Hence, they are not applicable to DCCB applications.

In a series-connected ASM array (Fig. 9 (a)), dynamic voltage sharing is achieved by controlling the dv_{CE}/dt of ASMs. With AGD action, unbalances due to device parasitics are eliminated, and the ASMs share voltage during switching.

Fig. 10 (a) and (b) show the voltage sharing between two series ASMs turning OFF and ON, respectively. ASM achieves a preset slowed-down voltage slope in a series arrangement to ensure a synchronized voltage slope during the switching dynamics. Moreover, when the ASM is turned on, the regulated voltage slope guarantees that the voltage across the ASMs is brought to zero in unison, as depicted in Fig. 10 (b).

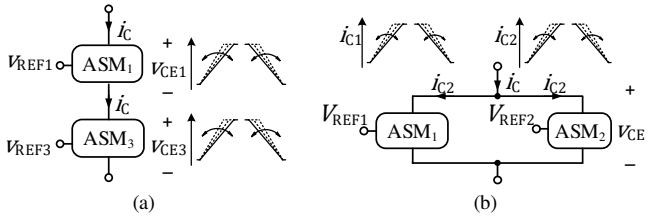


Fig. 9. Connection of ASMs in (a) Series and (b) Parallel.

B. Current balancing in parallel ASMs

In the conduction state, disparities in v_{CE} among parallel-connected IGBTs lead to an unbalance in the current flowing through these IGBTs. Hence, it is vital to minimize the difference in v_{CE}.

When connecting IGBTs in parallel, it is imperative to use devices of the same production batch to keep v_{CE} difference to a minimum [34], [35]. In addition, parasitic resistance that exists in the PCBs and wiring paths affects the current balancing between parallel connected IGBTs. To mitigate current unbalances, PCB layouts should be designed with symmetry in mind to ensure that the parasitic resistances in the paths are the same.

The output characteristics of an IGBT are temperature-dependent. Hence, the current unbalance of the IGBTs varies according to the device temperature. In a parallel connected IGBT arrangement, positive temperature dependence stabilizes current unbalance. As the temperature increases, the IGBT with a higher current will experience a slightly larger rise in on-state voltage drop, which helps counteract current unbalances, thus promoting more even current sharing among the parallel-

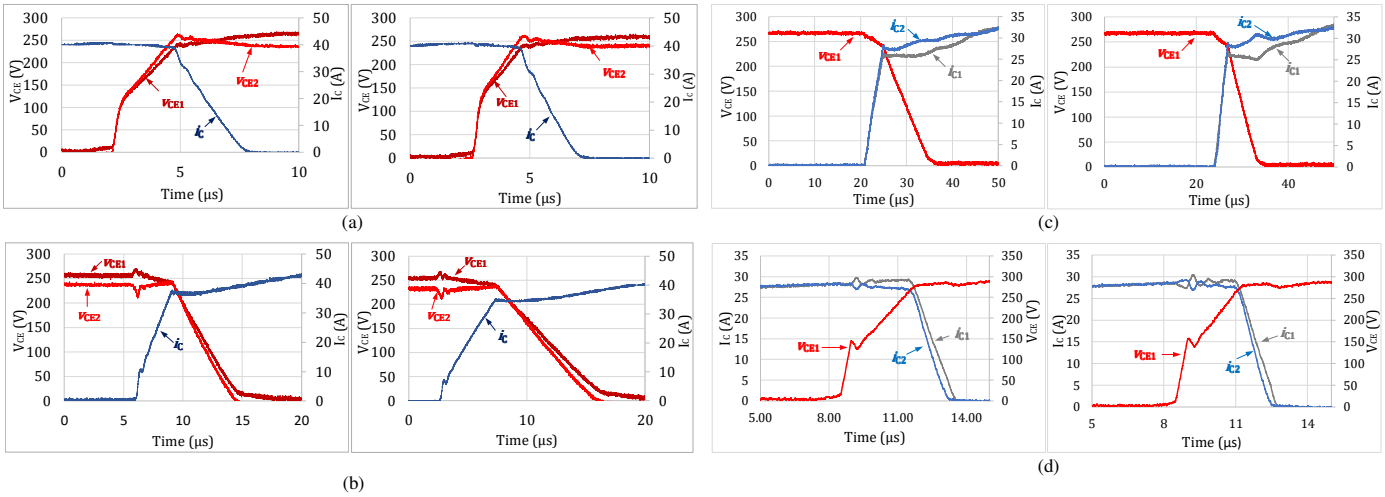


Fig. 10. Voltage sharing between two series connected ASMs, with different $(dv/dt)_{REF}$, during (a) turning OFF, (b) turning ON. Current sharing between two parallel connected ASMs with different $(di/dt)_{REF}$ during (c) turning ON, (d) turning OFF.

connected devices [34], [36]. For parallel IGBTs, it is recommended to use the IGBTs in the positive temperature-dependent range [36].

Dynamic current unbalance during IGBT switching is mainly caused by different delay times in gate drives and optical isolators and different tolerances of IGBT parameters [29].

In switching applications using AGDs for current balancing between parallel connected IGBTs, current unbalance is addressed over a period of several switching cycles. Initial unbalance is measured in the IGBTs, and the di/dt is adjusted accordingly to nullify the dynamic unbalance. This corrective action takes several switching cycles, and the IGBTs operate with significant unbalances for several switching cycles. This requires the IGBTs to be derated to cater to the temporary unbalance.

In contrast, in DCCBs, we focus on one critical switching instance. Furthermore, the MB unit of the DCCB needs to be sized to handle the short circuit current of the network and resulting TIV. Hence, semiconductor devices have a significantly higher cost, necessitating optimal current and voltage capacity use.

Using the proposed AGD-based ASMs, the current slope during ASM switching can be dynamically controlled to achieve the dynamic current balance between parallel ASMs.

Two parallel ASMs (Fig. 9 (b)) are tested in the double pulse test setup. Fig. 10 (c) and (d) show the current sharing between two parallel connected ASMs when turning ON and OFF, respectively. ASM_1 and ASM_2 share current with minimal current unbalance during switching. This demonstrates the ability of the proposed ASM scheme to attain dynamic current balance while maintaining predefined $(di/dt)_{REF}$.

VI. Standardized-ASM Based DCCB Architecture: Operating Principle and Experimental Results.

A Hybrid DCCB configuration featuring a Mechanical Switch (MS) and a Current Commutation Switch (CCS) within the primary conduction branch is utilized in this study. The Main Breaker (MB) unit is the current making/breaking unit that turns ON and OFF during DCCB operation.

Fig. 11 (a) illustrates the schematic of the hybrid type DCCB. The turn ON and OFF sequences of the hybrid DCCB are presented in Fig. 11 (b) and (c), respectively.

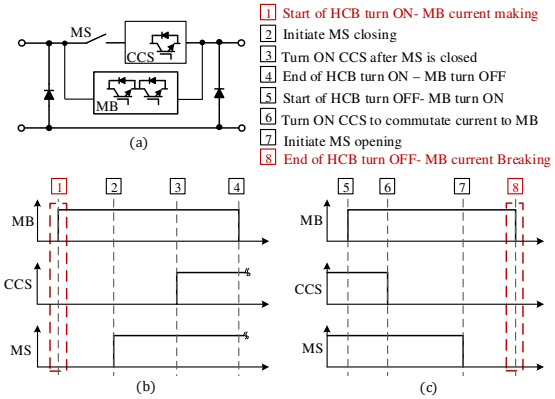


Fig. 11. Hybrid DCCB (a) Structure, (b) Turn ON, and (c) OFF sequences.

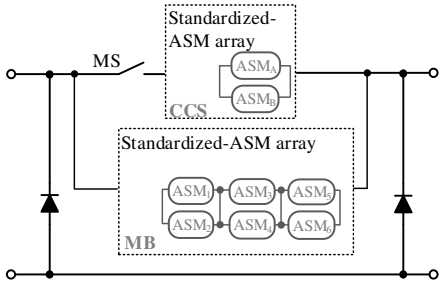
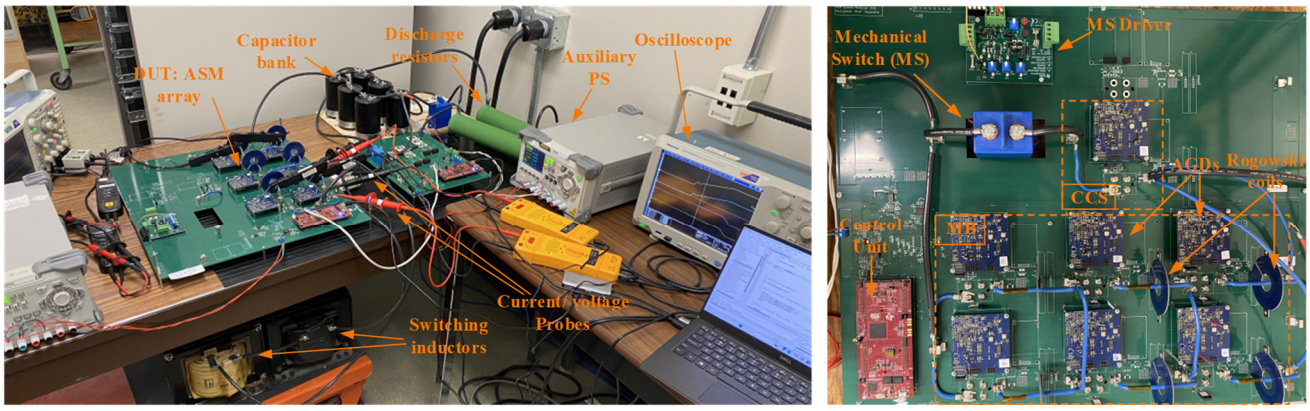


Fig. 12. Standardized-ASM based Hybrid DCCB architecture.

Dynamic current and voltage slopes are evident across MB during DCCB turn ON and OFF instances. Corresponding switching instances are highlighted in Fig. 11 (b) and (c). The MB undergoes TIV and high current stress during these instances. These two instances are the only switching instances where the MB undergoes high voltage and current stress, so testing the DCCBs under this section is primarily concentrated on these instances.

The proposed DCCB architecture allows scalability by the addition of standardized-ASM units in series and parallel, as shown in Fig. 12. This scalability can be tailored to meet the



(a) (b)

Fig. 13. (a) Experimental setup for the pulse current testing of the MB unit of the DCCB, (b) 2kV/100A rated DCCB prototype.

application's specific voltage and power level demands. With a wide range of MVDC applications demanding varying voltage and power levels, the scalable DCCB architecture using standardized ASMs provides a flexible DC protection solution.

A DCCB prototype with a rating of 2kV/100A was developed to evaluate the performance of ASMs in the proposed DCCB architecture (Fig. 13 (b)). The experimental setup for pulse current testing is shown in Fig. 13 (a). Testing of DCCBs over the full range of operating conditions requires a source capable of sourcing short circuit fault current under the rated voltage, which is impractical. Hence, DCCB testing is carried out using two different test scenarios:

1) DCCB high voltage testing for ASM voltage sharing operation during DCCB turn ON and OFF.

2) Double pulse current testing of the MB to evaluate ASM current and voltage sharing operation at the rated voltage and current.

The schematic of the two test setups is shown in Fig. 14 (a) and (b).

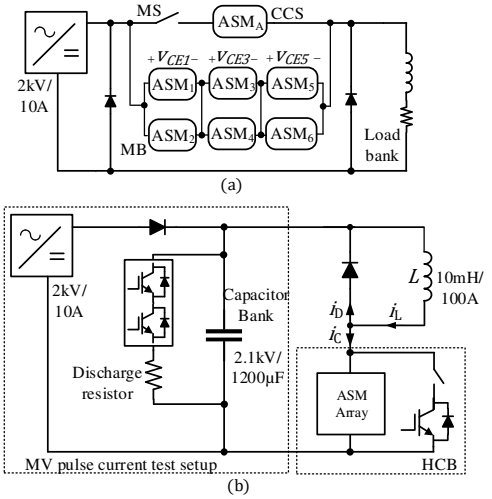


Fig. 14. Test setup for the (a) DCCB high voltage testing and (b) Double pulse testing of the MB of the DCCB at rated voltage and current.

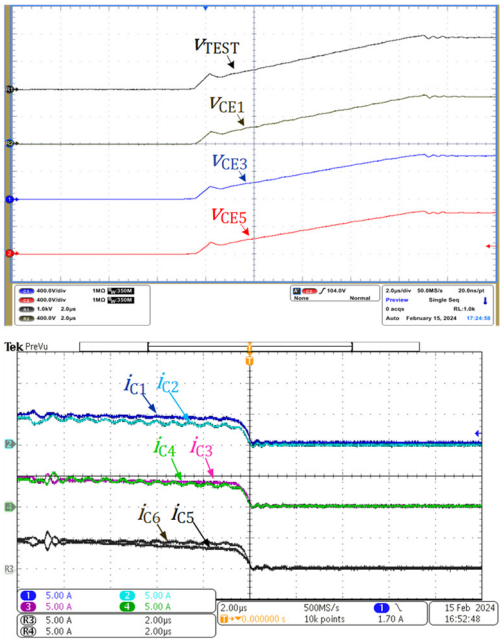


Fig. 15. Voltage and current sharing between ASMs during MB turn OFF in the course of DCCB turn OFF.

A. ASM-DCCB high-voltage testing

ASM-based DCCB is tested in a 2kV/10A test setup to examine the voltage and current sharing operation of ASMs during DCCB operation (see Fig. 14 (a)).

Fig. 15 shows the voltage sharing between series connected ASMs and the current sharing between each parallel ASM pair during MB turn OFF. Specifically, at DCCB turn OFF with inductive loads. The inclusion of freewheeling diodes suppresses the TIV during the DCCB turn OFF. Fig. 16 shows the voltage and current sharing between ASM units in the MB during turn ON. A non-inductive load is employed in this test to assess the current sharing capability during fast current rise via the MB unit.

The experiment results illustrate the capability of the ASM modules in the DCCB to share the voltage and current stress during breaker turning ON and OFF while adhering to the designated switching sequence of the DCCB.

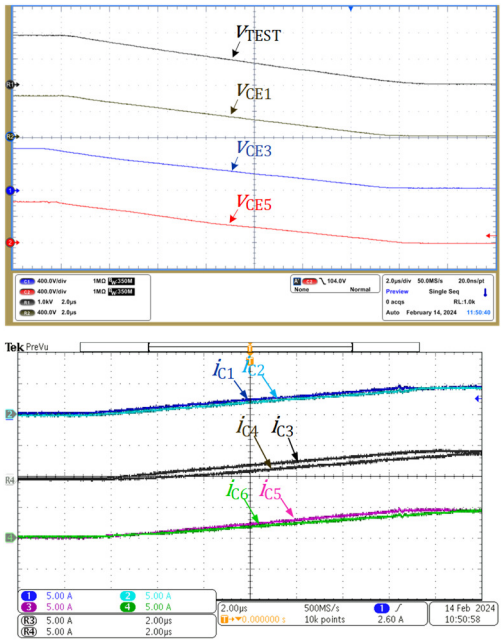


Fig. 16. Voltage and current sharing between ASMs during MB turn ON in the course of DCCB turn ON.

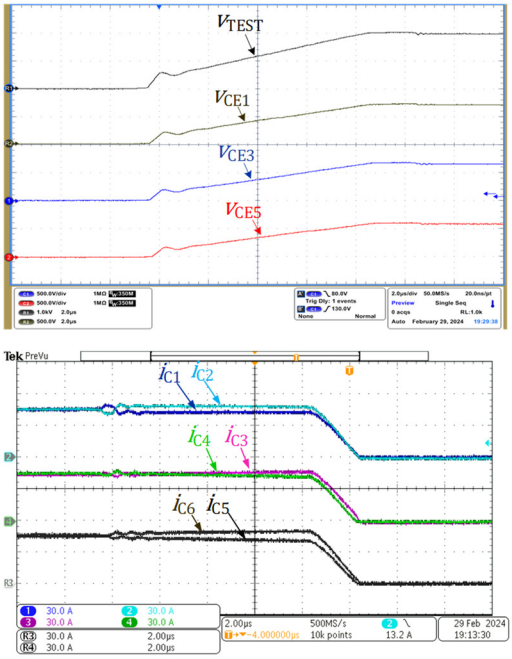


Fig. 17. Voltage and current sharing between ASMs during MB turn OFF in double pulse switching at rated voltage and current (2kV/100A).

B. DCCB - MB double pulse testing at rated voltage and current.

Fig. 17 and Fig. 18 show the experimental results for MB pulse current testing at rated 2kV/100A. During both turn OFF and ON dynamics, the test voltage of 2kV is shared equally among three series-connected ASMs of the MB. Similarly, during the dynamic current rise and falling stages, the test current of 100A is shared equally among all three pairs of ASMs.

The test results demonstrate the homogeneous current and voltage distribution among the ASMs with minimal deviations, indicating robust current and voltage-sharing capabilities. At rated capacity, The di_C/dt and dv_{CE}/dt control period is approximately 12 µs, which is well within the SAO requirements of each IGBT.

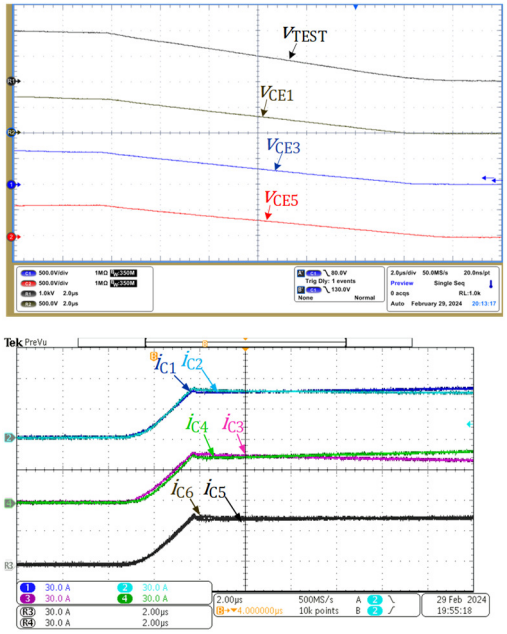


Fig. 18. Voltage and current sharing between ASMs during MB turn ON in double pulse switching at rated voltage and current (2kV/100A).

VIII. Conclusions

Dynamic di_C/dt and dv_{CE}/dt control technique is presented to attain equal voltage and current sharing between IGBTs. The experimental results show the fast and accurate di_C/dt and dv_{CE}/dt control capability of the proposed Active Gate Drive (AGD), independent of the IGBT parameter variations and non-linearities.

The high BW analog controller employed in the AGD allows swift control of the IGBT switching in the sub-microsecond range. Although operating the IGBTs in the active region for extended periods can damage the IGBT, accurate and reliable di_C/dt and dv_{CE}/dt control capability allows for adherence to the FSOA requirements of the IGBTs during active region operation.

A series of tests were conducted to validate the suitability of the proposed Standardized-Active Switching Modules (ASMs) in achieving voltage and current sharing. ASM-based Direct Current Circuit Breaker (DCCB) architecture is proposed to accommodate the diverse voltage and current requirements of modern MVDC networks. The ASM-DCCB prototype, comprising modular ASMs in the MB was tested under different test scenarios. The experimental result demonstrates the dynamic current and voltage-sharing capability of the ASMs within the DCCB configuration. The demonstrated homogeneous current and voltage sharing capability of the ASMs underscores the reliability of the proposed scheme for MVDC applications. Moreover, the proposed ASM-DCCB architecture facilitates scalability to accommodate varying power requirements while minimizing IGBT derating.

Steady-state current unbalance within parallel connected ASMs cannot be compensated using the proposed AGD scheme, which remains a subject for future research that

requires attention. Furthermore, ASMs can limit the fast current rise in the event of a fault, and self-fault protection actions implemented via ASMs require further investigation. These actions might involve internal diagnostics to detect faults and implementing shutdown procedures to mitigate the effects of the fault.

Future research endeavors will further explore the applications of standardized ASM arrays in high-power MV DCCBs to enhance their voltage and current handling capacities. The steady-state current sharing capability of ASMs, especially in thermal steady state, needs to be evaluated. Standardized-ASM based DCCBs are envisaged to facilitate flexible protection solutions for MVDC networks with their scalability and reliable, current interruption capability.

APPENDIX A

Table 1. Previous studies on AGD schemes and proposed applications

AGD Scheme	Remarks	Applications
Open loop AGD using switchable gate resistors [26], current sources [37], and voltage sources [38]	• Specific gate resistor, current source, or voltage source are applied in each interval to obtain desired switching characteristics. • IGBT non-linearities and temperature dependencies cannot be compensated.	• Pulsed power applications such as motor drives. • Fine-tune the switching performance regarding efficiency, radiated emissions, and diode recovery spikes.
AGD with direct cascaded control of v_{CE}, dv_{CE}/dt and v_{GE} with a voltage feedback loop [30]	• AGD can set the dv_{CE}/dt and implement an overvoltage clamping function using the reference. • The IGBT turn ON phase can be characterized by reference variable ramps.	• Reduction of switching losses in pulsed power applications. • IGBT voltage balancing in series operation.
AGD scheme with i_C and v_{CE} feedback loop [25]	• The v_{CE} and i_C values are sampled by ADCs, and the digital controller calculates the gate voltage profile. • Iterative and adaptive control methodologies are utilized to compensate for the delays. • Requires complex control and measurement circuitry.	• Power optimal digital slew rate control scheme for high-power industrial and automotive applications. • Desired voltage and current slopes are achieved over a few switching cycles. Not applicable to DCCBs.
AGD scheme, with i_C and v_{CE} feedback, which uses complementary current sources to inject extra drive current [33].	• Specific transient switching stages are accelerated by injecting gate current via the complementary current source, leading to higher switching speed and lower switching loss of the IGBT.	• Switching performance improvement and overvoltage protection of high-power IGBTs. • Not intended for applications with series and parallel IGBT modules.
AGD scheme with v_{CE} feedback and i_C estimation via bond wire voltage drop [31].	• Voltage drop via bond wire inductance is used to estimate the i_C. • The current balance is achieved over several switching cycles and is not suitable for DCCB applications.	• Static current balancing in IGBTs for PWM applications.
AGD scheme with di_C/dt and dv_{CE}/dt feedback [21]	• Extended gate current control. • Parallel connected IGBTs are daisy-chained and require a few cycles to determine the required delay compensation for the current balance.	• Current balancing in parallel connected IGBTs using delay time compensation. • Short circuit detection and turn-off . • For IGBTs in bridge leg configuration, minimize output voltage distortion by the reciprocal interlocking of the complimentary IGBTs.

APPENDIX B

A. ASM turning On behavior

Stage I: Gate charge delay period – Initiates the charging of the IGBT input capacitance, C_{ies}. i.e., C_{GE} is charged while C_{GC} is discharged. The IGBT is blocked while v_{GE} stays below the threshold voltage, $v_{GE,th}$. When the v_{GE} reaches $v_{GE,th}$ the IGBT starts to conduct current according to its transfer characteristics. Until this point, AGD behaves as a resistive GD; Therefore, the equations that describe the behavior of the IGBT with a resistive GD remain applicable up to this juncture. For the charging of an RC circuit using a resistive gate drive,

$$v_{GE}(t) = V_{CC}\left[1 - e^{-t/\tau_G}\right] \tag{B1}$$

$$i_G(t) = \frac{V_{CC} - v_{GE}(t)}{R_G + R_D} \tag{B2}$$

Here τ_G is the time constant of the equivalent circuit. $i_G(t)$ is the instantaneous gate current. $C_{GE,int}$, R_D, and $C_{GE,ext}$ make up a second-order low-pass filter with two different time constants τ_1 and τ_2. When we take the output across $C_{GE,int}$ we have a system with two poles and a zero. By using the method of open circuit time constant.

$$\tau_1 = R_G C_{GE,int} \tag{B3}$$

$$\tau_2 = [R_G + R_D] C_{GE,ext} \tag{B4}$$

Considering $C_{GE,ext}$ is several times larger than $C_{GE,int}$, for simplicity of analysis, we can consider the circuit time constant.

$$\tau_g = \tau_2 = [R_G + R_D] C_{GE,ext} \tag{B5}$$

Stage II: Current overshoot period – Due to the absence of di_C/dt feedback, the AGD behaves as a resistive GD. As a result, $i_C(t)$ experiences a rapid increase. However, AGD receives di_C/dt feedback and assumes control over the di_C/dt rate.

The collector current is defined using the static transfer characteristics of the IGBT. g_{ms} is the IGBT transconductance.

$$ic(t) = g_{ms}\left[V_G(t) - V_{GE,th}\right] \tag{B6}$$

$$\frac{di_C(t)}{dt} = g_{ms}\left[\frac{dV_{GE}(t)}{dt}\right] = g_{ms}\left[\frac{i_G(t)}{C_{ies}}\right]$$

$$\approx g_{ms}\left[\frac{i_{\mathrm{G}}(t)}{C_{\mathrm{GE,int}}+C_{\mathrm{GE,ext}}}\right] \quad \text{(B7)}$$

Stage III: Active current slope control period – AGD controls the collector current rise as set by the $(di/dt)_{\mathrm{REF}}$. As the IGBT remains within its active region, the equation (B7) governing the di_C/dt from the previous stage remains applicable.

$(di/dt)_{\mathrm{REF}}$ determines the $i_G(t)$ during this stage. The drive voltage of the AGD, V_{AGD}, replaces the V_{CC} in equation (B2) for calculating $i_G(t)$.

$$i_{\mathrm{G}}(t)=\frac{V_{\mathrm{AGD}}-v_{\mathrm{GE}}(t)}{R_{\mathrm{G}}+R_{\mathrm{D}}} \quad \text{(B8)}$$

The gate voltage is a function of threshold voltage, $V_{GE,th}$, and instantaneous collector current, $i_C(t)$, during this period.

$$v_{\mathrm{GE}}(t)=V_{\mathrm{GE,th}}+\frac{i_{\mathrm{C}}(t)}{g_{ms}} \quad \text{(B9)}$$

Stage IV: *Active voltage slope control period* – After the collector current reaches load current I_{L}, the i_{C} is constant. Hence, gate voltage stays clamped to $v_{\mathrm{GE,th}}+\frac{I_{\mathrm{L}}}{g_{ms}}$. The gate current only discharges C_{GC} and leads to the decay of V_{CE}.

$$\frac{dv_{\mathrm{CE}}(t)}{dt}=-\left[\frac{dv_{\mathrm{GC}}(t)}{dt}\right]=-\left[\frac{i_{\mathrm{G}}(t)}{C_{\mathrm{GC}}}\right]$$
$$=-\left[\frac{v_{\mathrm{AGD}}-(V_{\mathrm{GE,th}}+\frac{I_{\mathrm{L}}}{g_{ms}})}{R_{\mathrm{G}}}\right]\frac{1}{C_{\mathrm{GC}}} \quad \text{(B10)}$$

AGD automatically adjusts v_{AGD} to attain the set voltage slope. Here, C_{GC} is the sum of internal and external miller capacitors.

$$C_{\mathrm{GC}}=C_{\mathrm{GC,int}}+C_{\mathrm{GC,ext}} \quad \text{(B11)}$$

Stage V: *Gate charge period* - When the v_{GE} reaches zero, IGBT moves to the saturation region of operation, and the gate voltage continues to increase to V_{CC}.

B. ASM turning OFF behavior

Stage I: *Gate discharge delay* – When the negative V_{REF} is applied to the ASM it initiates the IGBT turn OFF. v_{GE} starts decaying, and the IGBT enters the active region. AGD does not receive dv/dt feedback; therefore, ASM operates as an IGBT with a resistive gate drive during this period.

The mathematical equations governing the turning OFF process are similar to the turning ON process. The IGBT input capacitor C_{ies} is discharged, and gate voltage $v_{\mathrm{GE}}(t)$ can be calculated from

$$v_{\mathrm{GE}}(t)=V_{\mathrm{EE}}\left[1-e^{-t/\tau_G}\right] \quad \text{(B12)}$$

Gate current can be calculated from

$$i_{\mathrm{G}}(t)=\frac{V_{\mathrm{EE}}-v_{\mathrm{GE}}(t)}{R_{\mathrm{G}}+R_{\mathrm{d}}} \quad \text{(B13)}$$

Stage II: *Voltage overshoot period* – Initially, due to the absence of the dv/dt feedback, voltage rise is rapid until AGD gains control over the dv/dt rate of the IGBT. The IGBT switching equations with resistive GD are valid in this region.

When the gate voltage reaches the minimum value to carry the load current, which is $V_{\mathrm{GE,th}}+\frac{I_{\mathrm{L}}}{g_{ms}}$, IGBT enters the active region

Gate current only charges C_{GC} and leads to the rise in V_{CE}.

$$\frac{dv_{\mathrm{CE}}(t)}{dt}=-\left[\frac{dv_{\mathrm{GC}}(t)}{dt}\right]=-\left[\frac{i_{\mathrm{G}}(t)}{C_{\mathrm{GC}}}\right]$$
$$=-\left[\frac{V_{\mathrm{EE}}-V_{\mathrm{GE,th}}-\frac{I_{\mathrm{L}}}{g_{ms}}}{R_{\mathrm{G}}}\right]\left[\frac{1}{C_{\mathrm{GC,int}}+C_{\mathrm{GC,ext}}}\right] \quad \text{(B14)}$$

Stage III: *Active voltage slope control stage* – AGD controls the voltage rise as set by $(dv/dt)_{\mathrm{REF}}$. Since the IGBT is still in the active region, mathematical equations describing $dv_{\mathrm{CE}}(t)/dt$ in the previous stage are still valid. However, $i_{\mathrm{G}}(t)$ is determined by the $(dv/dt)_{\mathrm{REF}}$. Hence, drive voltage v_{AGD} replaces V_{EE} in equation (B13) for calculating $i_{\mathrm{G}}(t)$.

$$\frac{dv_{\mathrm{CE}}(t)}{dt}=-\left[\frac{v_{\mathrm{AGD}}-V_{\mathrm{GE,th}}-\frac{I_{\mathrm{L}}}{g_{ms}}}{R_{\mathrm{G}}}\right]\times\left[\frac{1}{C_{\mathrm{GC,int}}+C_{\mathrm{GC,ext}}}\right] \quad \text{(B15)}$$

Stage IV: *Active current slope control stage* – AGD controls the collector current rise set by the $(di/dt)_{\mathrm{REF}}$. The IGBTs static transfer characteristics define the IGBT collector current as in (B6). The rate of change of collector current can be calculated from (B7). Similar to when the IGBT turns ON, $i_{\mathrm{G}}(t)$ can be calculated from (B8). The gate voltage is a function of threshold voltage and collector current and can be calculated from (B9).

Stage V: *Tail current and gate discharge* – The collector current reaches the level of tail current. Therefore, cannot actively be reduced further by AGD, and solely relies on the IGBT characteristics and other external passives. The tail current decays and after V_{GE} decreases until it reaches V_{EE}.

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