Real Time Digital Simulation of Electric Power Systems

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1

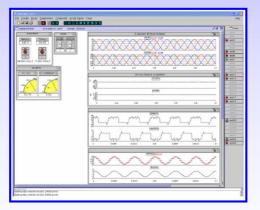
Real time digital simulation for the power industry

Real Time Digital Simulation of HVDC Systems

Presentation Outline

- Theory of Parallel Computation for Power Systems
- Overall Introduction of Real Time Simulation
- The Solution Structure of Real Time Simulation: Parallel Processing
- Differences between Real Time and Non Real Time Simulation
 - No Interpolation
 - No Iteration
 - Model Simplification
 - Small Time Step Solution
 - Surrogate Network
- Questions and Answers





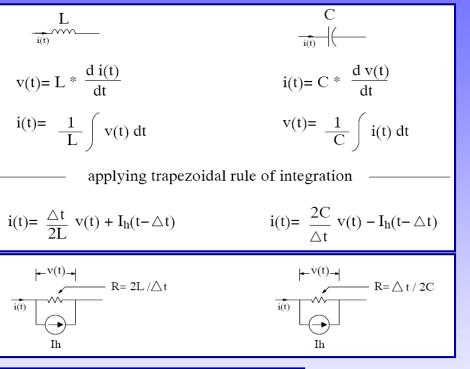


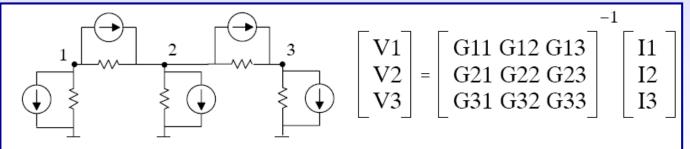


EMT Theory

Real Time Digital Simulation

- Electromagnetic transient solution (EMTP type simulation)
 - Based on the *Dommel* algorithm
 - Trapezoidal rule of integration
 - New solution produced each timestep





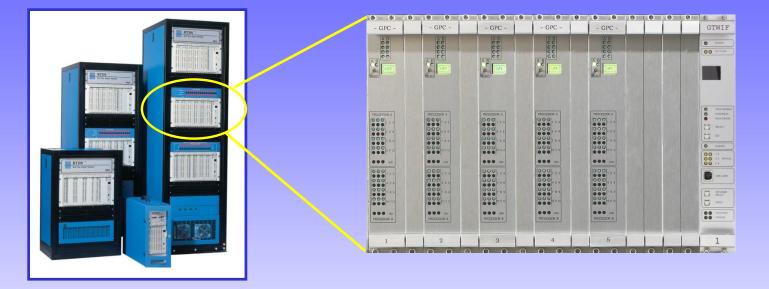


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Technologies

Simulation Hardware

A Rack:



A unit of hardware is called a '*Rack'* and typically includes:

- 1~6 RISC Processor Card (PB5)
- 1 Giga Transceiver Workstation InterFace Card (GTWIF)

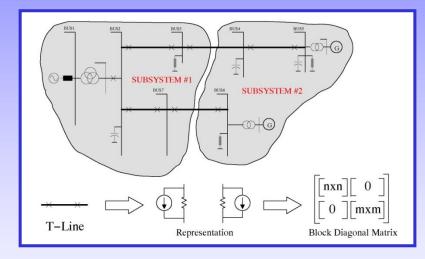


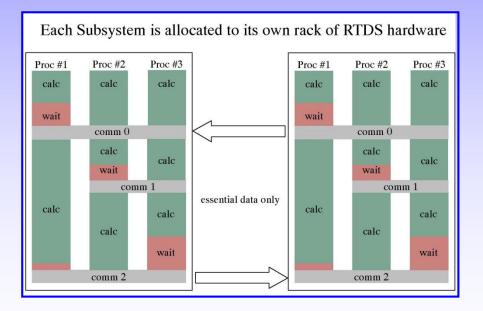


Network Splitting

Splitting the Network into Subsystems:

As the network gets bigger the size of the conductance matrix also increases (one matrix element per system node).





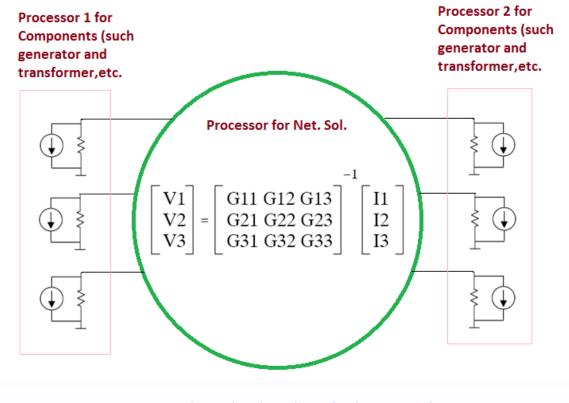




Solution Structure

Balance between Efficiency and Flexibility:

One of Two Processors Per Rack Exclusively Used for Network Solution Other Processors Used for Component







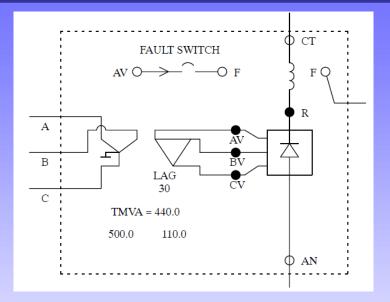
Power System Components

An Example: Six Pulse Valve Group Model in RTDS

- Embedded Model
- With internal faults included
- Improved firing function
- Be used and verified for over 10 years
- Developed based on close relationship with world leading manufactures

External Nodes vs Internal Nodes

- External nodes connect the network solution
- Internal nodes be eliminated
- The purpose is to minimize the number of nodes





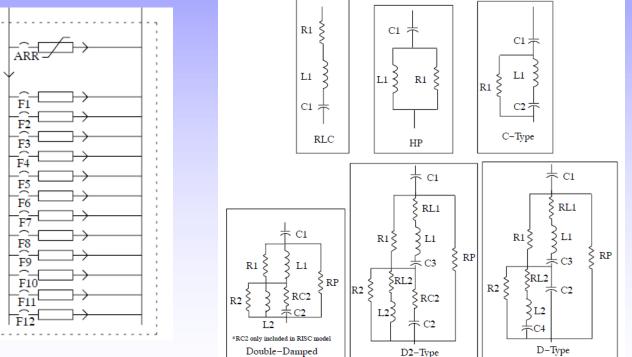


Power System Components

Other Example: Switchable Filter

Modelling filters in individual branch requires significant resources

- Switchable filter model can represent 12 filter plus 1 arrestor on 1/12 processor
- Various types of filters are included according to the requirement of manufactures





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Solution Requirements

No Interpolation and No Iteration are allowed

- The time step in real time simulation must be strictly predictable
- The longest predicted time step should be less than the time step used
- Interpolation is not possible because the firing pulse may come at the last moment within a time step, therefore no sufficient time available for interpolation
- Iteration is not possible either because the convergent cannot be guaranteed with certain times of the iteration, therefore the time step cannot be predicted.
- Alternative approaches must be taken to deal with the valve On/Off and nonlinearity within some components



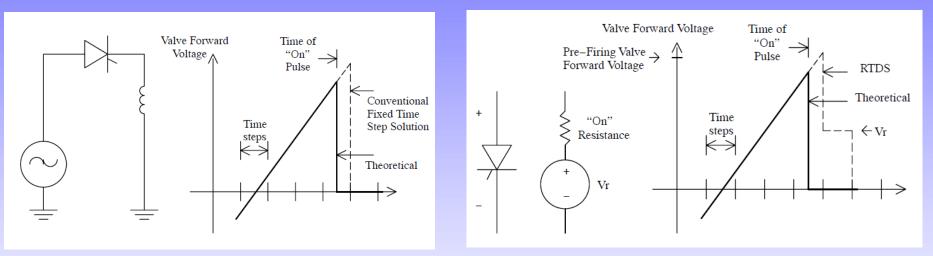


9

Modelling of HVDC Valve

Improved Firing – An Important Aspect of Digital Simulation

The Algorithm of Improved Firing



- Compensation through improved firing function instead of interpolation
- Even delay exists but possible to be adjusted
- Successfully avoid non-characteristic harmonics due to numerical jitters
- Implemented in software-hardware special design
- Same idea in creating valve current zero crossing pulse





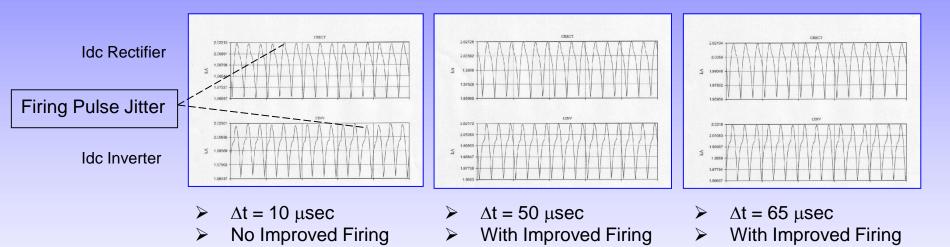
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Modelling of HVDC Valve



Improved Firing – An Important Aspect of Digital Simulation

The Effect of Improved Firing



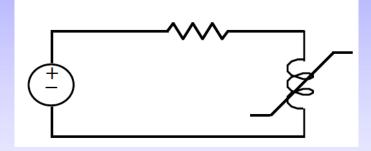


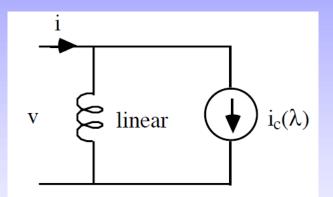


Modelling of Nonlinear Components

Example: Saturation Curve in Transformers

- Variable G vs Injection Model
- Prediction and Correct Method
- Numerical Damping





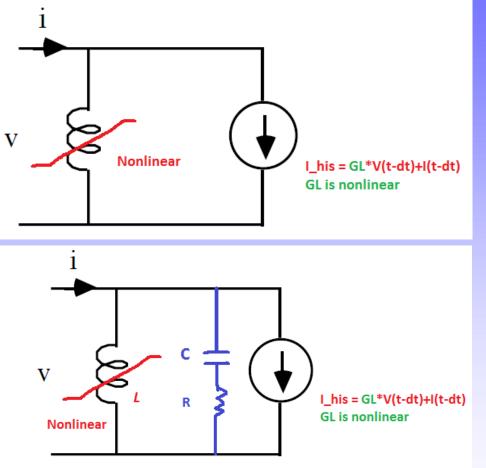




Modelling of Nonlinear Components

Example: Saturation Curve in Transformers

- Variable G vs Injection
 Model
- Prediction and Correct
 Method
- Numerical Damping



|Z(w)|=|R+jXc(w)|>>XL(w) when w=2*pi*f,f=50Hz |Z(w)| << X(w) when f is very high such as f => 1.0/dt (e.g. 20kHz)





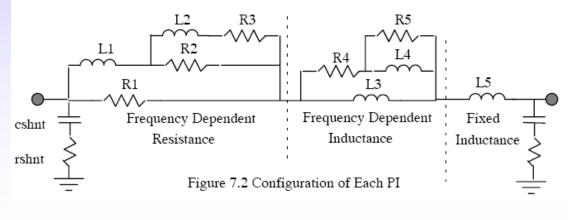
Modeling of TLINE and Cable in Small Time Step

FREQUENCY DEPENDENT PI SECTION

> The frequency dependent TLINE/Cable model cannot be used in small time step solution, because the high computation burden of convolution is not permitted in small time step;

> This model provide a frequency-dependent representation of a single-phase transmission line or cable;

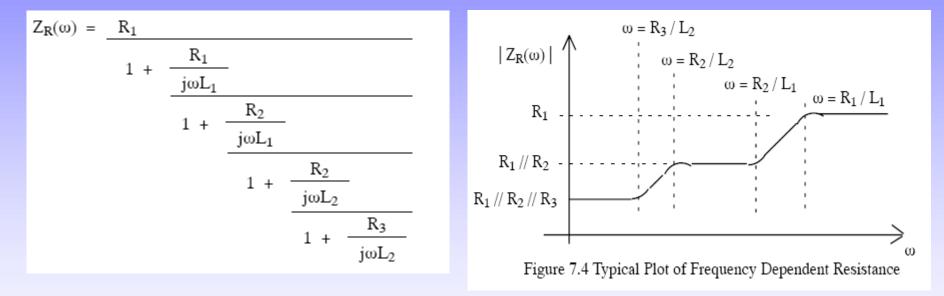
Each instance of the PI model can optionally represent between 1 and 4 identical single-phase series-connected PI sections and the intermediate nodes.





Frequency Dependent PI Section Model

Fitting the frequency dependent characteristic of resistor-





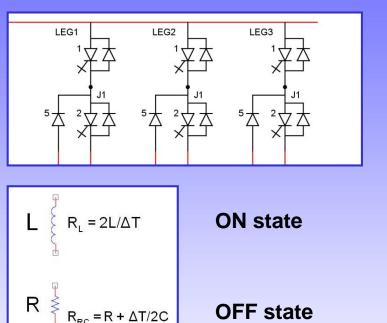


Fast VSC Simulation in Small Time Step

VSC Valve Representation



- Same branch conductance used for both the valve ON and valve OFF state
- The Dommel current history term I_H defines the valve state
- In the ON state the valve is represented as inductor
- In OFF state the vale is represented as a series RC branch
- When R_L = R_{RC} then no decomposition or inversion of the VSC sub-network conductance matrix is needed when valve states are switched







Voltage Source Converter

Solution with constant G matrix and Small ΔT

Breaker modellingOpenDommelClosedsmall Cbranchsmall LHigh
impedance R_b \downarrow Low
impedanceC= $\Delta T/2R_b$ L= $R_b\Delta T/2$

For a given C and ΔT , there is a corresponding L, which causes $\Delta T/2C = 2L/\Delta T = R_b$





MMC Model

The Trans Bay HVDC Project:

Customer	Trans Bay Cable, LLC
Project name	Trans Bay Cable Project
Location	Pittsburg, California, and San Francisco, California
Power rating	400 MW
Voltage levels	± 200 kV DC, 230 kV /138 kV, 60 Hz
Type of plant	85 km HVDC PLUS, submarine cable
Type of semiconductor	IGBT, 212 SM per arm (1,696 per converter)

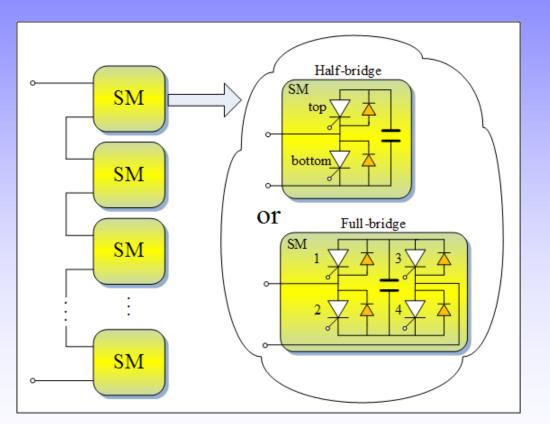








MMC Valve Model

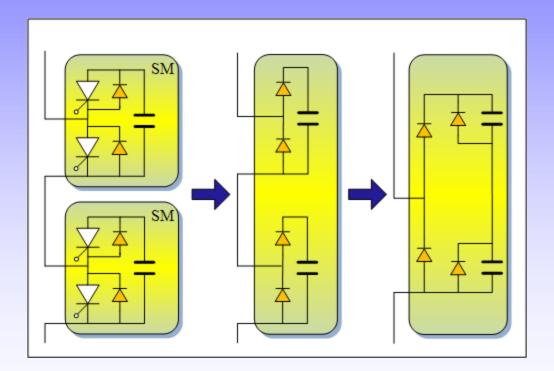


- The calculation for MMC valve model quite heavy
- The concept of a **surrogate network** employed to reduce the computational burden
- Three configurations exist:
- Blocked
- Active Inserted
- Bypassed





Configuration 1 - Blocked SM Model

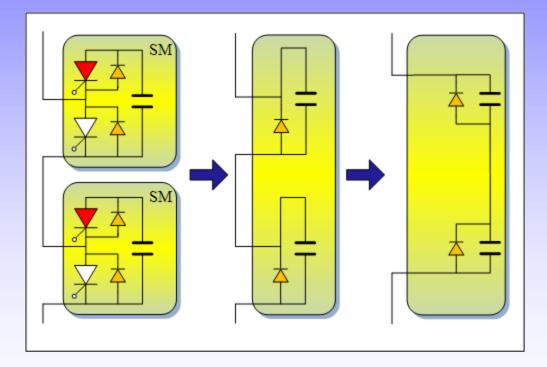


- Neither IGBT fired
- Example of 2 SMs





Configuration 2 – Active Inserted SM Model

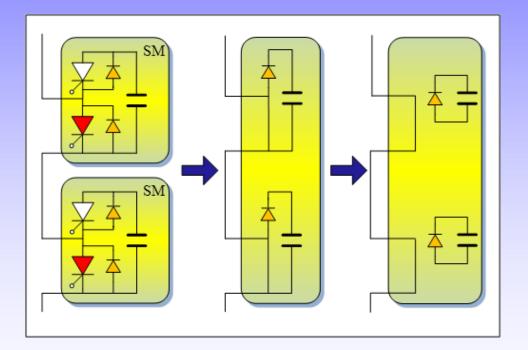


- The top IGBT fired
- Example of 2 SMs





Configuration 3 - Bypassed SM Model

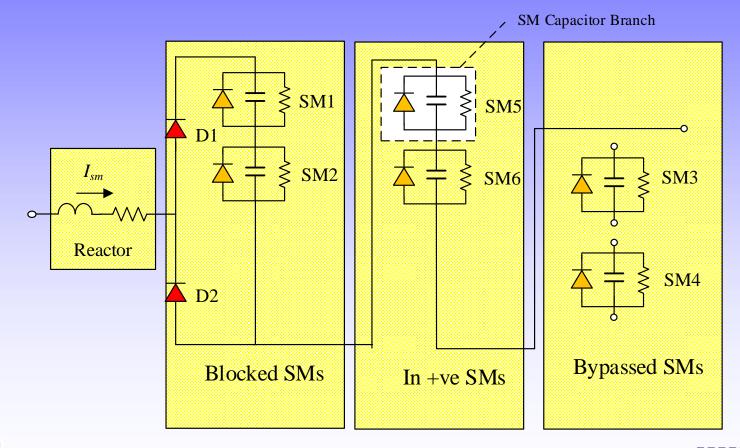


- Bottom IGBT fired
- Example of 2 SMs





Half-Bridge Surrogate Network Topology

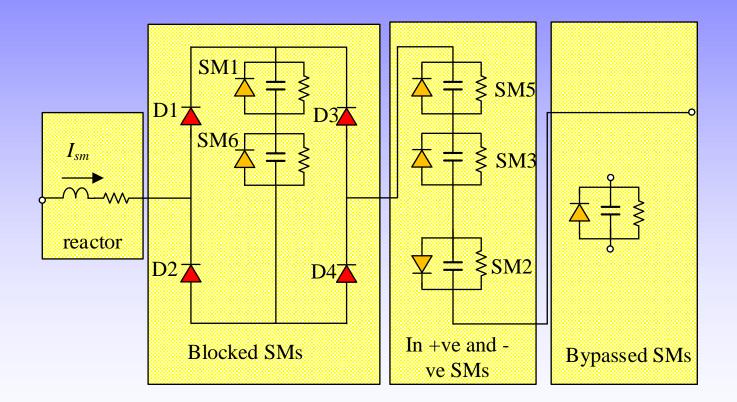






Technologies

Full-Bridge Surrogate Network Topology







Conclusions

- 1. Real Time Simulation Is Essentially A Parallel Processing EMTP
- 2. Some Specially Techniques Need to Used to Realize the Fast and Stable Solution
- 3. Questions and Answers



