TRANSIENT SIMULATION: LECTURE III
Modeling Nonlinearities In The Admittance Matrix Based Techniques

3.1 Switches

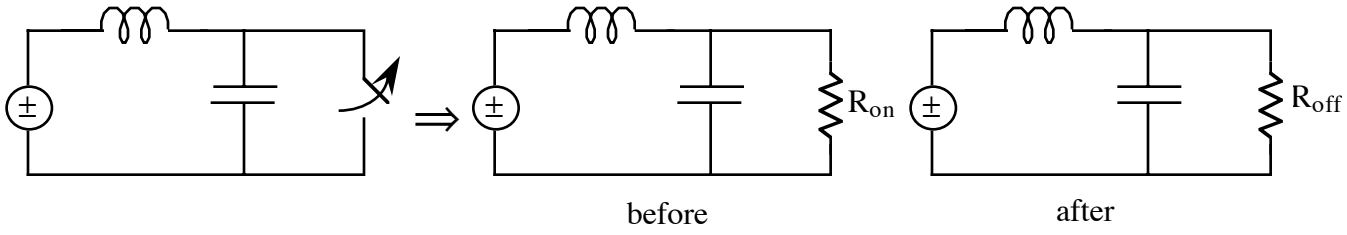


Fig. 3.1: A Network with Switching Nonlinearity

The admittance matrix can be reformulated using a different value for the switch branch resistance. An off switch can be ideally modeled by putting $g_{ij} = 0$. This procedure is quite trivial, but involves a re-inversion of the system matrix.

Many practical switches have the property that they open only on a current zero (for example circuit breakers). There is no guarantee that the current zero will occur exactly at a simulation timestep.

In the simulation, the switch might open while still carrying a current because the actual current zero lies in between timestep (see Fig. 3.2).

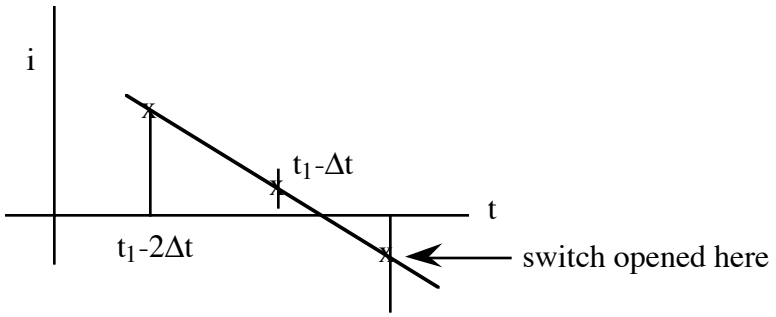


Fig. 3.2: Current zero lies between timesteps.

Opening the switch when it is still carrying a current can cause spurious voltage spikes in the solution, particularly when the switch is in series with an inductance as is often the case.

Two remedies exist:

i) Use a variable timestep, where we backtrack to $t=t_1-\Delta t$, and use smaller timesteps so that the switching instant is more closely approximated.

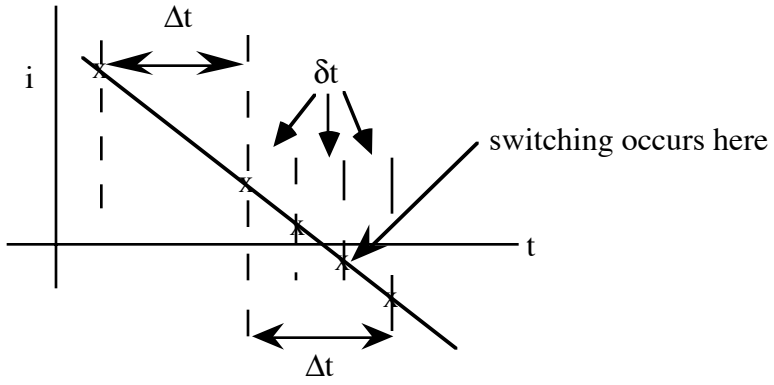
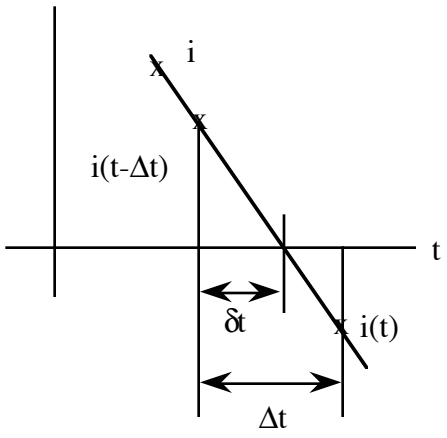


Fig. 3.3: Variable timestep reduces uncertainty in switching instant.

This procedure involves inversions of the reformulated Y matrix (All g_{ij} elements and history terms have to be reformulated for the new timestep δt).

ii) The entire solution can be interpolated to the expected switching instant, and the solution re-started from this interpolated condition, i.e.,



$$\delta t = \left(\frac{0 - i(t-\Delta t)}{i(t) - i(t-\Delta t)} \right) \bullet \Delta t$$

Fig. 3.4: Interpolating to find the likely switching instant δt.

Thus if $\underline{v}(t-\Delta t)$ is vector of voltage solutions at $(t-\Delta t)$ and $\underline{v}(t)$ is the new solution, we find the interpolated solution

$$v'(t-\Delta t+\delta t) = v'(t-\Delta t) + \frac{\delta t}{\Delta t}\left(v(t) - v'(t-\Delta t)\right)$$

Likewise the current $i'(t-\Delta t+\delta t)$ required for the history terms in the following timestep are now evaluated using these $v'(t-\Delta t+\delta t)$ voltages. We now assume that the solution is known at $t-\Delta t+\delta t$ (point A) and begin taking further timesteps of period Δt from this instant onwards. See Fig. 3.5 for an illustration of this process of adjusting the value of time.

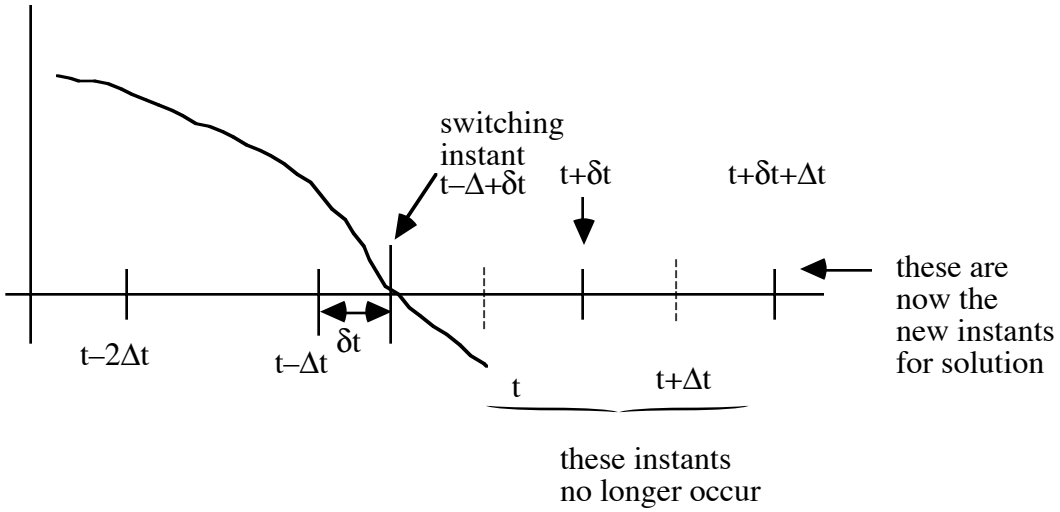


Fig. 3.5: Shifting of the solution instants due to interpolation.

This technique is relatively inexpensive on computer time compared to the variable timestep technique. It has been used in the NETOMAC program from Siemens [1] and also in EMTDC.

If LU factorization is used for matrix studies the switches should be placed between higher numbered nodes so that they appear towards the bottom diagonal of the admittance matrix. It turns out that only entries with either node number greater than that of the switch nodes have to be re-factorized thereby saving significantly on computer time.

3.2 Functional Nonlinearities

One example of these is a nonlinear resistor. Such nonlinearities may be similarly treated with the value of the resistive branch being changed in a few discrete steps.

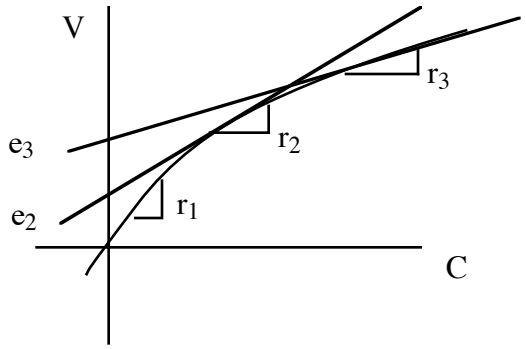


Fig. 3.6: Nonlinear Resistor Characteristic

3.3 Dynamic Nonlinearities

Core saturation is one such type of nonlinearity.

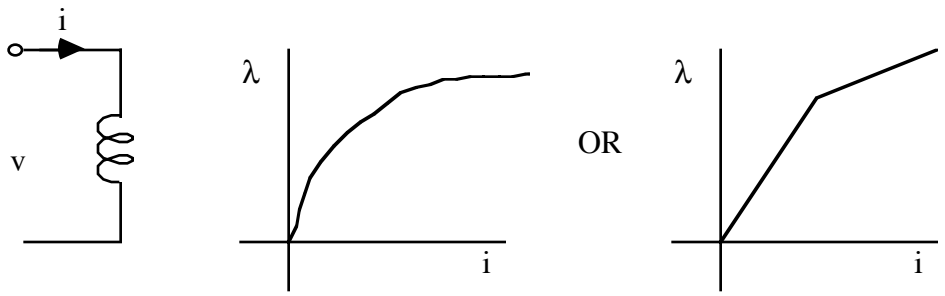


Fig. 3.7: Example of dynamic nonlinearities.

$$v = \frac{d\lambda}{dt} = \frac{d\lambda}{di} \bullet \frac{di}{dt}$$

$$= L(i) \frac{di}{dt}$$

where $\alpha(i)$ is the incremental inductance (slope of the λ–i curve) at a value of current = i. As before, we now use a trapezoidal resistance of $2L(i)/\Delta t$, and change this every timestep.

For the 2 step characteristic the incremental inductances are two different constants and are easy to model.

Again as there is an abrupt change of characteristic, a procedure such as variable timestep or interpolation of solution is recommended.

3.4 Using State Variables for Modeling Nonlinearities

For Modeling Switches, see section on modeling thyristors and diodes in the earlier state variable lecture.

For Dynamic Nonlinearities, we can reformulate the problem by replacing current or voltage variables with flux or charge, i.e.,

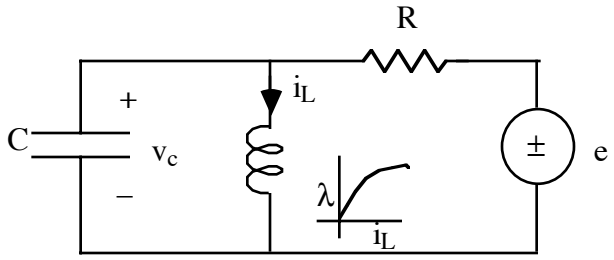


Fig. 3.8: Modeling a dynamic non-linearity with a state variable formulation.

$$C\frac{dv_c}{dt} = \frac{e - v_c}{R} - i_L$$

$$\frac{d\lambda}{dt} = v_c$$

Since i_L is a known function of λ (the saturation curve), we may replace it with this function, i.e.,

$$\frac{dv_c}{dt} = \frac{-v_c}{RL} - \frac{i_L(\lambda)}{C} + \frac{e}{RC}$$

$$\frac{d\lambda}{dt} = v_c$$

or

$$\frac{d}{dt}\begin{bmatrix} v_c \\ \lambda \end{bmatrix} = \begin{bmatrix} \frac{-v_c}{RL} - \frac{i_L(\lambda)}{c} \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{e}{RL} \\ 0 \end{bmatrix}$$

which is in the form

$$\frac{d}{dt}\underline{x} = \underline{f}(\underline{x}) + Bu$$

and may be numerically integrated by a method such as the Runge-Kutte 4rth order. Note, in general, a direct trapezoidal solution may not be possible because an inverse of f may not be easily calculable.

3.5 Use of Compensating Sources [2,3]

Often, nonlinearities can be modeled via a 'compensating' source. For example:

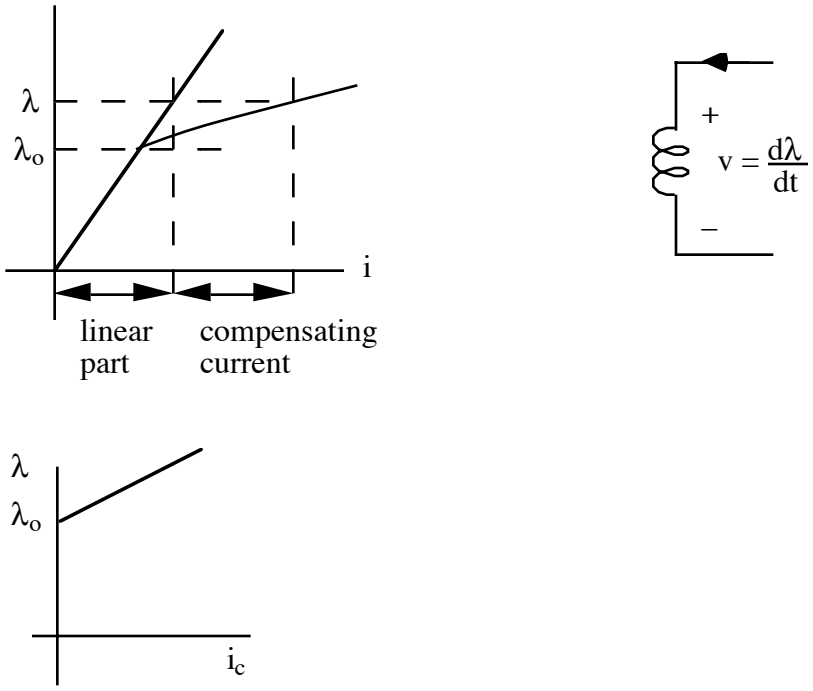


Fig. 3.9: Separating out the linear part and modeling the nonlinear part as a current source.

The inductance is then modeled as a linear inductance in parallel with a current source (or 'compensation source') as in Fig. 3.10.

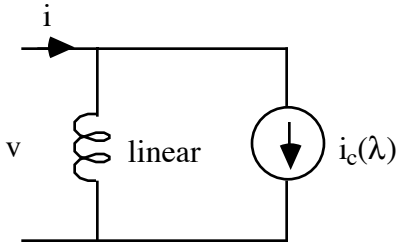


Fig. 3.10: Equivalent Circuit for the case of Fig. 3.9.

The solution is most accurate when the magnitude of the compensation is small. For this reason, we model most of the circuit behaviour in the form of the lumped inductor and only leave the saturation correction to the current source.

We could have modeled the entire response as a current source but this has a drawback.

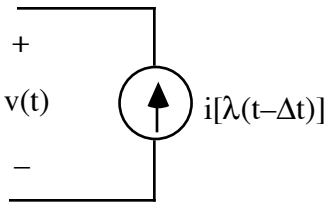


Fig. 3.11: Modeling Entirely by Compensation Source.

By necessity the current has to be calculated from past information and is thus not responsive immediately to changes in the present timestep, i.e., it behaves as an 'open circuit' to voltages in the present timestep. The effect of such "open circuit" terminations can be de-stabilizing. One way around this is to represent the one timestep behaviour by a Norton resistance (large, but not 'infinite') and to attempt to correct for the error introduced by this by using a correction source.

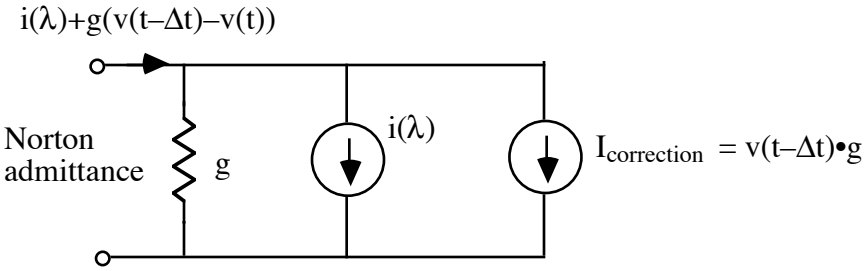


Fig. 3.12: Introducing an Interface Resistor.

3.6 Hybrid Formulations

A model such as the one in Fig. 3.12 lends itself easily for installation into an admittance matrix based simulation program because it has the admittance – current source equivalent circuit. One note of caution! It is recommended that such an approach be used if some continuity in the sourced variable is present such as an inductor current which does not change instantaneously with time. Thus non-linear inductor may be interfaced as Norton current source, and a non-linear capacitor as the Thevenin voltage source. Such approaches have been used to construct complex models such as electric machines and static compensators [3,4].

3.7 Modeling the Switching Logic

In the admittance matrix based formulations, switches are usually modeled as resistors with values that change as a function of the switching event. We have already discussed how switches are modeled in an earlier section, here we shall discuss how specific types of switches such as Thyristors, Diodes, GTOs, etc. are modeled.

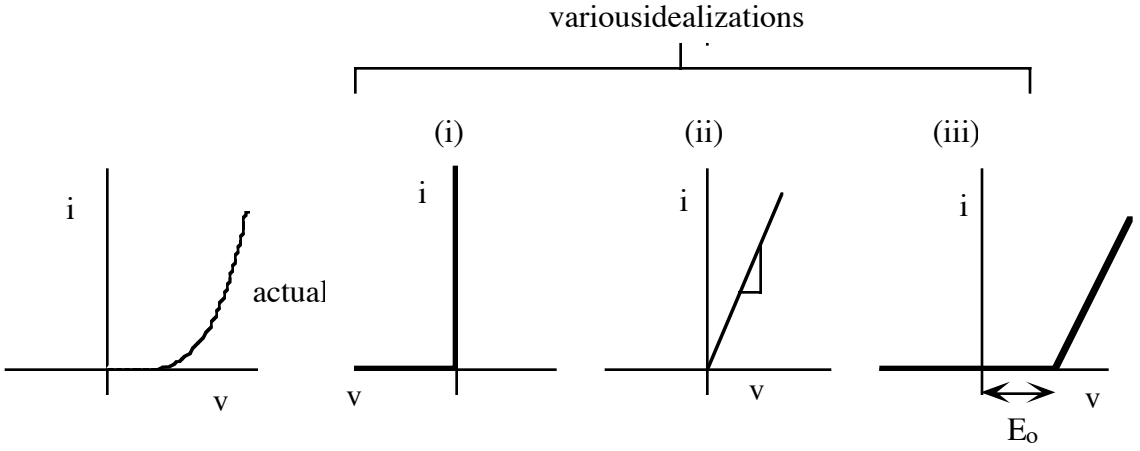


Fig. 3.13: Diode characteristics

Various idealizations of the characteristic are possible as shown in (i), (ii), and (iii) in Fig. 3.13.

Let us use idealization (ii), which is a typical approximation used in most power system applications.

Thus we have the following representation:

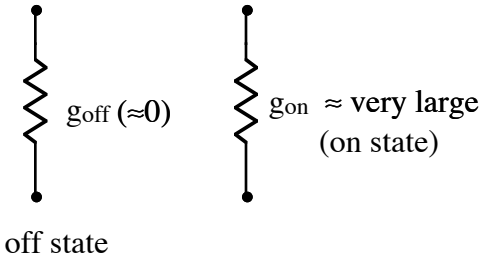


Fig. 3.14

In order to develop the switching logic, a state transition diagram is useful. Note: A diode goes on if it is forward biased and off if the current tries to reverse, i.e.,

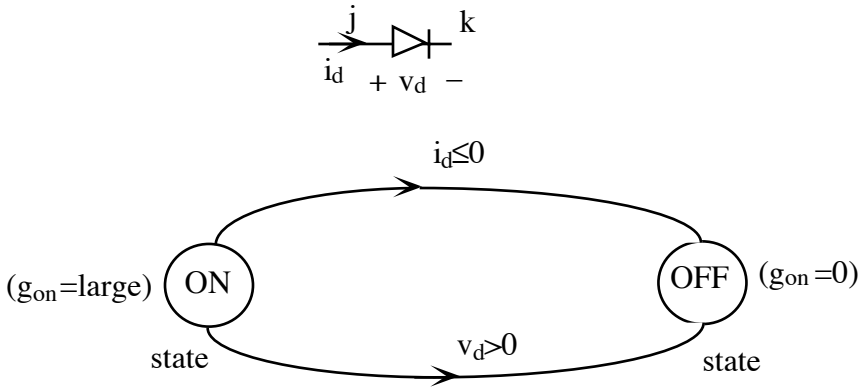


Fig. 3.15: State Transition diagram for diode switching

The following pseudocode could be used to implement a diode connected between nodes j & k.

```
if (time=0) state=off (assume an initial state)
 :
if (state=off) then                                   } off state logic
    if (v_j>v_k) then
            state=on
            g[j, k] = g_on
            call for matrix inversion (or factorization)
    else
            state=off
    endif
else if (state=on) then                               } on state logic
    if (i_jk<0) then
            state=off
            g[j, k]=0
            call for matrix inversion
    else
            state=on
    endif
endif
```

Similar switching programs can be developed for various other switching devices. The addition of interpolation/variable timestep approaches should be used in addition to the switching logic developed here if spurious switching transients are to be avoided.

Thyristors: The thyristor model is similar to the Diode Model, except that a firing pulse is required for the thyristor to turn on, in addition to the forward bias condition; i.e.

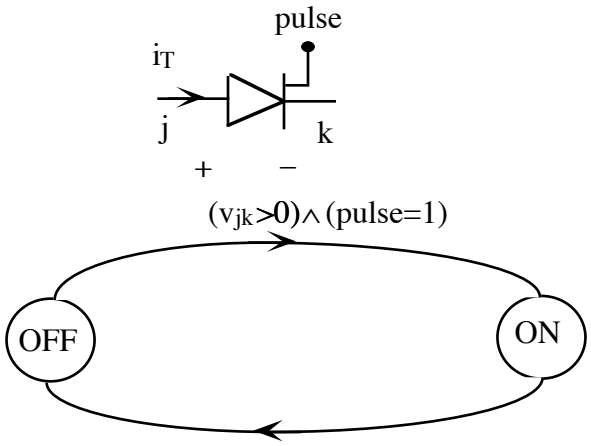


Fig. 3.16: State transition diagram for thyristor

Sometimes it is important to model the effect of inadequate turnoff time, i.e., if a thyristor has

turned off, and it is subjected to a forward bias before a sufficient 'deionization' time has elapsed, it will conduct even in the absence of a pulse. In that case, the following state transition diagram results:

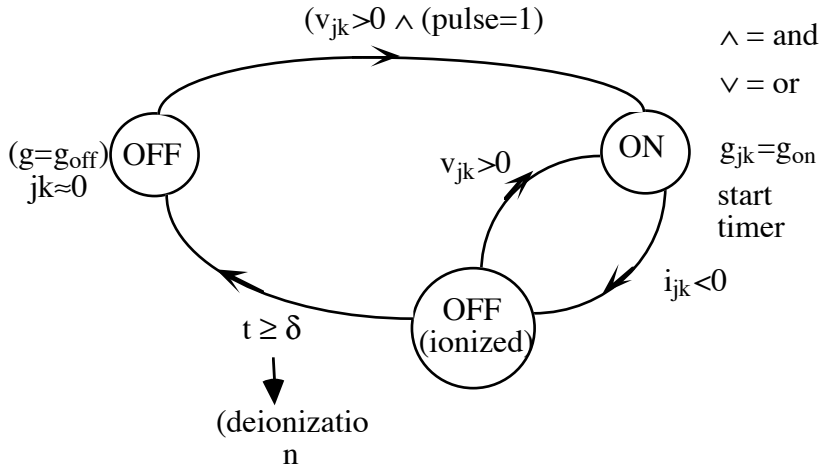


Fig. 3.17: State transition diagram for Thyristor including deionization time

Gate Turnoff Thyristor:

This device is similar to a thyristor except that it can be turned off with a turnoff with a turnoff pulse in addition to the normal reverse bids turnoff.

Thus:

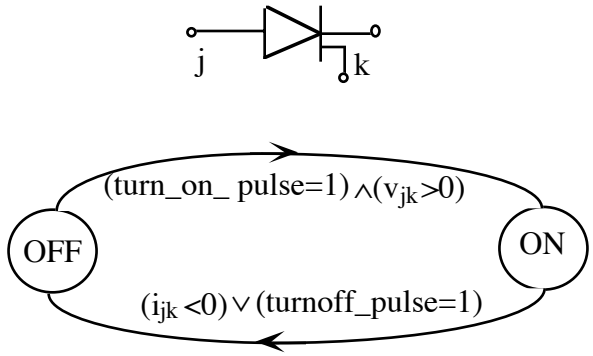


Fig. 3.18: GTO State Transition logic

Transistors, IGBTs, MOSFETs

These are turned on with a continuous on pulse applied to the gate. Very often these devices come with an antiparallel diode across them, i.e. In most circuit applications the diode usually conducts when the transistor is turned off. Fig. 3.19 shows the state transition diagram for such devices.

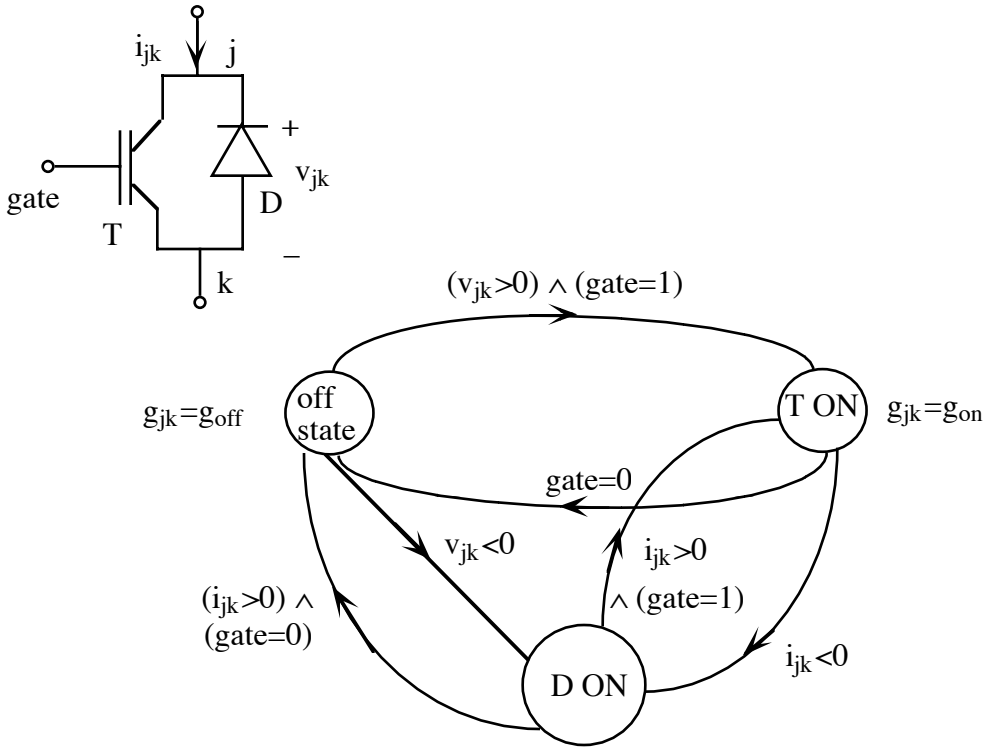


Fig. 3.19: State Transition diagram for IGBT type device with reverse conducting diode.

Other factors: Certain switching topologies make it necessary to model the resistance of the switch changing over several timesteps.

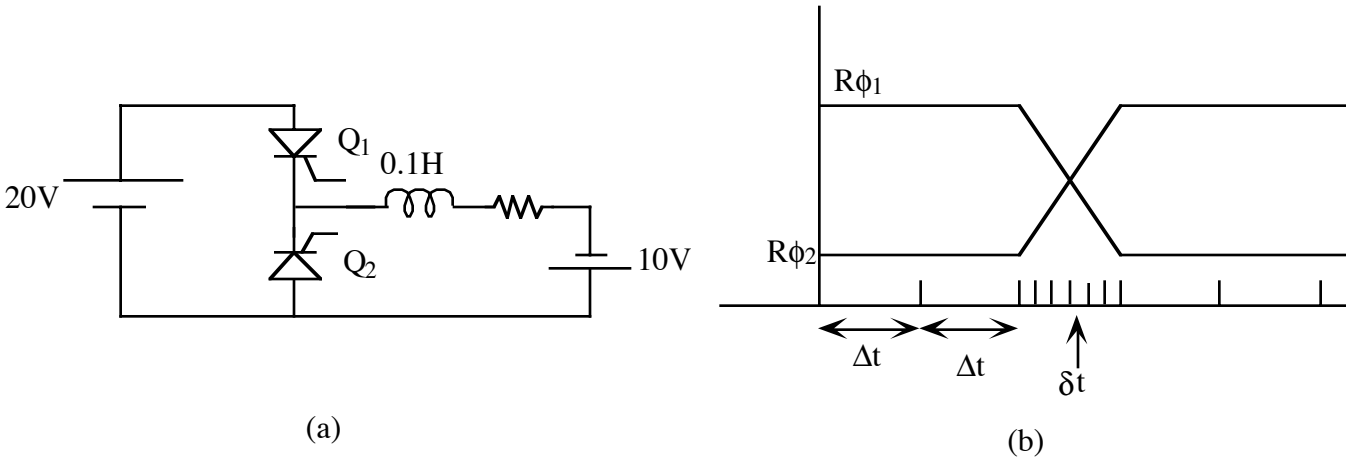


Fig. 3.20

Assume in Fig. 3.20 Q_1 has been on for a long time and is carrying 1A of current. If Q_1 is fired, Q_2 should turn off instantaneously. In a simulation with discrete timesteps this may cause problems because if Q_2 is on, firing Q_1 puts a dead short across the 20V battery causing a spike

of current. One way around this problem is to go to a smaller timestep, and turn Q_2 off gradually, and turn Q_1 on gradually as depicted in Fig. 3.20b.

Assignment 3
Do either Assignment 3A or 3B

Assignment 3A

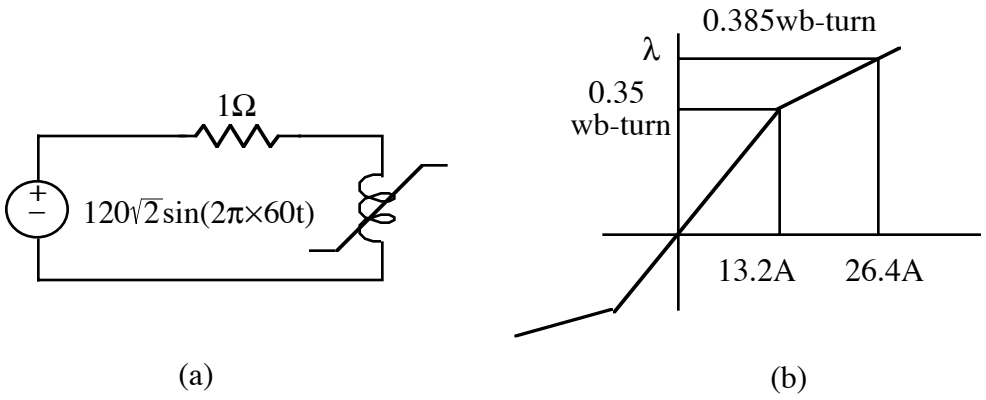


Fig. 3.21

a) Model the circuit in Fig. 3.21a using an admittance matrix formulation in which the matrix value changes when the non-linear characteristic is encountered. The non-linear inductor characteristic is as shown in Fig. 3.21b and can be considered as a piecewise linear type of characteristic. Use interpolation at the exact instant of slope change. Compare with simulation with interpolation.

b) Solve the circuit of problem (a) with a hybrid approach in which the inductor is modeled as a linear part inserted in the Y matrix, with the non-linear part treated as a current source. (Hint: λ can be calculated as $\int$ vdt, and i can be found from the λ-i curve of Fig. 3.21b.) You may use simple rectangular integration for this calculation.

c) Attempt to model the inductor as a current injection. Use a resistive interface for connecting into the Y matrix formulation. Experiment with various values of interface resistance. Don't forget to compensate for this resistance.

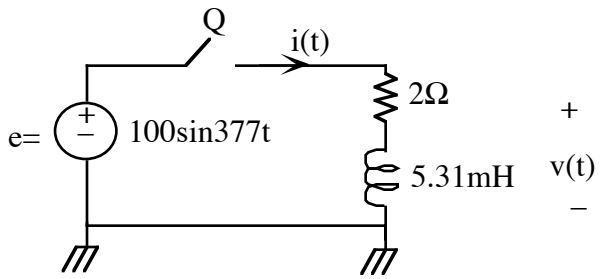
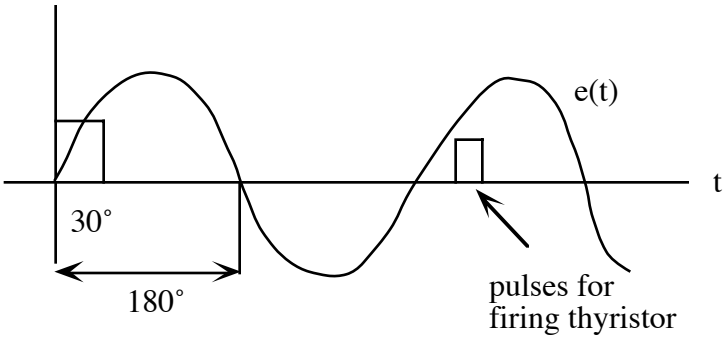


Fig. 3.22

a) For the above circuit, the switch Q is closed at t=0 and opened at t=0.2s. The switch however opens only on a zero crossing of current (the very first one after t=0.2s). Formulate an admittance matrix based solution procedure to solve for i(t) and v(t). Use interpolation to obtain the correct switching instant. Use r_{on}=0.1Ω, r_{off}=1000Ω for the switch. Compare with simulation without interpolation.

b) Modify the switch opening-closing logic to simulate a thyristor that is fired at a firing angle α=30°.



(Note: Interpolation should still be maintained). Plot v(t) and i(t).

c) Switch s in Fig. 3.23 is closed at t=0s, opened at t=0.2s. Use an ideal switch model in a state variable formulation for the circuit. Note that you must use a topologically varying network model because this switch is ideal and cannot be represented as a varying resistance. Plot i(t) and v(t).

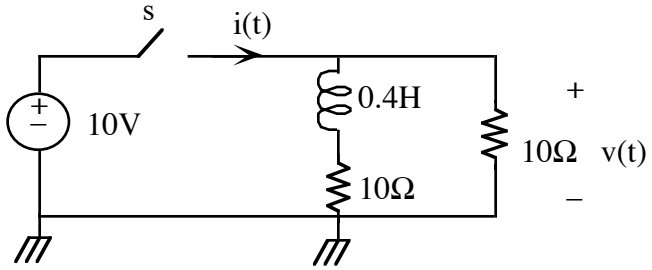


Fig. 3.23